COMPSYS 401A/B

Part IV: Interim Report

An Electronically Isolated UPS Charger-Inverter Scheme with Lightning Protection

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Summary

One of the main drawbacks of current Uninterrupted Power Supply (UPS) systems is their inability to fully protect user-applications from very high surges, such as those that happen in tropical countries. Therefore the main aim of this project was to design a novel UPS system using self contained multiple energy storage elements to transfer energy between input and output and thereby completely electrically isolating the load from the main power supply. The system was to comply with the IEEE C62.41 Class B standard and provide sufficient common and normal mode surge protection.

Supercapacitors have been used as the main energy storage element for this project and an Atmel Mega64 microcontroller has been chosen to provide control to guarantee proper functionality.

This report outlines the main aspects of the proposed design and the individual modules involved, and discusses possible design solutions considered to implement the required control. It also details out the final options chosen and their selection process along with a project schedule for the completion on the project.

Declaration of Originality

This report is my unaided work and was not copied from or written in collaboration with any other person. However diagrams and ideas common to our group have been shared between the two group members.

Signed:_____ Signed: _____
(Thusitha Mabotuwana) (Duleepa Thrimawithana)

Acknowledgement

Researching for various aspects of the project and getting started was quite a daunting task for both, me and my partner Mr. Duleepa Thrimawithana and we would like to take this opportunity to thank our supervisors Mr. Nihal Kularatna and Dr. Patrick Hu for all the support and guidance given to us throughout.

We would also like to thank the technicians Mr. Grant Sargent, Vic Church and Howard Lu for helping us gather various parts and products required for the project. The kind advice given to us whenever required is also very much appreciated.

Thusitha and Duleepa

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Glossary of Terms

A/D	Analogue-to-Digital
BJT	Bipolar Junction Transistor
DSP	Digital Signal Processor
ECE	Electrical and Computer Engineering
FET	Field Effect Transistor
IEEE	Institute of Electrical and Electronic Engineers
I/O	Input-Output
kSPS	kilo Samples Per Second
LCD	Liquid Crystal Diode
LED	Light Emitting Diode
SPI	Standard Peripheral Interface
TVS	Transient Voltage Surge-suppressor
UART	Universal Asynchronous Receiver and Transmitter
UPS	Uninterrupted Power Supply
USART	Universal Asynchronous and Asynchronous Receiver and Transmitter

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1.0 Introduction

One of the main problems, especially in tropical countries with old power distribution systems still in use is the damage caused to electronic equipment by heavy lightning. Amount of money and time spent on fixing these equipment along with the damage caused to the daily industrial workflow are simply immeasurable. Although there are many uninterrupted power supply (UPS) systems in the current market, most of these are designed in western countries that have well controlled mains supply with underground power lines which are less prone to high transient voltage spikes, hence do not provide adequate protection for the degree of lightning in tropical countries [1]. Therefore there is a high need for a novel UPS design with complete load isolation.

The main aim of this project is to design a lightning protected UPS system that can protect modern electronic equipment from a severe lightning surge of IEEE C62.41 Class B Standard[1]. The possibilities of a fully isolated inverter design using storage elements such as supercapacitors were to be considered in an attempt to stop common mode and normal mode transient surges from passing through to the user devices, thus providing better lightning protection. Also a controller subsystem was to be used to provide control for the overall system.

As briefed out in the Part IV project handout [2], the project was to be carried out by two Part IV students. The project partner was to be chosen at our own discretion and my chosen partner was Mr. Duleepa Thrimawithana (Student id: 9778679) of Electrical and Electronics Department. The main supervisor assigned for us was Mr. Nihal Kularatna and the second supervisor was Dr. Patrick Hu of ECE Department. This report focuses mainly on the control part and is structured as follows: Firstly, a brief introduction is given on some common UPS topologies and the importance of the proposed design. A project overview is given in the following section followed by a discussion related to the control aspects. An approximate timeline for the completion of the project with milestones is given towards the end and then conclusion. Relevant diagrams and tables are also included and referenced appropriately.

2.0 Some Common UPS Topologies

There are mainly three basic types of UPS topologies, off-line, line-interactive, and on-line. All three have some features in common but differing levels of performance. In general they function differently and are appropriate for different user applications [3]. Let's discuss some of the basics of these topologies and compare their functionalities with those of the proposed system.

2.1 Overview of UPS Systems

Off-line UPS systems generally have the load powered-up with the supply mains. There is sensor circuitry which monitors the input lines and switches the load from the supply mains to battery power via an inverter, if the input voltages get beyond acceptable limits, or fail completely. Off-Line UPS systems provide no line conditioning or voltage or frequency regulation, cause glitches at the output during switching and have very limited surge protection. These have low cost, good efficiency and are small in size and weight, however their reliability is quite low which make them unsuitable for devices such as network protection systems needing good stability and protection [1,3].

The line-interactive UPS systems offer the same surge protection and battery backup as the off-line systems, except that they can also provide output voltage regulation (but not frequency regulation) while operating from the supply mains. These systems provide acceptable output voltage regulation even during brownouts and/or surge conditions, under which the UPS goes to battery operation. Should the condition last long enough, the battery fully discharges and turns

[1] Refer to Appendix A for details on this Standard

the power off to the connected equipment and the UPS cannot be restarted until the main power is restored. Therefore if used in critical applications, special attention should be paid to battery replacement intervals [3].

On-line UPS systems provide the highest level of power protection for critical applications and ideal for use with the specialised, power sensitive equipment. The main advantages are; no switching involved, hundred percent line conditioning and regulation, good sustained brownout protection, typically sinusoidal output, power factor correction and very high reliability [1]. Although these systems are very robust, they have very complex designs than the first two topologies and have a higher price, weight and volume [1,3].

2.2 Existing Systems vs. Proposed System

As discussed above, the off-line and line-interactive UPS systems are very prone to surges and other voltage transients which make them unsuitable for devices that need good line stability. The level of protection of these systems can be enhanced by integrating them with devices such metal oxide varistors, transient voltage surge suppressor (TVS) diodes and TVS thyristors and having an inductor in series to suppress common and normal mode surges [1], but at a considerably higher cost. On the other hand on-line UPSs provide very good surge protection and regulation but their cost makes them unrealistic for domestic use.

The proposed design suggests that the user-end be completely electrically isolated from the mains at all times to provide very good surge and lightning protection. Energy storage devices (such as supercapacitors) are proposed to be used to transfer the energy from input to output by using suitable switching techniques. Due to the complete load isolation a fully functional system is expected to protect the load even from the heavy lightning seen in tropical countries, something which even most of the on-line systems fail to cope with [1]. Cost is expected to be around that for an off-line or line-interactive UPS but with better surge protection capabilities than on-line systems. Another advantage can be seen as the environmental friendliness over on-line UPSs. On-line UPSs use battery power continuously and the batteries undergo constant charging and discharging. This process shortens their useful life and disposal can be pollutive and costly. In contrast, super capacitors virtually have an unlimited number of charge-discharge cycles hence have longer lives and produce no toxic substances.

We intend to design a 200W UPS with Class B type lightning protection and the main aim is to prove a new concept. Therefore we do not intend to develop a fully functional prototype with any of the power management, power factor correction, user interfaces and other advanced schemes commercial systems have, mainly due to time constraints.

3.0 Project Specifications and Overview

The main aim of the project was to design a UPS with common and normal mode isolation. Energy was to be transferred to the output from the input via some self contained multiple energy storage elements while accounting for redundancy. The whole system was to be monitored and duly controlled with some processor based control system.

Amid many possibilities, the main charge-holding device for this project was decided to be supercapacitors[2]. Using a systems approach, six main modules were identified, namely the energy pump or the supercapacitor charger, charge-holding devices or the supercapacitor banks, inverter, controller subsystem, battery backup and battery charger. This section outlines the individual modules involved and gives a rough breakdown of the tasks between the group members.

3.1

[2] Refer to Mr. Thrimawithana's report for other options considered and details of the selection process

Overview of the system and the individual modules

Shown below in Figure 3.1 is a block diagram of the overall system.

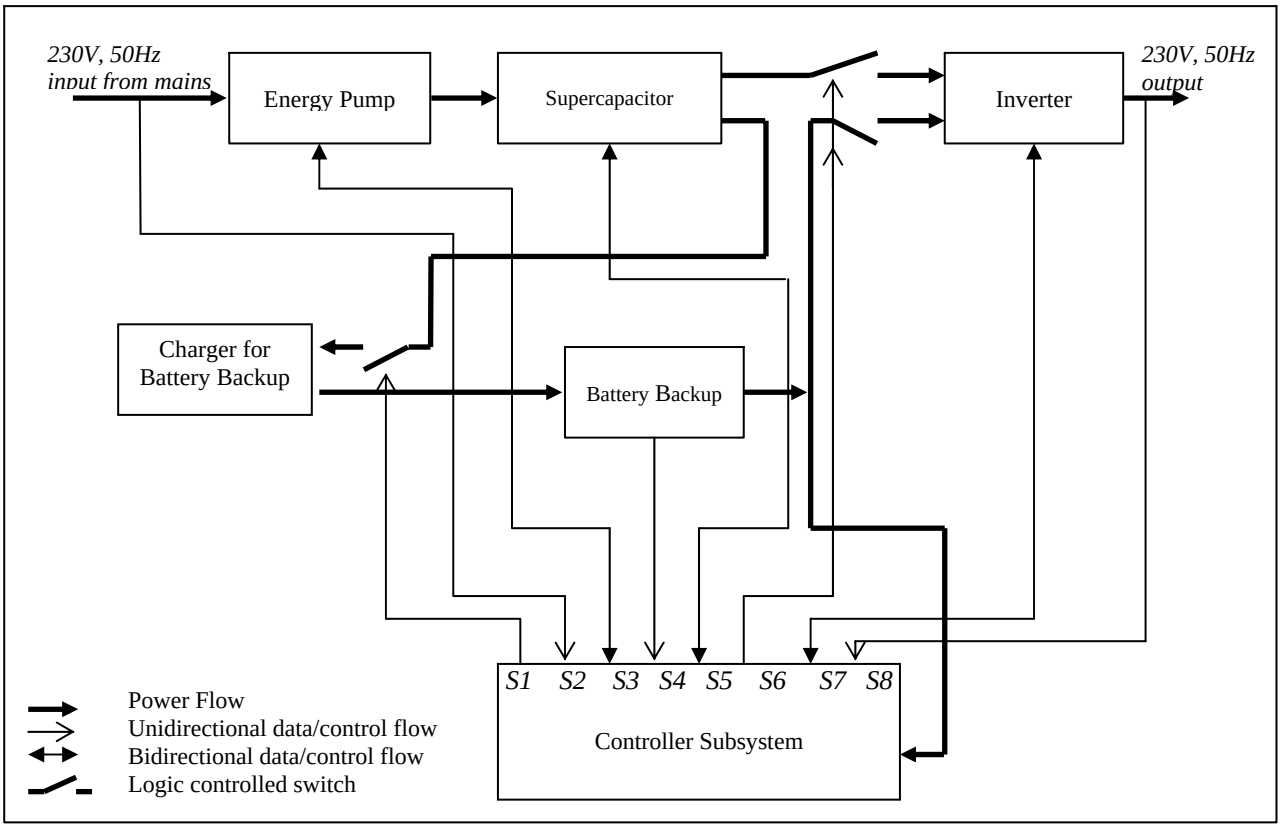

Figure 3.1: Block diagram of the overall system

The input to the energy pump or the supercapacitor charging block is the mains supply with 230V, 50Hz. Whenever a supercapacitor bank needs to be charged, the controller subsystem will set appropriate control signals and establish electrical connection between the bank and the input.

At any given time, a supercapacitor bank will be in discharging mode to ensure uninterrupted power supply at the inverter end, provided that this general mechanism has not been changed as during a blackout. Part of the discharging bank's energy will also be used to power-up the backup battery charger whenever this needs to be used. At this stage of the development process, five supercapacitor banks (with each containing several supercapacitors) are thought to be adequate to supply the load. In case of a high voltage transient, there is a possibility of the charging bank blowing up which is the reason for the redundant banks. However this number is subjected to change during the course of the project based on charging mechanisms, charging and discharging rates of supercapacitor, storage of supercapacitor and so on.

The input to the inverter will be from the supercapacitor banks or from the battery. The former will be used under normal operating conditions whereas the latter will provide the energy in the event of a blackout. The input to this inverter block is $12V_{DC}$ which will be converted to $230V_{AC}$, 50Hz at the user end.

The battery backup is used to power-up the controller subsystem since the controller needs to be protected from any incoming surges. Also it is used to supply power to the load for about fifteen minutes in the event of a blackout. The charger will be used to recharge the battery after it reaches a certain minimum voltage.

The main purpose of the controller subsystem is to ensure correct and timely functionality of the overall system. It has to monitor the line voltages to detect any incoming surges, switch the capacitor banks to guarantee uninterrupted power supply at the inverter end and also monitor the battery health.

3.2 Breakdown of tasks between the group members

The charger unit, capacitor bank module and the inverter were to be designed by my project partner, Mr. Thrimawithana since these require sufficient knowledge in power electronics design. I was to develop algorithms for switching, research for a suitable battery and a charger we could use and also work on the development of the controller subsystem using my knowledge in control and embedded systems design, signal processing and computer systems. Therefore this report focuses mainly on the design issues involved with the controller subsystem and the battery backup and its charger. Issues related to the other modules can be found in Mr. Thrimawithana's interim report.

4.0 Controller Subsystem and Battery-Backup

Research for the battery backup system and charger was given less priority over the other since it is required mainly in a final product implementation and not in a proof-of-concept design. Discussions with the supervisor suggested that trying to design our own charging system within the given time constraints of the project will not be feasible, hence it was decided to simply use a commercially available charger. This section discusses the controller's main tasks, selection process for a suitable controller, battery backup systems considered and possible ways of powering up the controller.

4.1 Controller subsystem and its tasks

The controller subsystem was to provide control for the whole system and had to be well chosen to ensure it could meet all the requirements of the individual modules. The main tasks of the controller can be listed as follows:

1. Monitor the input lines and surge detection
2. Monitor the capacitor bank voltages
3. Monitor the output voltage
4. Ensure timely switching of the supercapacitor banks, inverter and charger
5. Detection of faulty supercapacitors
6. System initialisation at start-up
7. Monitor battery health
8. System shutdown

4.1.1 Monitoring the input lines and surge detection

The input lines need to be monitored continuously to prevent any power interruption to the load from surges, spikes, sags, voltage transients, brownouts and blackouts. Although the actual values of the voltages are not decided yet, the idea is to give a certain minimum and maximum voltage (say 200 and 330V_{AC} respectively) and consider any line voltage outside this range as a potential spike/sag. A simple circuit as in Figure 4.1 will be used to detect these conditions.

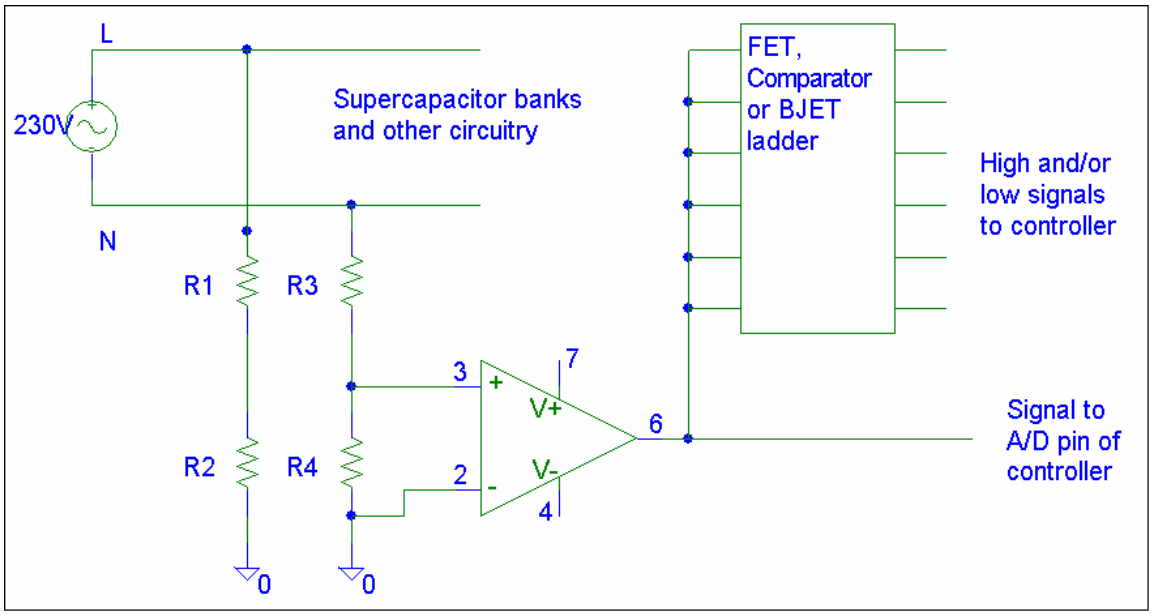

Figure 4.1: Simple circuit used to measure line voltage

The first part of the above figure will be the same irrespective of whether the ladder circuit block is being used or not. The voltage dividers R1,R2 and R3,R4 will give the controller a signal on one of its Analogue-to-Digital (A/D) pins. If used, the controller will also receive the outputs from the ladder circuit via some input pins[3]. The purpose of the ladder circuit block is to give the controller a set of high/low signals depending on the line voltage. These high/low signals can then be used by the controller to determine a range (for example if the first two signals were high the range corresponds to 500-600V, if the first four signals were high the range is 1000-1500V and so on), in the event of a surge coming through. This ladder circuitry can even be completely eliminated by using a controller such as a Digital Signal Processor (DSP). Discussed below are some of the design options.

1. Using a DSP with built-in A/D converters: DSPs are very commonly used in commercial UPS systems and models such as Motorola DSP56F80x and Analog Devices ADSP-2199x offer very user-friendly features for UPS system design with very high accuracy and speed. These new DSPs, or hybrid controllers, combine the power of traditional DSPs with microcontroller features to provide very high sampling rates of around 20MSPS, with up to 14-bit resolution [4,5]. Therefore using one of these to monitor the line voltages will guarantee precision of the measurements and also help detect any unwanted voltage variations without the use of any ladder circuitry. At the same time, the DSP chips are fairly expensive and the university hasn't got any of the new chips with the built-in A/D converters in them. Lack of my experience in working with a DSP system and the requirement to learn how to program and debug such a system within the given duration of time can be considered the main drawbacks.

2. Using a microcontroller with built-in A/D converters: Compared to the DSPs, these have lower sampling rates and lower A/D resolution. Generally most microcontrollers have 8-10 bit resolution and around 10-20 microsecond sampling intervals. This will be sufficient to monitor the line voltages under normal circumstances, but not when there's a voltage surge which would last only a few microseconds requiring higher sampling rates. However this option can be used along with the ladder circuitry as the main processor clock (which will be much faster than the A/D clock) can be used to determine voltage levels on the ladder outputs. This option will be cost effective and make the development process relatively faster

[3] Note that there will be similar circuitry even for the R1,R2 voltage divider as for R3,R4, though not shown in the diagram

compared to a DSP, since I will be able to use my knowledge and experience in microcontroller programming.

3. Using a simple DSP or a microcontroller with a separate A/D chip: This is another possible and a feasible option. A relatively simple DSP or a microcontroller can be used with a separate A/D chip with a high sampling rate. A UART, USART or SPI connection can be used for the main processor to communicate with the external A/D chip when necessary. The ladder circuitry will not be required since the surge can be sampled by the fast A/D chip, but this option will be rather costly since a microcontroller or a DSP *and* an external A/D chip will be required.

An important point to note is that if the ladder block is used in Figure 4.1, we will be able to determine only a range for the voltage but not the actual voltage itself. However final resolution will depend on the number of different steps implemented within the ladder block. There are a few options that can be used for this ladder circuitry if used, as summarised in Table 4.1.

Property	Analogue Comparators	BJTs	FETs
Cost	High	Low	Low
Switching speed	Low	Moderate	High
Ease of implementation	Easy	Hard	Easy
Availability	Readily	Readily	Readily

Table 4.1: Comparison between different options for the ladder circuitry

From the controller's perspective, monitoring the line voltages and detecting surges can be considered the most important, requiring critical timing. All other processes of the system are much slower than this process since any of the very short duration pulses or surges in the input will appear here first, which need detection. Therefore the selection of the controller subsystem will depend mainly on the timing requirements of this task.

4.1.1.1 Selecting a suitable controller

The two main options for a controller were a DSP system or a microcontroller. Microcontrollers are generally used primarily in control-oriented applications that are interrupt-driven, sensing and controlling external events whereas DSPs are traditionally found in systems that require the precision processing of digitised analogue signals [6]. Some of the advantages of a microcontroller are efficient control of external devices through I/O ports with bit-level control, hardware support for expansion, direct interface to switches and digital status signals, low software overhead and lower price compared to DSPs. The DSPs have the advantage of having digital filtering in few cycles, hardware support for translation of analogue signals and high-speed serial ports [7]. However DSP chips are more expensive.

For this project it was decide to use a microcontroller instead of a DSP due to the following reasons:

- We are not trying to develop a surge measurement system, so there's no need to determine the actual value of the surge. A range such as 500-1000V, 1000-1500V will be sufficient, which can be measured by using the second or third technique in Section 4.1.1. Therefore there's no need for very high sampling rates.
- The cost of a DSP system is very high compared to a microcontroller and will not help in minimising cost of the product.
- A microcontroller can be used to accomplish all the required tasks of the controller subsystem except for measuring an exact value for a high voltage transient.
- I have no prior experience working with a DSP system and difficulty of properly learning such a system within the given time constraint.

An Atmel Mega64 chip has been chosen for this project after a thorough comparison between microcontrollers from Atmel, Microchip and Motorola. Appendix C provides details of various features considered in this decision process.

4.1.1.2 Surge detection

To monitor the input line voltages, option two of Section 4.1.1 is preferred over option three. The built-in A/D converter of the chosen microcontroller runs at 15kSPS [8] and is sufficient to monitor the line voltage under normal operating conditions. In the event of a surge coming through, the ladder circuit will send out high and/or low signals to the microcontroller. As these high/low pin voltages will be monitored by the microcontroller's main clock, a range for the voltage transient along with a value for the duration of the transient can be determined. This process eliminates the requirement for an external fast A/D chip, and also minimises cost.

FET switches were decided to be used in the ladder block in Figure 4.1 since these are very fast and cost effective compared to the others.

4.1.1.3 Sags, brownouts and blackouts

These voltage transients can be detected by the microcontroller as the input lines are continuously monitored. The idea to detect these conditions is to compare the output with the input and if the input is considerably low over a certain period of time (say 15ms which is normal for most sags and other transients [1]) , change to battery mode.

4.1.2 Monitoring the supercapacitor bank voltages

Each capacitor bank has a relay and two switches along with the driver/isolation circuits (please refer to Mr. Thrimawithana's report for these circuit designs and the development process of this module) as shown in Figure 4.2.

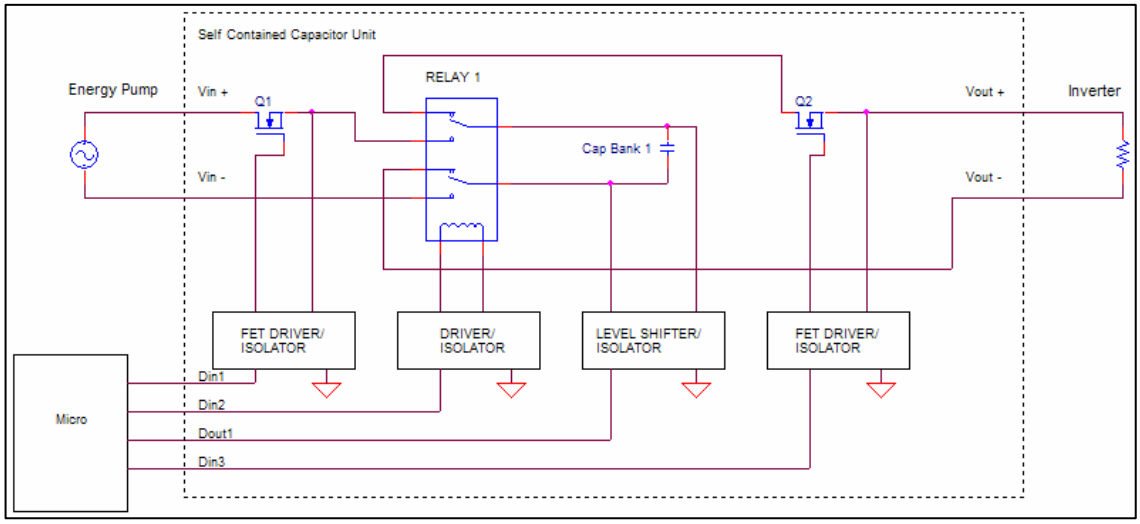

Figure 4.2: Block diagram of a self-sustained supercapacitor module (as seen from the electronics)

The input to the microcontroller is the voltage across the capacitor bank[4] and the outputs are three on/off signals to drive the relay and the switches, for each capacitor module. The ways in which these voltages can be monitored are very similar to the discussion in Section 4.1.1, apart from the fact that only the microcontroller's A/D converter *or* the ladder of FETs in Figure 4.1 will be required due to the absence of any high voltage, short duration spikes.

[4] The input voltage from each bank will be with reference to the microcontroller's ground plane and this has been achieved using electronics. Refer to Mr. Thrimawithana's report for more details.

These bank voltage measurements do not require very high sampling rates. For example, we will need to check for the bank voltages only on a millisecond, or even a second based timescale instead of a microsecond timescale as for a surge and this can be easily achieved with the 15kSPS A/D converter. Therefore the microcontroller's A/D converter will be used which will eliminate the cost of any FET circuitry required by the alternative option.

4.1.3 Monitoring the output voltage

This end of the system is expected to be $230V_{AC}$ and totally surge free, hence does not need any high frequency sampling. The measurement process and discussion is very similar to that in Section 4.1.2 where the voltages will be measured using the microcontroller's A/D converter.

4.1.4 Timely switching of the supercapacitor banks

The capacitor banks need to be switched between charging, discharging or standby modes according to some predetermined manner to guarantee uninterrupted power supply at the user-end. It was decided to use a state diagram as shown in Figure 4.3 below to implement these different modes of operation.

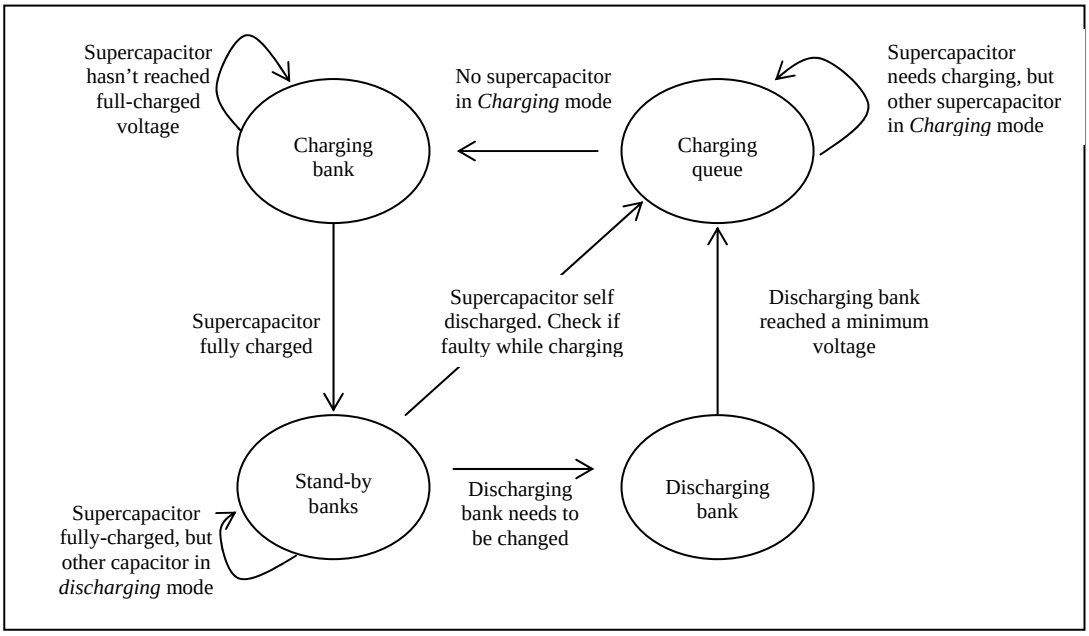

Figure 4.3: State diagram showing capacitor bank states

The banks will be changed to the different modes of operation by setting appropriate control signals. Since the microcontroller will be monitoring the charging, stand-by and the discharging supercapacitor bank voltages, it will know which switches to turn on and/or off. However one important point is that when switching it is important to ensure that the one of the charged banks in *standby* state is moved to *discharging* state before that bank is switched to the *charging queue*. This consideration is important to maintain continuous power for the load. The switch state control signals sent out by the controller to the banks and the charging unit are explained in more detail in Appendix B.

4.1.5 Detection of faulty capacitors

A count-down timer with a higher than normal charge time (for example, if a supercapacitor bank generally takes 2 seconds to reach full charge, the timer will be set to around 4 seconds) will be started each time a supercapacitor bank is moved into *charging* state. If this timer times-out (i.e. reaches zero) before the bank reaches the full-charged voltage, the bank will be considered faulty. It is assumed that once a supercapacitor bank is fully charged, it will not get faulty until it cycles back to the *charging* state; hence time-outs will not be used on the supercapacitor in any of the other states. The user will be notified of the faulty bank by means of a LCD or LED display.

4.1.6 System initialisation at start-up

At start-up, it is required to initialise the system by setting the control signals appropriately. The capacitor bank voltages need to be measured and their correct states determined, battery backup system checked and presence of line input signal verified. Also it is important to determine if any of the capacitor banks are faulty by using techniques described in Section 4.1.5 before the processor moves onto its normal mode of operation. Some calibration technique might also be required by the whole system at start-up, which has not been decided on at this stage.

4.1.7 Monitoring battery health

The backup battery health needs to be monitored on a regular basis in order to ensure power-on state of the controller at all times. Similar techniques to those described in Section 4.1.3 can be used to determine the current health level. This voltage level needs to be measured on a minute based timescale since the controller is expected to use up only a very few milliamperes during its normal mode of operation. Once the battery terminal voltage drops to a certain minimum level, control signals should be set to turn the battery charger on. However battery health will need to be monitored more often, presumably on a second based timescale in the event of a blackout, since it'll be used not only to power up the controller but also to supply the load hence undergoing a higher rate of power dissipation.

4.1.8 System shutdown

There are two cases where a total system shutdown will be inevitable. In the event of a blackout, the battery back-up is designed to power up the system only for around fifteen minutes after which the system has to be shut down since the battery will be fully drained. The second scenario is if the user plugs in a load with a higher VA rating that the system is designed for. The capacitor banks will not be able to keep up with this power requirement hence a system shutdown will be performed.

4.2 Battery backup

Six different types of rechargeable batteries in the market were considered, namely NiCd, NiMH, Lead Acid, Li-ion, Li-ion polymer and reusable alkaline. Each one has its own advantages and disadvantages as summarised in Table 4.2.

Property	NiCd	NiMH	Lead Acid	Li-ion	Li-ion polymer	Reusable Alkaline
Gravimetric Energy Density (Wh/kg)	45-80	60-120	30-50	110-160	100-130	80 (initial)
Internal Resistance (includes peripheral circuits) in mW	100 to 200[1] 6V pack	200 to 300[1] 6V pack	<100[1] 12V pack	150 to 250[1] 7.2V pack	200 to 300[1] 7.2V pack	200 to 2000 6V pack
Cycle Life (to 80% of initial capacity)	1500	300 to 500	200 to 300	500 to 1000	300 to 500	50 (to 50%)
Fast Charge Time	1h typical	2-4h	8-16h	2-4h	2-4h	2-3h
Overcharge Tolerance	moderate	low	high	very low	low	moderate
Self-discharge / Month (room temperature)	20%	30%	5%	10%	~10%	0.3%
Cell Voltage (nominal)	1.25V	1.25V	2V	3.6V	3.6V	1.5V
Load Current - peak - best result	 20C 1C	5C 0.5C or lower	5C[7] 0.2C	>2C 1C or lower	>2C 1C or lower	0.5C 0.2C or lower
Operating Temperature (discharge only)	-40 to 60°C	-20 to 60°C	-20 to 60°C	-20 to 60°C	0 to 60°C	0 to 65°C
Maintenance Requirement	30 to 60 days	60 to 90 days	3 to 6 months	not req.	not req.	not req.
Cost per Cycle (US$)	$0.04	$0.12	$0.10	$0.14	$0.29	$0.10-0.50
Commercial use since	1950	1990	1970	1991	1999	1992

Table 4.2: Comparison of characteristics of some commonly used rechargeable batteries [modified from 9]

The system is to be designed to run without any interruption for about fifteen minutes in the event of a blackout. It was decided to use a 12V battery to supply the 200W required, which requires approximately 20A/s. Most of the above batteries range from 1000-1800mAh and using an average battery of 1500mAh, we can get

$$\frac{1.5\text{Ah x } 60\text{s x } 60\text{s}}{20\text{A/s}} = 4.5mts$$

This figure means that we'd require at least three such batteries in parallel to run the system for around 15 minutes. Also since a current of 20A will be required each second, several batteries will need to be used in parallel to contribute for the required current with each branch containing a few batteries in series to get the required voltage. However if the parallel arrangement to get the required current is less than three, at least one more parallel branch will need to be added to gain the fifteen minute duration.

A NiCd battery was decided to be used for this module due to its advantages over the other batteries along with a suitable commercially available charger, which hasn't been decided on yet.

4.3 Power for the battery charger

Power for this unit could be derived from either point A, B, C, D or E as shown below.

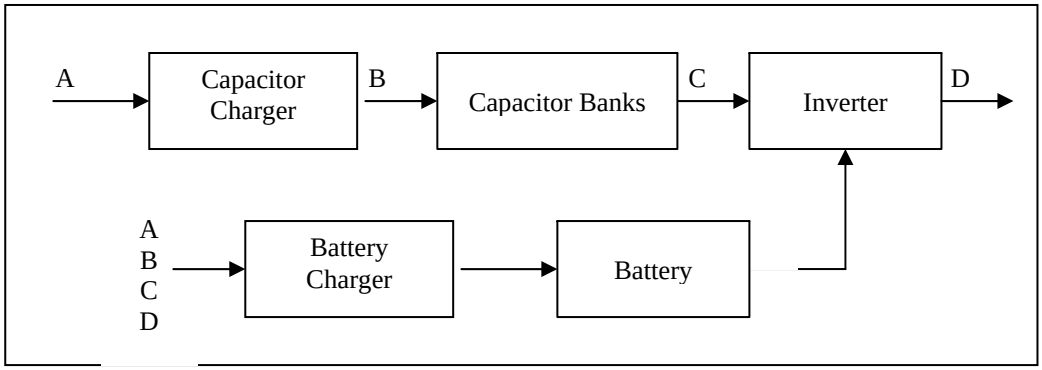

Figure 4.4: Different possibilities of powering up the battery charger

The table below shows a comparison of these five options.

Position/ Option	Rectification	Step-down transformer	Filter	Subject to surges
A	Yes	Yes	Yes	Yes
B	No	No	Yes	Yes
C	No	No	No	No
D	Yes	Yes	Yes	No

Table 4.3: Comparison of possibilities for battery charger power-up

By taking all the pros and cons as outlined in Table 4.3 into account, position **C** was determined as the best option to power-up the charger when required.

4.4 Control for the overall system

Figure 4.5 shows the inputs received by the microcontroller and the generated control signals along with a brief description of their overall functionality. Please refer to Appendix B for details on the individual control signals and the modules they control.

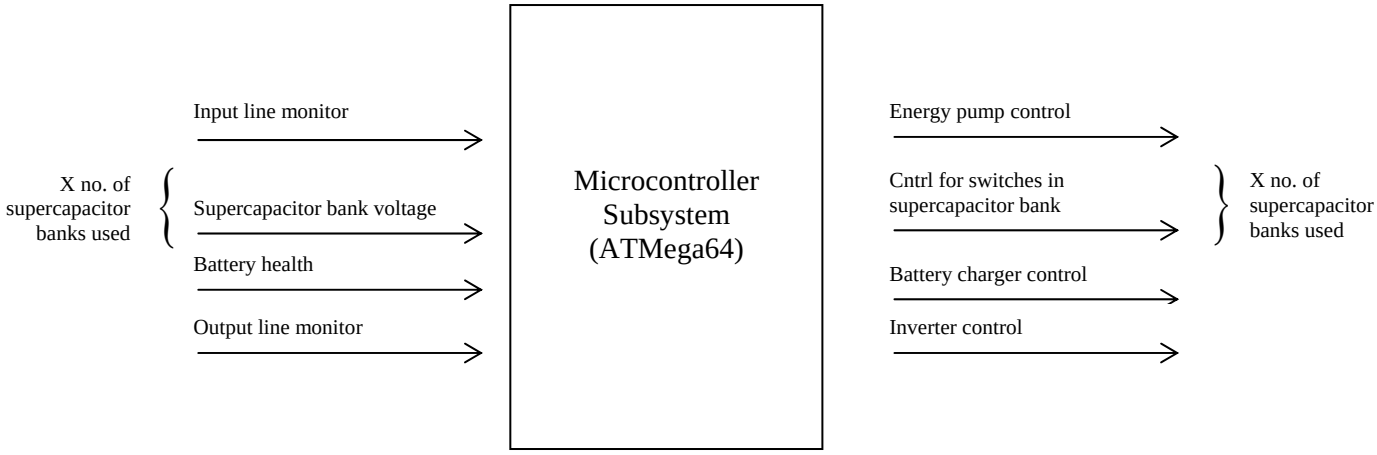

Figure 4.5: Control for the overall system

The line input voltage will be on one A/D pin as well as on multiple high/low input pins of the microcontroller depending on the number of stages implemented (i.e. resolution) in the ladder circuit in Figure 4.1. Under normal conditions the A/D pin will be used to monitor the 230V, 50Hz input, whereas the high/low values on the other pins will be used to measure the surges. The surge voltage will appear even on the A/D pin but this will last for too short a duration for the microcontroller A/D converter to detect it. Other inputs are as the names imply. All the outputs shown in Figure 4.5 are logic based and a *low* or *high* voltage (i.e. 0 or 5V) will be outputted.

As explained in detail in Appendix B, a total of about 40 I/O lines are required to provide control for the whole system and the controller has been chosen to meet this requirement. However it should be noted that the above control signals are determined using the current configurations for the supercapacitor banks and the inverter. These are likely to be changed in the course of the project if my partner Mr. Thrimawithana decides to use some other techniques for his electronics which might need a different number of control signals. Therefore some redundant pins have been accounted for, which might or might not be used.

5.0 Progress To-date and Timeline for Completion of Project

From the controller's perspective I've managed to do some basic switching using an Atmel Mega8 that was available in the ECE store. A single capacitor was used in the experiment with a switch on either side. One switch was connected to a DC power supply and the other was connected to a resistive load. Capacitor voltage was continuously monitored and each time the voltage dropped to less than 3V, a switch on the supply side was turned on to charge the capacitor. After the terminal voltage reached 5V, it was disconnected from the power supply and the other switch turned on to connect it to the load. Voltage waveforms on the oscilloscope revealed that the switching was working as expected. Other control aspects discussed in above sections are yet to be implemented.

A Gantt chart showing the main breakdown of tasks and approximate time durations for completion is given below.

	Task Name	Duration	Start	Finish	Predec
1	Understanding project concepts and breakdown of	4 days	Wed 3/03/04	Mon 8/03/04	
2	**Research on possible implementation strategies**	**39 days**	**Tue 9/03/04**	**Sat 1/05/04**	**1**
3	Energy pump	22 days	Tue 9/03/04	Wed 7/04/04	
4	Charge holding device bank	24 days	Tue 9/03/04	Fri 9/04/04	
5	Inverter	21 days	Fri 26/03/04	Sun 25/04/04	
6	Battery and charging system	13 days	Wed 14/04/04	Sat 1/05/04	
7	Controller subsystem	38 days	Wed 10/03/04	Fri 30/04/04	
8	Simulations and preliminary experimental work	38 days	Wed 10/03/04	Fri 30/04/04	1
9	Writing the interim report	7 days	Sun 2/05/04	Sun 9/05/04	2
10	Exam Break	11 days	Sat 5/06/04	Sun 20/06/04	9
11	**Implementation and debugging**	**49 days**	**Mon 21/06/04**	**Sun 22/08/04**	**10**
12	Energy pump and control	9 days	Mon 21/06/04	Thu 1/07/04	
13	Charge holding device bank and control	47 days	Mon 21/06/04	Fri 20/08/04	
14	Inverter and control	38 days	Fri 2/07/04	Fri 20/08/04	12
15	Battery backup and control	2 days	Sat 21/08/04	Sun 22/08/04	14
16	Overall system implementation, debugging and control	5 days	Mon 23/08/04	Sun 29/08/04	11
17	Presentation and preparation	8 days	Mon 30/08/04	Wed 8/09/04	16
18	Demonstation and preparation	4 days	Sun 12/09/04	Wed 15/09/04	16
19	Writing final report	18 days	Sat 21/08/04	Sun 12/09/04	

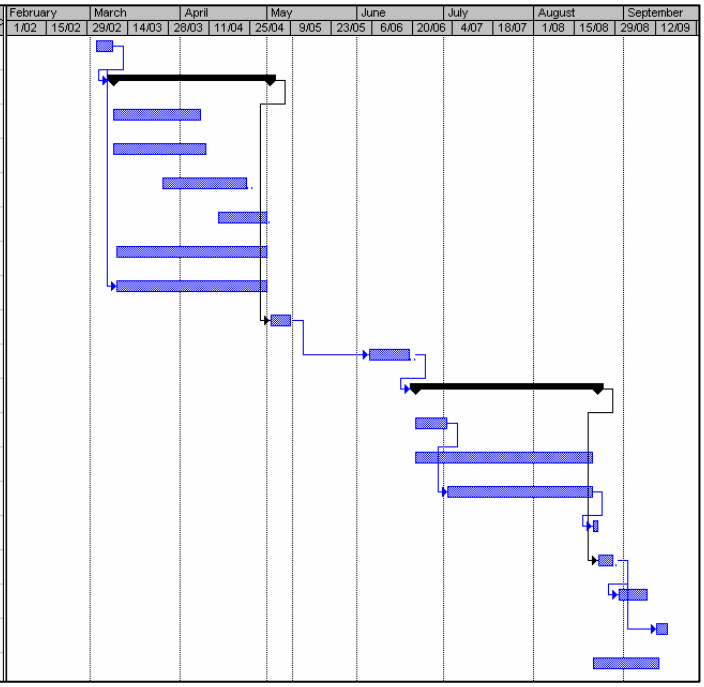

Figure 5.1: Schedule showing main tasks and approximate completion dates

As shown in the above figure the preliminary work has been successfully completed. My partner is aiming to complete the charging unit and the supercapacitor bank module by the end of June and then start working on the inverter. The inverter design is more complex and requires more time, hence we've decided to buy a commercially available inverter so that I can work on the control part for the whole system while the inverter is being finalised.

6.0 Conclusions

A novel concept for UPS system design has been introduced and thoroughly investigated. Supercapacitors have been chosen as the self contained energy storage elements which are used to transfer energy from the input to output while maintaining complete electrical isolation between supply and load. An Atmel Mega64 microcontroller is to provide the required control for the system to guarantee proper functionality at all times.

The first phase of the project has successfully been completed with many possibilities considered out of which the final solutions have been selected. In the next phase of the project, these selected methodologies will be implemented and the quality and standard of the final implementation compared against current systems and evaluated.

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Appendices

Appendix A: Extract from IEEE C62.41 Class B Standard

This Standard is quite lengthy and very informative hence cannot be summarised within a few pages. The only aim of this Appendix is to give a very brief outline of what a Class B surge is. Details and diagrams are from the IEEE C62.41 document [10]. Please refer to this for further details.

A surge to any location can be considered to be of Class A, B or C and a rough sketch of these locations is given in Figure A.1 below.

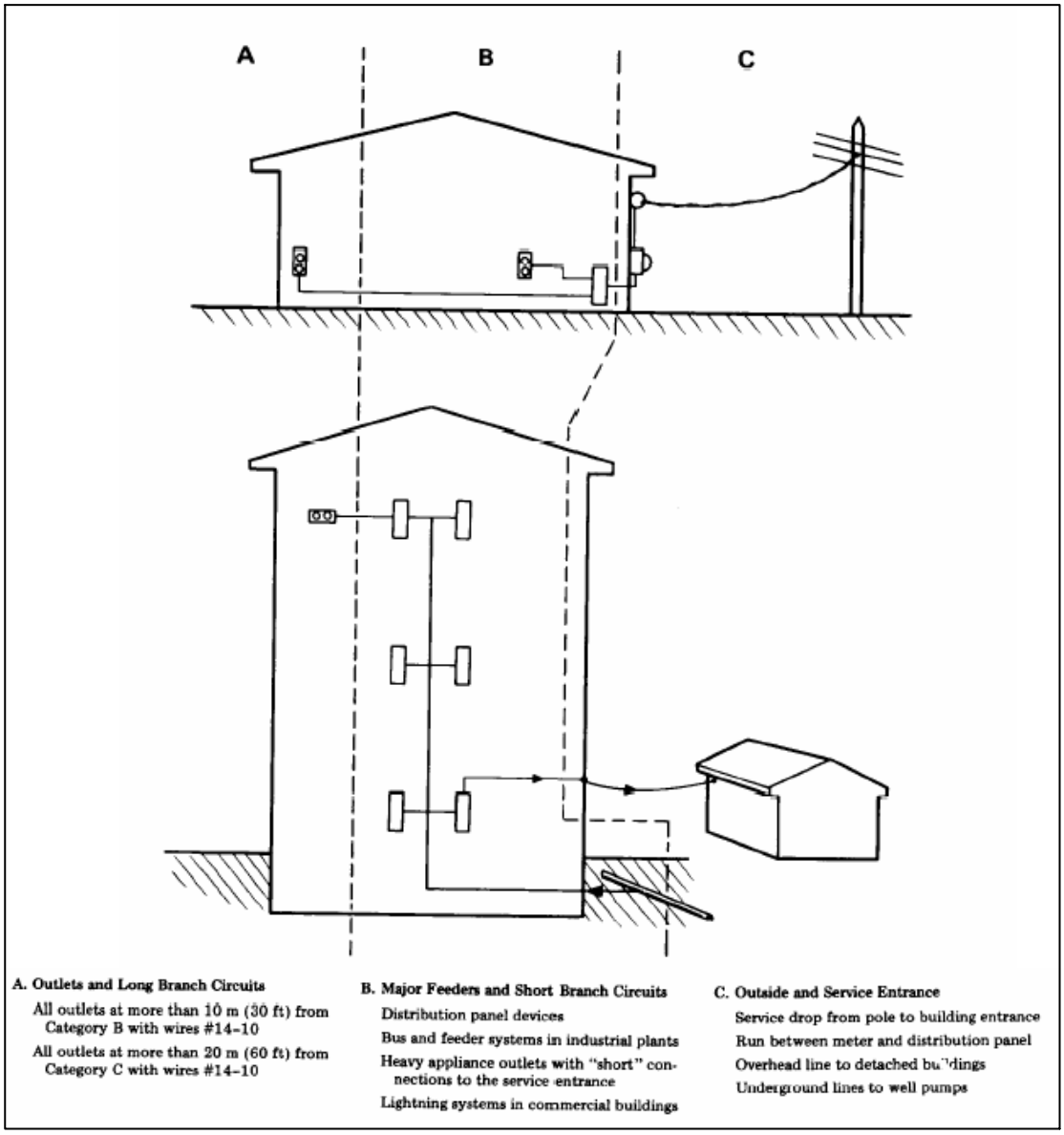

Figure A.1: Location Categories [10]

"The values in Table [A.1] represent the maximum range and correspond to the medium exposure situation of Figure [A.1 above]. For less exposed systems, or when the prospect of a failure is not highly objectionable, one could specify lower values of open-circuit voltages with corresponding reductions in the discharge currents.

The 6kV open-circuit voltage derives from two facts; the limiting action of wiring devices sparkover and the unattenuated propagation of voltages in unloaded systems. The 3kA discharge current in category B derives from experimental results, field experience in suppressor

performance and simulated lightning tests. The two levels of discharge currents for the 0.5 microsecond-100kHz wave derive from the increasing impedance expected in moving from location B to location A.

Location C is likely to be exposed to substantially higher voltages than location B because the limiting effect of sparkover is not available. The high-exposure rates of Table [A.1] could apply with voltage in excess of 10kV and discharge currents of 10kA or more. Installing unprotected load equipment in location C is not recommended; the installation of secondary arresters however can provide the necessary protection. Secondary arresters having 10kA ratings have been applied successfully for many years in location C" [10].

Location Category	Comparable to IEC No 664 Category	Impulse		Type of Specimen or Load Circuit	Energy (joules) Deposited in a Suppressor* with Clamping Voltage of	
		Waveform	Medium Exposure Amplitude		500V (120 V System)	1000V (240 V System)
A Long branch Circuits and outlets	II	0.5 μs-100 kHz	6 kV	High impedance†	—	—
			200 A	Low impedance‡, §	0.8	1.6
B Major feeders, short branch circuits, and load center	III	1.2 × 50 μs	6 kV	High impedance†	—	—
		8 × 20 μs	3 kA	Low impedance‡	40	80
		0.5 μs-100 kHz	6 kV	High impedance†	—	—
			500 A	Low impedance‡, §	2	4

*Other suppressors having different clamping voltages would receive different energy levels.
†For high-impedance test specimens or load circuits, the voltage shown represents the surge voltage. In making simulation tests, use that value for the open-circuit voltage of the test generator.
‡For low-impedance test specimens or load circuits, the current shown represents the discharge current of the surge (not the short-circuit current of the power system). In making simulation tests, use that current for the short-circuit current of the test generator.
§The maximum amplitude (200 or 500 A) is specified, but the exact waveform will be influenced by the load characteristics.

Table A.1: Surge voltages and currents at standard locations [10]

Appendix B: Control Required for the Overall System

1. Control for a supercapacitor bank

Figure 4.2 in Section 4.1.2 shows the architecture of an individual supercapaitor bank. The required control signals are as follows and use the states shown in Figure 4.3 in Section 4.1.4.

Q1_cntrl	Relay_cntrl	Q2_cntrl	Operating mode of supercapacitor bank
0	1	0	Turn relay on and prepare bank to charge (used to reduce mechanical stress on the relay)
1	1	0	Bank in charging mode
0	0	0	Bank fully charged, move it to stand-by or move to charging queue if previous state was *discharging*
0	0	1	Bank in discharging mode

Table B.1: Control for a supercapacitor bank

Q2_cntrl actually has 2 lines, where a *high* level on either line will turn on the corresponding switch as shown in Figure 4.4 on Page 10 of Mr. Thrimawithana's report.

2. Control for the supercapacitor charging unit

The energy pump or charger has been implemented using the following architecture (refer to Mr. Thrimawithana's report for details of this design).

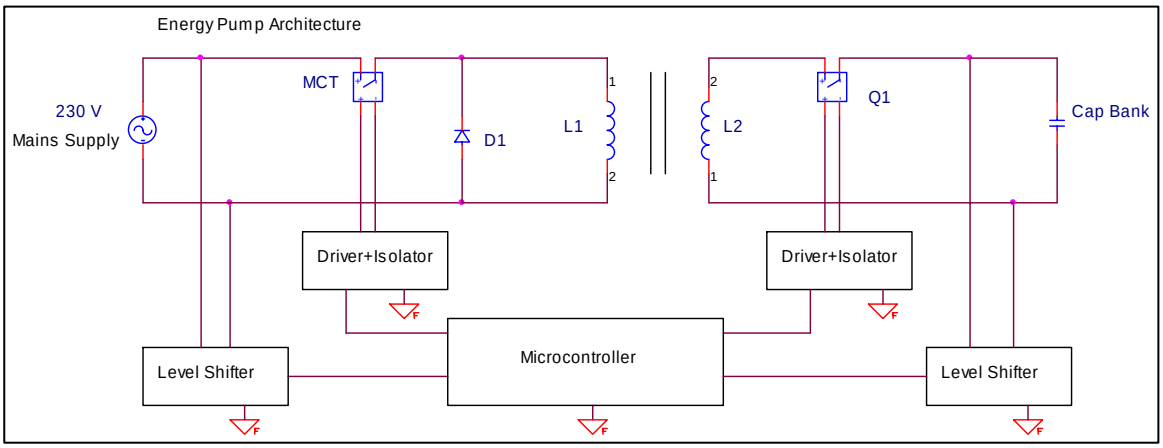

Figure B.2: Control for charging unit

Only one control signal is required by the charger which will be used to control the state of the MOS Control Thyristor (MCT). If the input is in the positive half of the cycle and the supercapacitor bank voltage is greater than the minimum threshold 12V, a *high (or 5V)* repetitive signal of 5kHz will be sent to turn the MCT on. A *low (or 0V)* signal will be sent at all other times including when there's no bank in *charging* mode.

3. Control for the battery charging unit

This will have only one control signal which will be used to power up this unit using power from the charged supercapacitor banks and then recharge the battery backup.

4. Control for the inverter

As designed by Mr. Thrimawithana, the inverter design to be used is

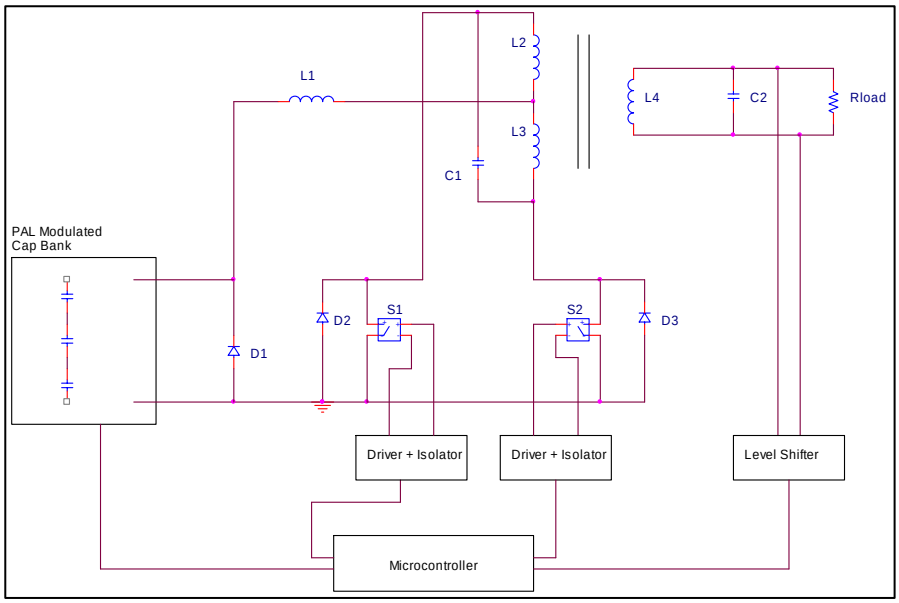

Figure B.3: Circuit diagram for the inverter

The microcontroller will provide two control signals to control switches S1 and S2 based on the bank voltage and the output voltage. When the discharging bank is in the first half of the cycle, S1 will be turned on and then S2 will be turned on for the rest of the cycle. Apart from these signals, one more signal will be used to choose the power source for the inverter. For example under normal conditions energy will be from the supercapacitor banks whereas during blackouts this will be via the battery backup.

Such are control signals for the overall system. Let's summarise to determine the total number of I/O lines required.

Purpose	Input and Outputs
Monitor line voltages	1 A/D input 4-8 inputs from the ladder circuitry
Monitor bank voltage	1 A/D pin for each bank x number of banks = 5 (assuming 5 banks)
Battery health	1 A/D pin
Monitor output	1 A/D pin
Control for banks	4 output pins for each bank x number of banks = 20 (assuming 5 banks)
Control for supercapacitor charger	1 pin
Control for battery charger	1 pin
Control for inverter	3 pins
Total I/O lines required	***Around 40***

Table B.1: Total I/Os required by the microcontroller

Appendix C: Selection Process for a Suitable Microcontroller

As shown in Table B.1, we need a total of approximately 40 I/O lines. This requirement was given the highest priority in the selection process. Apart from this, the following were considered:

- 16MHz or higher to provide fast processing
- Need a simple 8-bit controller since we haven't got much data movement
- A UART to interface with a PC (this will be done only if time-permits but still needs to be accounted for)
- At least 4 (say 6 to account for possible future needs) A/D channels
- A good sampling rate. Theoretically we need to sample only at a minimum of 100Hz but this will not be sufficient when monitoring the actual bank voltages etc.
- Will need approximately 16kB flash memory. Better to have more to be on the safe side though.
- Intend to use a 5V microcontroller since this will be easy on most of the electronics which will be operated on 5V.
- Will need around 1kB of SRAM for variables and other storage.
- Need at least 4 external interrupts to capture a surge, indicated by the circuitry of the ladder block in Figure 4.1.
- Need around 3 timers to detect the duration of a surge and also for other timeouts (for example to detect a bank taking too long to charge, due to a fault).
- Watchdog timer to monitor the system and recover if something goes wrong.
- Use minimum power as possible

The following microcontroller's were selected based merely on the number I/O lines, clock frequency, A/D channels and availability:
Atmel: ATmega128, ATmega64, ATmega169
Microchip: PIC18F6680, PIC18F6490
Motorola: MC9S08GB32, MC9S08GB60

Shown in Table C.1 is a brief comparison between these devices.

Microcontroller	Clock Frequency (MHz)	I/O pins	External Interrupts	A/D channels[i]	Flash (kB)	V_{cc}(V)	SRAM (bytes)	Serial Interface	Timers[ii]
ATmega128	16	53	8	8	128	5	4096	UART, SPI	4
ATmega64	16	53	8	8	64	5	4096	UART, SPI	4
ATmega169	16	54	17	8	16	5	1024	UART, SPI	3
PIC18F6680	40	52	4	12	64	5	3072	UART	4
PIC18F6520	40	52	4	12	32	4.5	2048	UART	5
MC9S08GB32	20	56	1	8	32	3.6	2048	SPI, SCI	5
MC9S08GB60	20	56	1	8	60	3.6	4096	SPI,SCI	5

Table C.1: Comparison between some microcontrollers [data from 11,12,13]

Based on the above data, the Atmel ATmega64 can be considered the most suitable due to the following reasons:
The PIC microcontrollers have the required I/O pins and other characteristics, but these ones are not readily available in the ECE store. Also development boards for them are quite expensive. The Motorola ones were ruled out since they operate under low voltages. However all the Atmel chips meet all the project requirements and are available in the ECE store along with the STK development boards, hence were preferred. Although it is estimated that approximately 16kB of flash would be required, the mega64 chip was chosen as the final controller in order to account for a safety margin.

[i] Total of all A/D channels. For example if a device has 6 8-bit channels and 8 10-bit channels, this number will show 14.
[ii] Total of all timers. For example if a device has 6 8-bit timers and 8 16-bit timers, this number will show 14.