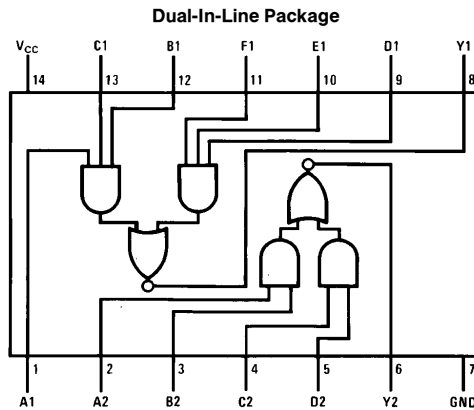


54LS51/DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function. Each package contains one 2-wide 2-input and one 2-wide 3-input AND-OR-INVERT gates.

Connection Diagram



TL/F/6369-1

Order Number 54LS51DMQB, 54LS51FMQB,
54LS51LMQB, DM74LS51M or DM74LS51N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y1 = \overline{(A1)(B1)(C1)} + (D1)(E1)(F1)$$

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Other Combinations						H

$$Y2 = \overline{((A2)(B2) + (C2)(D2))}$$

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	L
X	X	H	H	L
Other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	–55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS51			DM74LS51			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			–0.4			–0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	–55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –18 mA			–1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	54LS 2.5			V
			DM74 2.7	3.4		
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	54LS DM74		0.4 0.35 0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 10V (54LS)			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V	54LS DM74		–0.40 –0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	54LS DM74	–20 –20	–100 –100	
I _{CCH}	Supply Current with Outputs High	V _{CC} = Max		0.8	1.6	mA
I _{CCL}	Supply Current with Outputs Low	V _{CC} = Max		1.4	2.8	mA

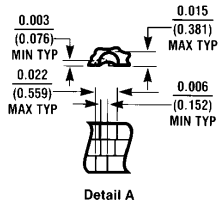
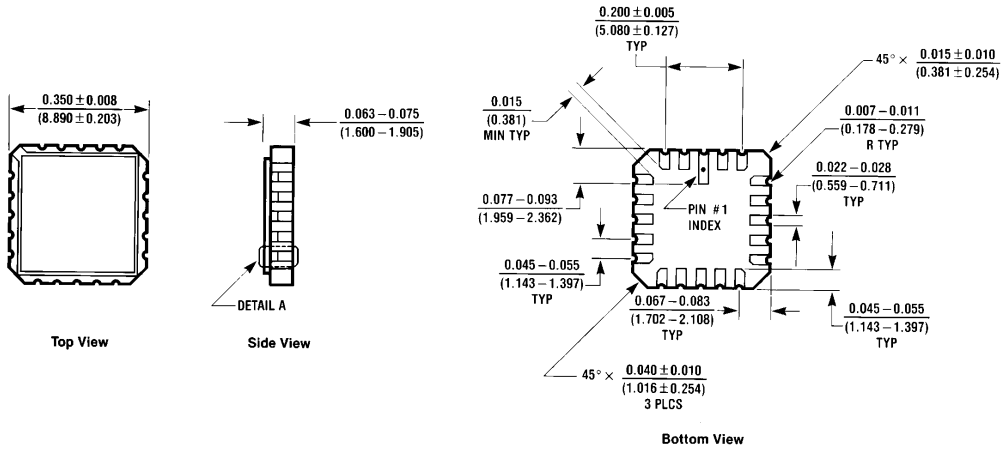
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

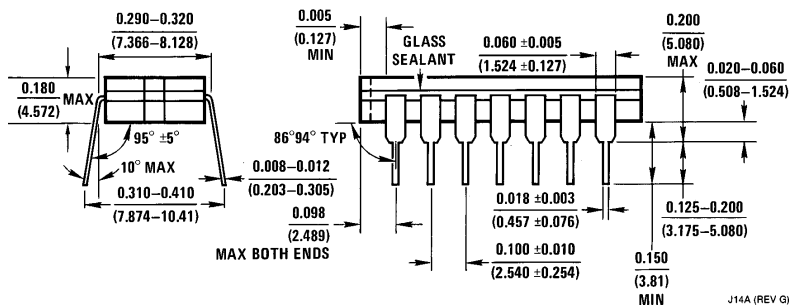
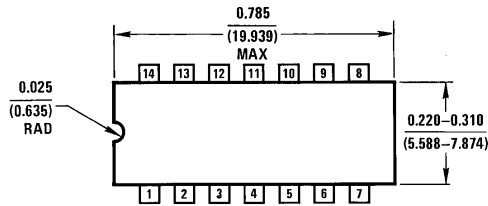
Symbol	Parameter	54LS51		DM74LS51		Units
		$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$		$C_L = 50 \text{ pF}, R_L = 2 \text{ k}\Omega$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		20	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	3	15	ns

Physical Dimensions inches (millimeters)



Ceramic Leadless Chip Carrier Package (E)
 Order Number 54LS51LMQB
 NS Package Number E20A

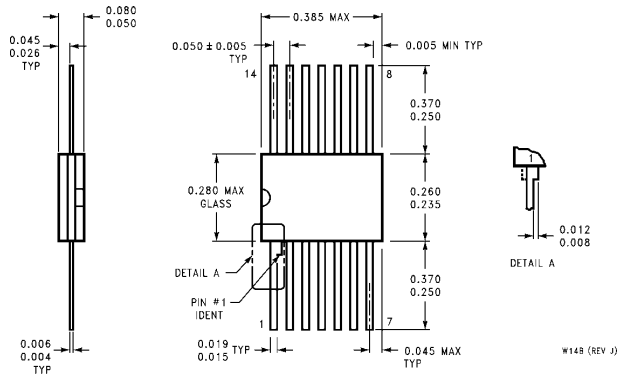
E20A (REV D)



Ceramic Dual-In-Line Package (J)
 Order Number 54LS51DMQB
 NS Package Number J14A

J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS51FMQB
NS Package Number W14B

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