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Enhanced mobility in 100 nm strained SiGe vertical P-MOSFETs fabricated by UHVCVD

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ABSTRACT

Strained SiGe vertical PMOSFETs with a channel length of 100 nm have been fabricated without sophisticated lithography and the whole process is compatible with a regular CMOS process. The source, channel and drain layers with *in situ* doping were grown by ultrahigh vacuum chemical vapor deposition (UHVCVD) at 500 ^{o}C. Atomic force microscopy (AFM) of the SiGe and silicon sample surfaces shows the RMS roughness to be 0.18 nm. X-ray diffraction (XRD) rocking curves of the Si (004) plane demonstrate that the SiGe layers do result in compressive strain. The drive current for the vertical SiGe PMOSFET was enhanced by as much as 80% as compared with the silicon control device, in both the forward and reverse modes of operation.

INTRODUCTION

In order to improve the packing density and device performance in ultra-large scale integrated (ULSI) circuits, MOSFETs have been scaled down successfully over the past few decades. However, the enhancement in drive current faces challenges such as lithography, channel doping fluctuation and short channel effects as the transistor sizes are scaled down [1]. Recently, strained silicon-germanium MOSFETs are receiving considerable attention due to the enhancement of in-plane hole mobility, as well as out-of-plane electron and hole mobilities over conventional silicon MOSFETs [2]. It has been predicted that the compressive strain in the SiGe layer splits the light and heavy hole subbands and improves the hole mobility in both out-of-plane and in-plane directions [3]. So both high performance SiGe planar [4] and vertical PMOSFETs [5] have been fabricated. In the present work, strained SiGe vertical PMOSFETs with a channel length of 100 nm were fabricated by UHVCVD. Hole mobility enhancement in the out-of-plane direction has been demonstrated. The device combines the advantages of a very short channel device without a critical lithography process and higher hole mobility in the channel.

DEVICE FABRICATION

Fig. 1 shows the process flow for the SiGe vertical PMOSFETs. The starting substrate was a <100> Si 100-mm diameter 0.008-0.02 Ω-cm p-type wafer. The source, channel and drain layers were grown by ultrahigh vacuum chemical vapor deposition (UHVCVD) at 500 ^{o}C using Si_2H_6 and GeH_4. PH_3 and B_2H_6 were used for *in situ* doping. Subsequently, a reactive ion etch (RIE) process with HBr and Cl_2 was used to define the mesa of the vertical MOSFET. A 10 nm

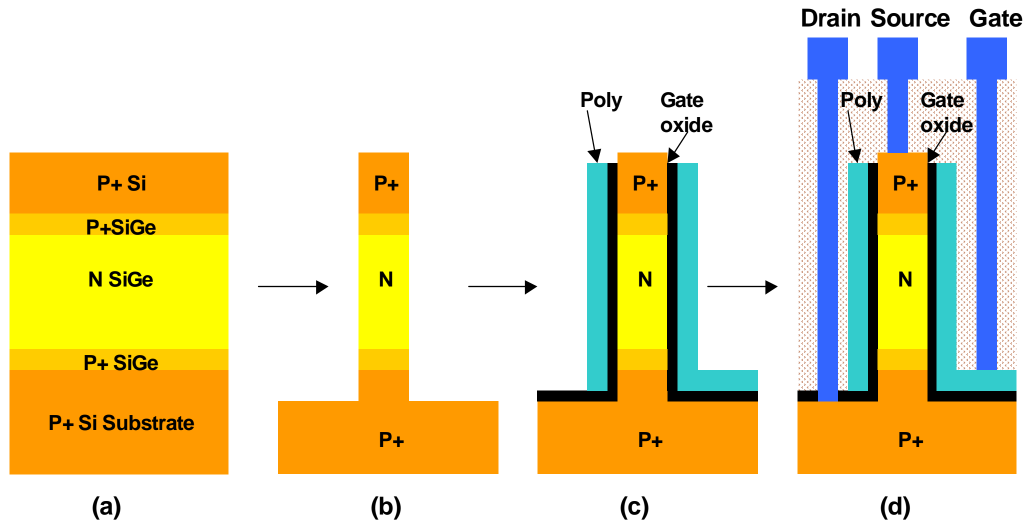

Figure 1. Process flow of the vertical SiGe PMOSFET: (a) UHVCVD growth; (b) RIE mesa etch; (c) Gate oxide growth and polysilicon gate deposition and patterning; (d) Isolation oxide deposition, contact hole etch and metal patterning.

silicon cap layer was grown by UHVCVD before growing a 40Å gate oxide by wet oxidation at 750 ^{o}C for 5 minutes. This was followed by 1000Å polysilicon deposition for gate electrode formation. The polysilicon gate was doped by BF_2 ion-implantation at 15 keV with a dose of $2x10^{15}$ cm^{-2}, which was then activated by a rapid thermal anneal at 950 ^{o}C for 1 minute.

The rest of the process was a more or less standard MOS process, including low temperature oxide (LTO) deposition for isolation and contact hole etching, metal deposition and patterning, followed by a forming gas anneal. The final device structure is shown in Fig. 1 (d). The gate oxide surrounds the mesa, and the channel region is formed on the sidewalls of the mesa.

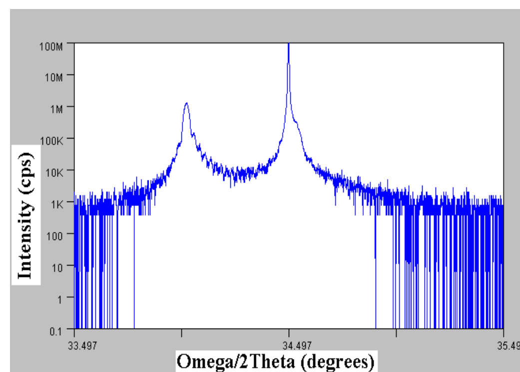

Figure 2. XRD data for SiGe strained layers.

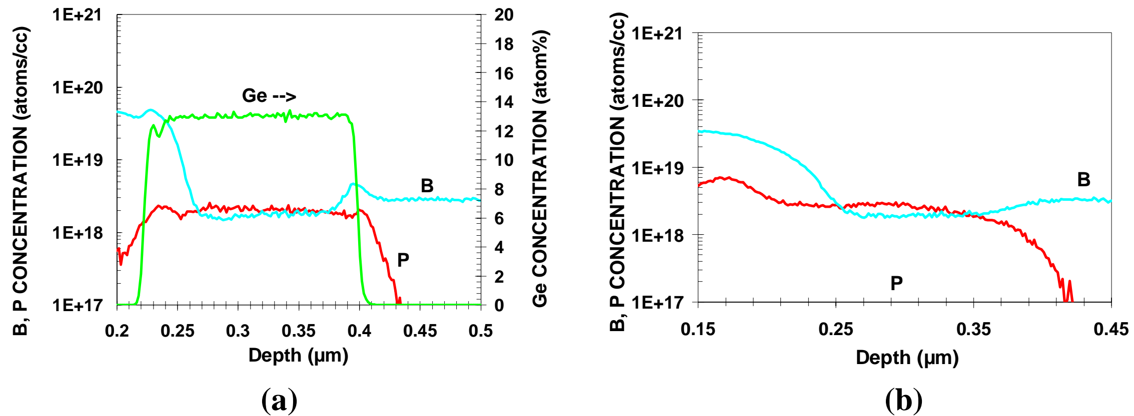

Figure 3. SIMS profile along the vertical channel of the (a) SiGe and (b) Si control PMOSFETs.

RESULTS AND DISCUSSION

X-Ray Diffraction (XRD) rocking curves of the Si (004) peak was studied (Fig. 2). The secondary peak to the left of the Si (004) peak demonstrates that the SiGe layers do result in compressive strain. The channel length is 100nm, and the Ge concentration is about 14% and uniform throughout the device, as determined by Secondary Ion Mass Spectroscopy (SIMS) and shown in Fig. 3. Atomic force microscopy (AFM) of the SiGe and Si sample surfaces (Fig. 4) shows the RMS roughness to be 0.18 nm.

Fig. 5 (a) shows the subthreshold characteristics for the SiGe and Si control PMOSFETs. The threshold voltage, V_T, for the Si device is –0.7V whereas that for the SiGe device is about 0.3V. The Si device shows very good turn-on and turn-off characteristics.

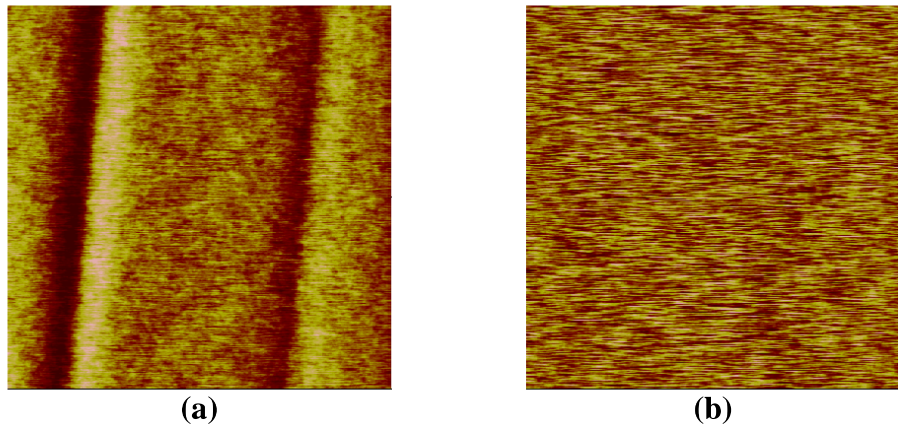

Figure 4.: AFM images of the (a) SiGe and (b) Si sample surfaces. Both have an RMS surface roughness of 0.18 nm.

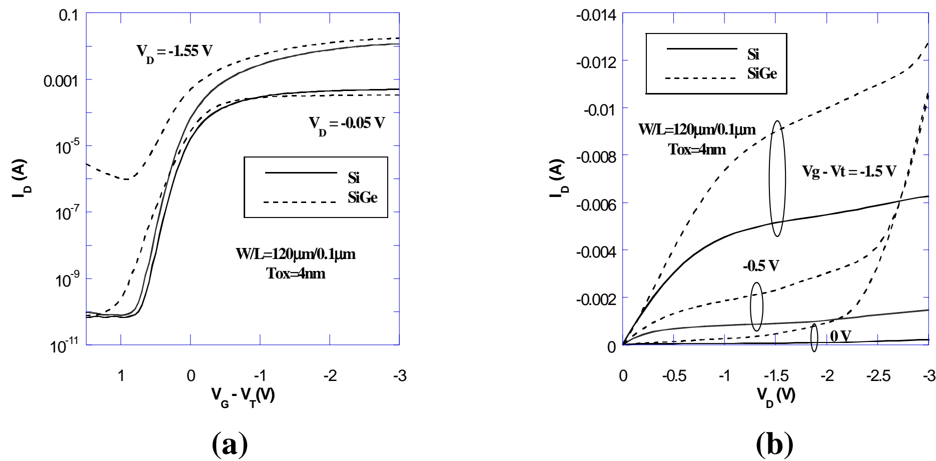

Figure 5. (a) Subthreshold characteristics and (b) Output characteristics of the SiGe and Si control PMOSFETs.

The leakage current at V_D = -1.55V and the Drain Induced Barrier Lowering (DIBL) for the SiGe device are both much larger than that for the Si device, since SiGe has a lower bandgap than that of Si. The sub-threshold slopes of the silicon and silicon-germanium devices were 105 and 180 mV/decade, respectively. The output characteristics are shown in Fig. 5 (b). The drive current for the SiGe PMOSFET is higher than the Si device, and this improvement is attributed to the out-of-plane hole mobility enhancement in SiGe. At V_G - V_T = V_D = -1.5V, the drive current for the SiGe PMOSFET is 90 mA/μm^2 compared to 50 mA/μm^2 for the Si control device, indicating an 80% improvement.

CONCLUSIONS

We have fabricated the first strained SiGe vertical MOSFETs with a uniform Ge profile by UHVCVD. The drive current for the 100nm SiGe PMOSFETs are enhanced by about 80% as compared to the Si control device. Since the improvement in the performance of PMOSFETs are more important for CMOS devices, SiGe devices are potential candidates for CMOS. The leakage current and DIBL are however degraded due to the smaller bandgap of SiGe.

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