Hole and Electron Mobility Enhancement in Strained SiGe Vertical MOSFETs

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***Abstract*—We have fabricated strained SiGe vertical P-channel and N-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) by Ge ion implantation and solid phase epitaxy. No Si cap is needed in this process because Ge is implanted after gate oxide growth. The vertical MOSFETs are fabricated with a channel length below 0.2 μm without sophisticated lithography and the whole process is compatible with a regular CMOS process. The enhancement for the hole and electron mobilities in the direction *normal* to the growth plane of strained SiGe over that of bulk Si has been demonstrated in this vertical MOSFET device structure for the first time. The drain current for the vertical SiGe PMOSFETs has been found to be enhanced by as much as 100% over the Si control devices and the drain current for the vertical SiGe NMOSFETs has been enhanced by 50% compared with the Si control devices on the same wafer. The electron mobility enhancement in the normal direction is not as significant as that for holes, which is in agreement with theoretical predictions.**

***Index Terms*—Bandgap engineering, electron and hole mobility enhancement, vertical MOSFET.**

I. INTRODUCTION

ULTRA-LARGE-SCALE integrated (ULSI) MOSFET devices have been scaled down successfully over several decades with higher package density and better device performance. However, when the transistor size is below 100 nm, a lot of challenges are encountered, such as lithography, channel doping fluctuation, and short channel effects [1], [2]. The drive current of the devices cannot be improved much more as the transistor size is scaled down. One possible solution to the above challenge is to take advantage of bandgap engineering. Strained SiGe has attracted much attention recently because of the hole mobility enhancement in this material and because it is compatible with current Si technology [3]–[10]. Strained planar SiGe PMOSFETs have been fabricated and show performance improvement compared with Si devices [11], [12]. It has been predicted that the compressive strain in the SiGe layer splits the light and heavy hole subbands and improves the hole mobility in both out-of-plane and in-plane directions [13], [14]. In addition, strain in SiGe also splits the six-fold degeneracy of the conduction band valleys. The four-fold in-plane valleys are lowered below the two-fold out-of-plane valleys [15]. Therefore, there is a greater proportion of the carriers in the four-fold valleys which have a lower out-of-plane mass. The electron mobility is direction dependent, and it increases in the out-of-plane direction and decreases in the in-plane direction. So, to improve the electron mobility in planar MOSFETs, tensile-strained Si has to be used which has demonstrated higher electron and hole mobility for both N-channel and P-channel MOSFETs [16], [17]. But it is hard to grow a high quality relaxed SiGe buffer layer on which tensile strained Si can be grown. In vertical MOSFETs, carriers flow in the out-of-plane direction, so both the electron and hole mobilities are improved in compressively strained SiGe films. With vertical MOSFETs, the channel length is not limited by lithography and we have much more freedom in terms of bandgap engineering [18]–[20]. In this paper, we report the fabrication of the strained SiGe vertical NMOSFETs and PMOSFETs by Ge ion implantation and solid phase epitaxy (SPE). Electron and hole mobility enhancement in the out-of-plane direction has been demonstrated. The device structure combines the advantages of a very short channel device without a critical lithography process and higher electron and hole mobility in the channel.

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II. ELECTRONIC PROPERTIES OF STRAINED SIGE

The biaxial compressive strain in SiGe lifts the degeneracy between heavy and light hole bands, and the spin-orbit split-off band is moved further down in energy (Fig. 1). The heavy hole sub-band moves up and light hole sub-band moves down. This results in reduced inter-band scattering and improved hole mobility in both the in-plane and out-of-plane directions [14], [15]. The effective mass of the heavy hole is reduced and the effective mass of the light hole is increased, which also results in the enhancement of the hole mobility. For the conduction band, The X valleys split into lower fourfold degenerate states and higher twofold states (Fig. 2). In the in-plane direction, the heavy longitudinal electron mass $(0.92m_0)$ leads to lower electron mobility in the plane of growth. In the out-of-plane direction, on the other hand, the effective mass of the electrons is reduced and a higher electron mobility is expected. If we consider alloy scattering, at low doping, the out-of-plane electron mobility in strained SiGe is also lower than that in Si. At higher doping levels, where ionized impurity scattering is expected to dominate, the out-of-plane electron mobility in strained SiGe is expected to exhibit an enhancement [5].

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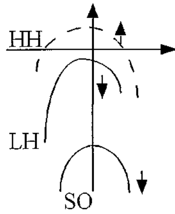


Fig. 1. Valence band splitting in compressively strained SiGe.

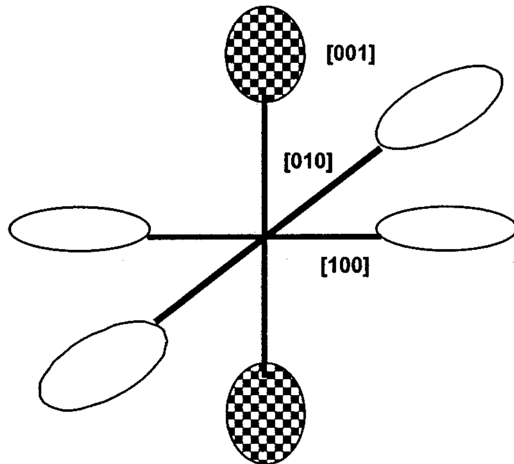


Fig. 2. Constant energy surfaces, $E(k)$ and splitting of the six-fold degeneracy of the conduction band in compressively strained SiGe. The shaded valleys are at a higher energy.

III. Device Fabrication

Fig. 3 shows the process flow for the SiGe vertical MOSFETs. Except for the channel and source/drain doping, the process flow is the same for the NMOSFETs and PMOSFETs. The starting substrates were $\langle 100 \rangle$ Si 100 mm diameter 8–12 Ω-cm p-type (NMOSFETs) and 3–5 Ω-cm n-type (PMOSFETs) wafers. Subsequently, 500 Å low temperature oxide (LTO) was grown for reactive ion etching (RIE) mask. An RIE process with HBr and Cl_2 was employed to etch the mesa region for the vertical channel. The size of the mesa is 40 μm $\times$ 40 μm. The height of the mesa is 250 nm. After RIE, a Si polishing etch and a sacrificial oxide were used to remove the RIE-induced damage. A low-temperature oxide (LTO) was then deposited for isolation. This was followed by 10 nm rapid thermal oxidation (RTO) for gate oxide growth and polysilicon deposition. An anisotropic etch was used to form a self-aligned side-wall polysilicon gate. Germanium at 200 keV, 7×10^{16} cm^{-2}, was implanted into the central 60 mm diameter of the wafer; the remaining unimplanted area was used for the fabrication of control Si devices on the same wafer. This minimized the possibility of channel length and thermal budget variations in Si and SiGe layer devices from wafer-to-wafer in a single wafer RIE and RTO process. The peak value of Ge mole fraction was 15% at a depth of 1500 Å below the surface. The solid phase epitaxy (SPE) of the SiGe films was done by furnace annealing at 590 °C for 60 min. Channel and source/drain implantation was done after that. For PMOSFETs, a two-stage P implantation, 150 keV, 5×10^{13} cm^{-2} and 200 keV, 7×10^{13} cm^{-2}, was used for channel doping and a low energy (10 keV) BF_2 implant was used to form the S/D region. For NMOSFETs, a two-stage B implantation, 55 keV, 5×10^{13} and 85 keV, 7×10^{13} cm^{-2}, was used for channel doping and a low energy (15 keV) As implant was used to form the S/D region. The rest of the process was a standard MOS process, based on low temperature oxide (LTO) deposition for isolation and contact hole etching, metal deposition and patterning, followed by a forming gas anneal. Al was used for the metal contact and no silicide was used in this process. Because Ge was implanted after gate oxide growth, no Si cap is needed for the gate oxidation.

The final device structure is shown in Fig. 3(d). The gate electrode surrounds the pillar, and the channel region is formed on the sidewalls of the pillar. The channel width for the devices is 160 μm. The sidewall has a (110) surface orientation, which has higher interface states [21], and it can degrade the subthreshold swing and device performance. To change the surface orientation of the sidewall from (110) to (100), the wafer has to be rotated 45 °. With this device structure, the channel length is determined by the mesa height, source/drain and channel implantation and is independent on the lithography. The channel length is below 0.2 μm, as confirmed by the secondary ion mass spectroscopy (SIMS) results and the height of the mesa. Unlike a conventional planar MOSFET, the two source/drain junctions at the top and bottom of the mesa are different. The top drain junction is very deep and the source junction depth at the bottom depends on the diffusion of the dopant in the mesa region. The deep drain junction can degrade the short channel performance of the devices. To suppress the short channel effects, a fully depleted vertical MOSFET [22], which has thin pillar, or a heterojunction MOSFET structure [23] can be used.

IV. Material Characterization

Using Ge implantation to form the channel region, the main concern is whether such a high dose Ge-implanted channel would exhibit good crystal quality or not after SPE. We examined the crystal quality of Ge-implanted Si by X-ray diffraction (XRD), Rutherford backscattering (RBS), and transmission electron microscopy (TEM).

First of all, the crystalline quality for the strained SiGe layer grown by SPE was studied by high-resolution double crystal XRD (Fig. 4). Normally, the out-of-plane epilayer lattice constant is determined by a shift from the Si (400) substrate peak of the X-ray rocking curve. For a graded SiGe layer formed by Ge implantation, the out-of-plane lattice constant varies continuously with graded Ge mole fraction. Therefore, a broad epilayer peak was observed to the left of substrate peak, corresponding to the graded SiGe layer. The peak Ge concentration is 15% and 150 nm below the surface, which is determined by SIMS, as shown in Fig. 5. Fig. 6 shows the results of an RBS measurement that was carried out to investigate the crystal quality. The low channeling yield indicates that almost all of the implanted Ge atoms are located at substitutional sites after annealing. A cross-sectional TEM micrograph revealed that the Ge-implanted SiGe film was epitaxially regrown after thermal annealing. The quality of the gate oxide after Ge implantation has also been investigated by low and high frequency capaci-

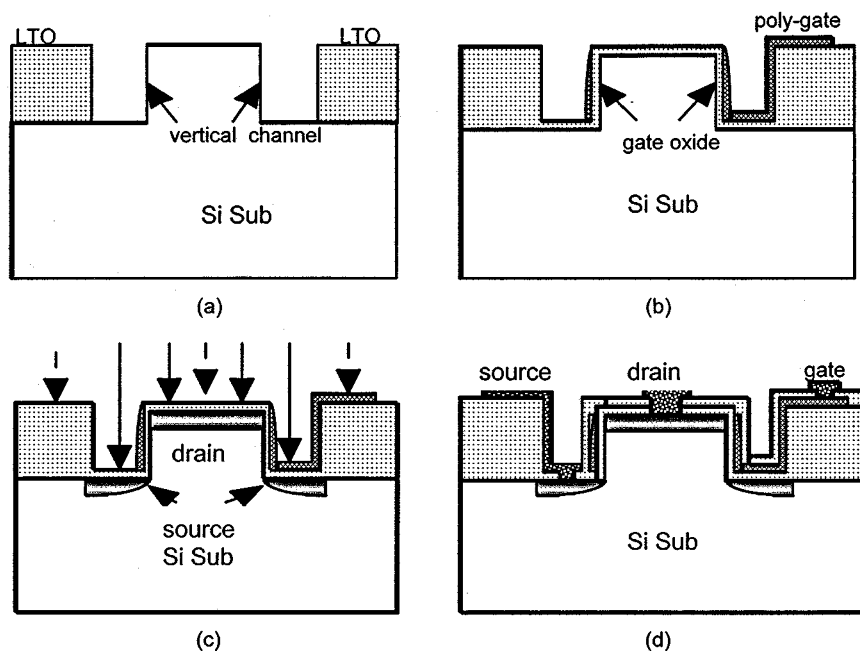


Fig. 3. Process flow of the vertical SiGe MOS transistor and structure: (a) RIE pillar etch, sacrificial oxide grow and removal, isolation oxide deposition and patterning; (b) growth of gate oxide and poly gate, self-aligned side-wall polysilicon gate formation; (c) channel, Ge, and S/D implantation; and (d) isolation oxide deposition, contact hole etch and metal patterning.

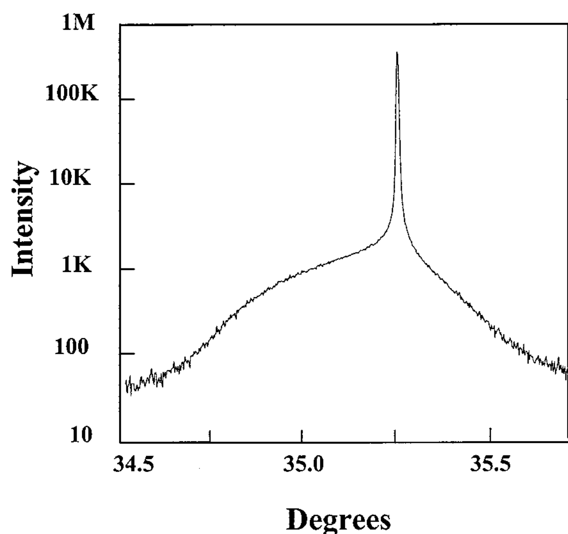


Fig. 4. XRD data for graded SiGe strained layers.

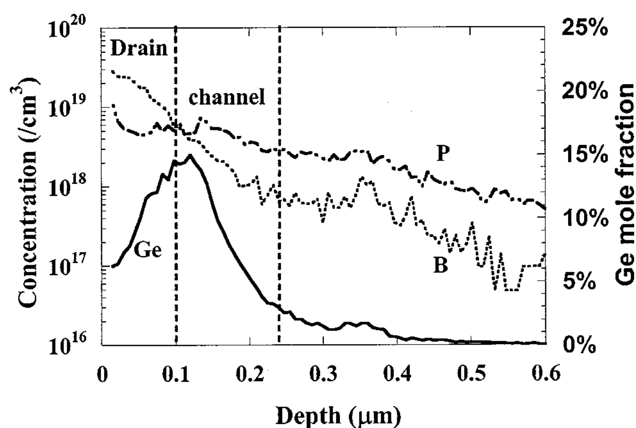


Fig. 5. SIMS profiles along the vertical channel of the PMOSFET.

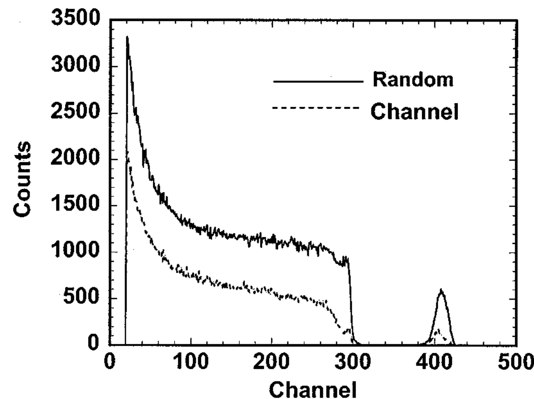


Fig. 6. Random and channeling RBS of the strained SiGe sample after annealing.

tance measurement. The repeatable measurement of quasistatic C–V indicates high quality of the gate oxide (Fig. 7).

V. Electrical Characterization

Due to the thick gate oxide and unoptimized channel doping, the threshold voltage and subthreshold swing are high for all of the devices. Due to the hole and electron mobility enhancement in the vertical direction, both SiGe channel PMOSFETs and NMOSFETs show higher drive current than the Si control devices.

A. PMOSFETs

Fig. 8 shows the I_D–V_D characteristics of 0.2 μm length vertical PMOSFETs using Si and SiGe channels. The channel length is determined by the SIMS profile and the height of the mesa. The devices show good saturation and turn-off

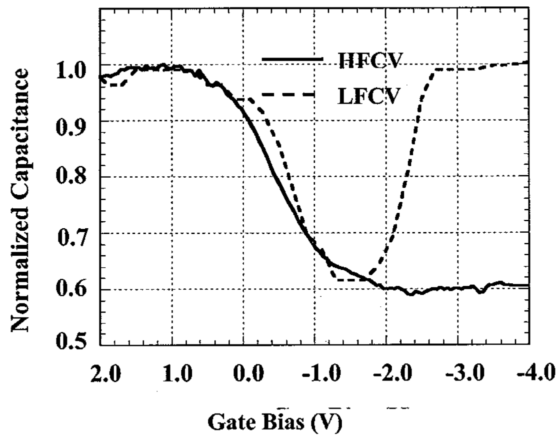


Fig. 7. High- and low-frequency C–V characteristics of vertical SiGe MOS capacitor.

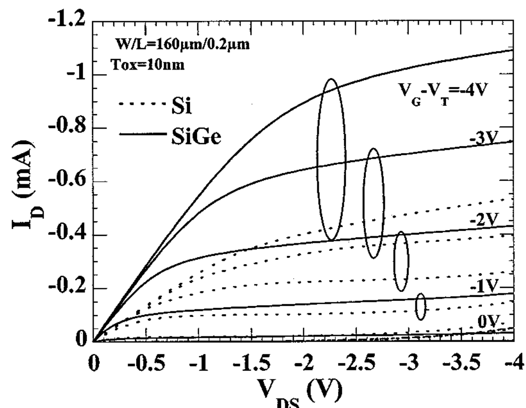


Fig. 8. Output characteristics of the graded SiGe vertical PMOSFETs and Si control device.

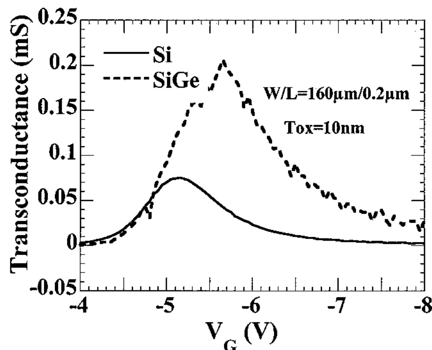


Fig. 9. Linear transconductance comparison of the graded SiGe vertical PMOSFETs and Si control device.

characteristics. As seen from the I_D–V_D behavior, the drain currents obtained for the SiGe channel PMOSFET are almost 100% higher than those for the Si control devices fabricated on the same wafer. Threshold voltage of both the devices is quite high because of unoptimized channel doping and thick gate oxide. The enhancement in drive current in SiGe is attributed to the effect of higher hole mobility in SiGe.

The channel mobility of holes could not be extracted from the device structure because there is only one channel length on the wafer. The transconductance in the linear region as a function of gate bias is shown in Fig. 9. The linear peak transconductance of the SiGe PMOSFETs was found to be 200 μS compared to

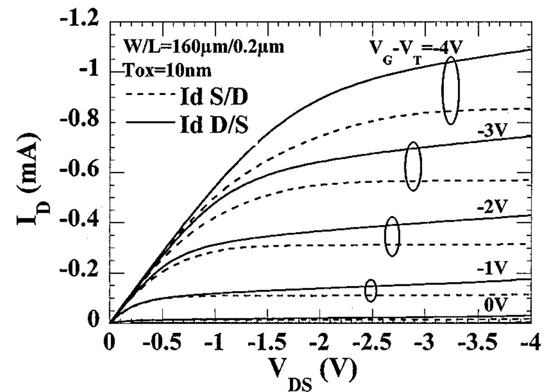


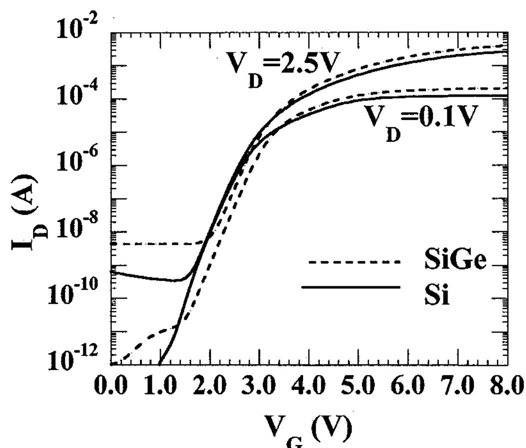
Fig. 10. Output characteristics of the graded SiGe vertical PMOSFETs with source contact on bottom and drain contact on top (solid line) and in reverse mode (dashed line).

75 μS for the control Si PMOSFETs. This is evidence of an enhancement in the out-of-plane hole mobility in the strained SiGe layer. The transconductance values in our devices are limited by the high source and drain series resistance. Since the process condition for the SiGe channel device and Si control device is same and Ge mole fraction in the drain and source layer is very low, the difference of the source/drain series and contact resistance in the two devices can only attribute a little to the transconductance difference. To make it much more conceivable, a series of devices with different channel length are needed to extract the source/drain series and contact resistance and the hole mobility. At high transverse fields, the linear G_m of SiGe PMOSFETs is comparable to that of Si because G_m becomes surface-roughness-scattering limited.

Another feature of the device structure is that, due to the graded SiGe in the channel, there is built-in electric field in the channel. Could the built-in electric field help to improve the drive current? To clarify this question, first, the device was measured with the source and drain contact interchanged (reverse mode). Fig. 10 shows the I_D–V_D curves in the normal and reverse mode. There is a lower value of drive current in the reverse mode, which seems to verify that the built-in electric field could indeed improve the drive current. However, after extensive device simulation, it was found that while built-in electric field does enhance the drift current, it is negated by the reduced diffusion current in the saturation/linear condition. The drive current, which is the sum of the drift and diffusion current, is actually same (lower) in the normal mode compared to the reverse mode in the linear (saturation) region [24]. The experimentally observed asymmetry in Fig. 10 might be due to the asymmetric device structure in terms of source/drains. Similarly, graded SiGe channels will not improve NMOSFET device performance either.

B. NMSOFETs

At high channel doping, electron mobility could also be improved in the out-of-plane direction. Fig. 11(a) shows the subthreshold characteristics for the SiGe and Si control NMOSFETs. Both devices show good on–off characteristics. The drive current for the graded SiGe NMOSFET is higher than that of the Si control device due to the out-of-plane electron mobility enhancement. The off-state current for the graded SiGe device is



(a)

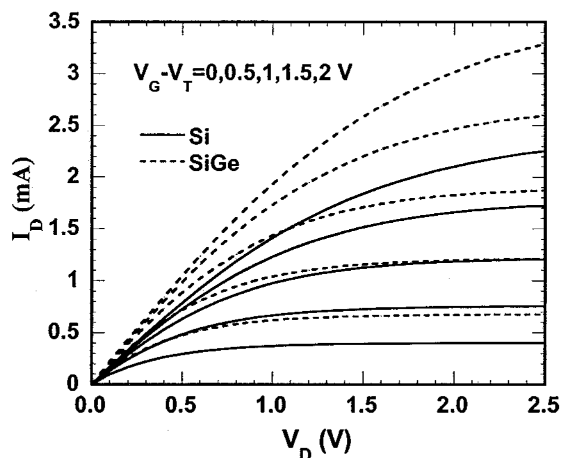
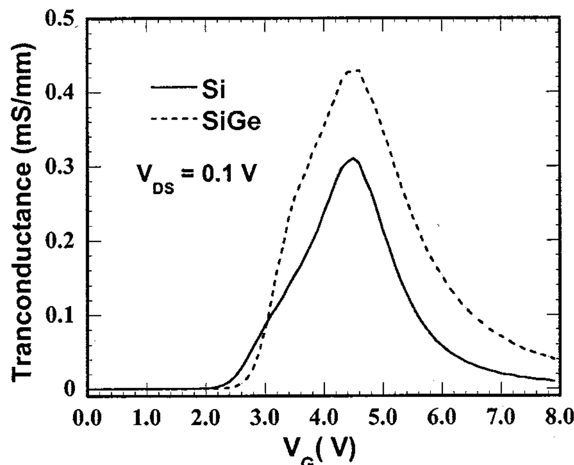
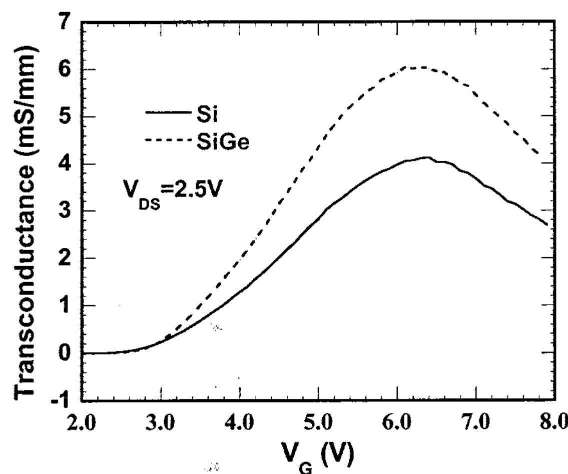


Fig. 11. (a) Subthreshold characteristics and (b) output characteristics of the graded SiGe NMOSFETs and Si control device.



(a)



(b)

Fig. 12. Linear transconductance comparison of the graded SiGe NMSOFETs and Si control device.

also increased. The graded SiGe NMOSFET has worse drain induced barrier lowering (DIBL). The V_T shift due to DIBL (for $V_{DS} = 2.5$ V) is 0.2 V for the SiGe device, which is due to the smaller band gap of the SiGe channel layer.

Fig. 11(b) shows the output characteristics for the devices. At $V_{DS} = V_G - V_T = 2$ V, the drive current for the graded SiGe NMOSFET is 50% higher than for the Si control device. In the graded SiGe PMOSFETs, we observed 100% enhancement of the drive current compared with the Si control device. So in the out-of-plane direction, the electron mobility enhancement for the strained SiGe layer is not as significant as the hole mobility enhancement, which is in agreement with Fischetti's theoretical calculation [5].

The transconductance in linear and saturation region for the strained SiGe vertical NMOSFETs is shown in Fig. 12. The linear peak transconductance for the graded SiGe device is 0.45 mS/mm, while it is 0.3 mS/mm for the Si control device. At high transverse fields, the improvement of linear transconductance for the graded SiGe device becomes insignificant because the transconductance becomes surface-roughness-scattering limited. In the saturation region, there is a 50% peak transconductance improvement for the graded SiGe NMOSFET compared with the Si control device.

VI. Conclusion

Strained SiGe vertical PMOSFETs and NMOSFETs have been fabricated by Ge ion implantation and SPE. Unlike the electron mobility degradation in the in-plane direction in strained SiGe planar NMOSFETs, both the hole and electron mobility enhancement in the out-of-plane direction have been demonstrated in this study of vertical MOSFETs. The effect of the built-in electric field in the graded SiGe channel has also been discussed. The enhancement of the electron mobility in strained SiGe is not as significant as the hole mobility enhancement. Since for CMOS devices, it is much more important to improve the performance of the PMOSFETs, based on our results, SiGe vertical MOSFETs are potential candidates for high performance vertical CMOS. Although the drive currents, transconductance, S and V_T of the devices are not as good as state-of-the-art Si MOSFETs, we believe that these parameters can be improved by optimization of the gate oxide thickness, channel doping and source/drain contacts. Since it is difficult to grow high quality thin thermal oxide on the sidewall of the pillar, high dielectric constant materials are alternatives for the gate dielectric and there are under investigation right now. Self-aligned silicide can also be used to reduce source/drain contact resistance.

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