

## Introduction

The LC series wireless data modules are intended for high-volume, low-cost applications. To be successful at designing a wireless data link using the LC series modules, all a designer must do is provide supply voltage and an antenna. All of the RF circuitry is contained in the LC module itself, relieving the designer of any RF engineering burden.

While the application of the module is quite straightforward, there are certain considerations which must be addressed due to the operational characteristics of the module and the legal regulations under which it operates.

## Output Power and Regulatory considerations

Linx Application notes #00140 and #00125 describe the FCC Part 15.231 regulations governing the LC module operation in great detail. This app-note assumes that you have already covered these topics and verified that your application is suitable under the FCC rules or the rules of the country in which operation is intended.

The LC-TX is a Carrier-Absent-Carrier-Present modulated transmitter. This special form of amplitude modulation is sometimes called On-Off-Keying because the two binary data states are represented as the conditions of “carrier off” or “carrier on”.

When data input is low, the transmitter fully suppresses the carrier to  $<-136\text{dBm}$ . This absence of carrier indicates to the receiver that a binary 0 is being sent.

When the data input transitions to a 1 (or a high) the transmitter generates a carrier. The receiver then sees this carrier, and translates its presence to a 1 on the data output of the receiver.

This method of modulation affords two benefits. First, it allows for some center frequency inaccuracies, which ultimately leads to simpler design and lower cost.

Second, it allows higher output powers per FCC Part 15.231 paragraph (b) subparagraph (2). By allowing the measurements made for carrier strength to be averaged over time, a much higher peak power can be achieved during the carrier-present portion of the data stream. For a 50% duty cycle square wave, it can be assumed that the transmitter will be on half the time, and, therefore, the transmitter can transmit at twice the peak output power. In cases where several “1” bits are sent in a row, the duty cycle of the wave form can increase significantly, also increasing the average output power of the transmitter. If the designer wishes to use the maximum output power available, he/she must first analyze the potential data streams to determine the most restrictive duty cycle and then design the antenna/attenuator accordingly.

This form of modulation also offers another benefit not inherent to its FM counterparts: it allows data rates from DC (or 0 hz) up to the maximum data rate of 4800 bits/second.

Depending on the antenna and the overall code balance used, the output power of the LC-TX can potentially violate FCC regulations. The output power is intentionally set high as we realize the designer will likely use an inefficient antenna to cut cost or save space and may use low Mark-to-Space code ratios. By providing this power margin, the designer can still realize the maximum output power allowed by the FCC using cheap, inefficient antennas or precisely match more efficient systems using an attenua-

tion pad as described in Application note #00150.

### Data In vs. Data Out

One of the most important points for a designer to consider is how the original data are affected by the transmission and recovery process. Each TX/RX design will cause some modification of the original square wave as it propagates from the transmitter circuitry, through free space, through the receiver, and finally out the receiver's data output. In this section, we will examine specifically how data are affected when transmitted with the LC series.

Figure 1 shows the RF output vs. a 4800 bps data input (modulated at 3V). The top trace is the time-domain RF output and the bottom trace is the modulation input. From this oscillograph, you can clearly see that there is a finite oscillator start-up time. Figure 2 shows the oscillator turn-on time for a single pulse.

Figure 3 is very similar to figure 1 except that the transmitter is operated and modulated at 5V instead of 3V. Under these conditions, the start-up time is shorter.

This start-up delay has two effects. First, it limits the maximum data rate possible to the start-up time itself. Second, it tends to shorten the data pulse.

The LC receiver discriminates a binary 1 from a binary 0 by the RF signal level of the carrier. Therefore, the receiver output will not go high until the transmitter oscillator has completed its start-up period. As a result, the LC receiver output will transition high a period of time after the data input, the time being determined by the transmitter start-up time.

The transmitter will also modify the data stream on a high-to-low transition. Once the data input has transitioned low, it takes a finite period of

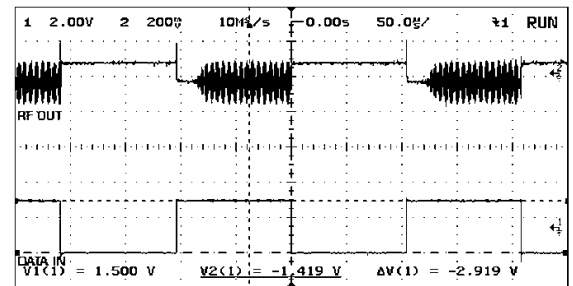


figure 1: Oscillator Response @3V (4.8Kbps)

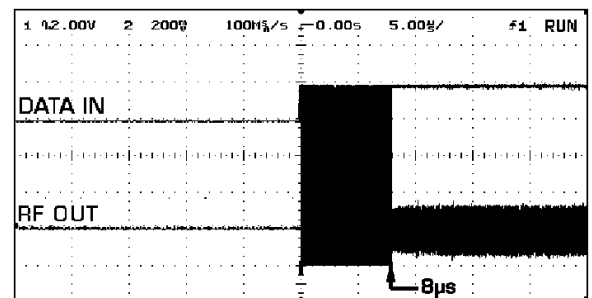


figure 2: Typical Oscillator Turn-On Time figure

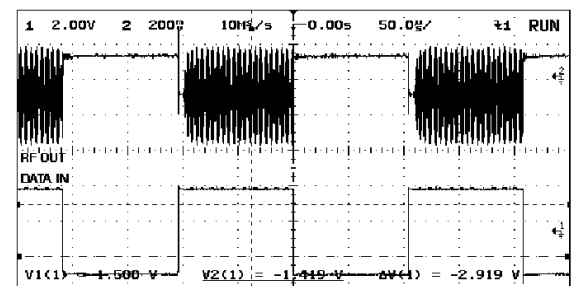


figure 3: Oscillator Response @5V (4.8Kbps)

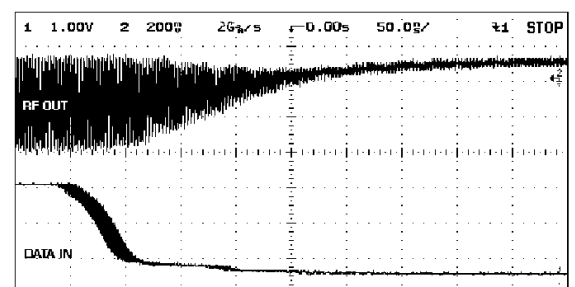


figure 4: Typical Oscillator Turn-Off Time

time for the transmitter oscillator to “ring-down”, as shown in figure 4. This will have the effect of stretching the pulse. This effect, however, is less prominent than the shortening effect due to start-up delay.

Like the transmitter, the receiver will also internally modify the data stream. Figure 5 shows that the receiver does not transition its data

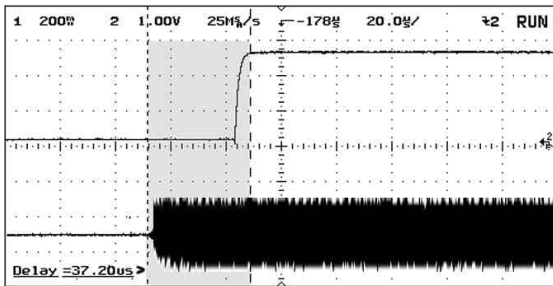


figure 5: RF in vs. Receiver response time

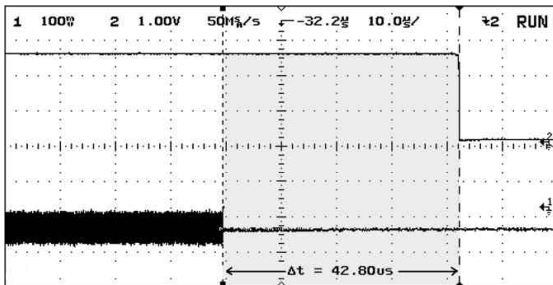


figure 6: Typical Receiver Turn-Off Time

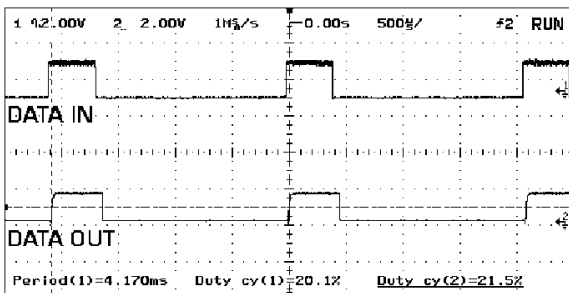


figure 7: Original vs. Received Data  
4,800 BPS 20% Duty Cycle

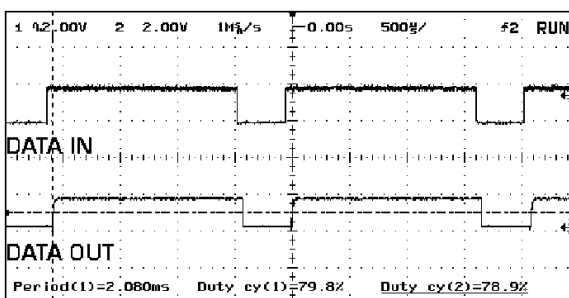


figure 8: Original vs. Received Data  
4,800 BPS 80% Duty Cycle

output high immediately after the transmitter has completed its start-up period. Instead, the receiver introduces a significant delay of 37.2uSec. This adds to the pulse-shortening effect caused by the transmitter oscillator start-up time.

Figure 6 shows the receiver's typical turn-off time, or the time it takes the receiver to transition its data output low after the transmitter carrier has been completely suppressed. This delay of 42.8uSec adds to the pulse-stretching effect due to the transmitter oscillator ring-down.

Figure 7 shows "data in" vs. "data out" for a 4800 bps bit stream with a 20% duty cycle. This would be representative of a data stream with two high bits and six low bits. The "data in" trace shows a duty cycle of 20.1%. The overall effects of pulse stretching and shortening explained here cause the data output duty cycle to be 21.5%.

Figure 8 shows "data in" vs. "data out" for a 4800 bps bit stream with a 80% duty cycle. This would be representative of a data stream with six high bits and two low bits. The "data in" trace shows a duty cycle of 79.8%. The overall effects of pulse stretching and shortening explained here cause the data output duty cycle to be 78.9%.

Thanks to the LC architecture, the effects of pulse shortening and pulse stretching tend to cancel each other and thus have little impact on the recovered data stream. It is important, however, that you keep these effects in mind when encoding and decoding your data stream.

## Encoding and Decoding

Now that we understand the effects that the LC Transmitters and Receivers have on the data stream, we can discuss appropriate encoding and decoding methods for the LC series modules.

In order to send data using the LC series mod-

ules, the data must be encoded in a serial stream of 1's and 0's. The method of encoding the data depends on the type of data to be sent.

For instance, if the designer wishes to send the status of a couple of push-button switches, then a remote control encoder and decoder would be in order. These inexpensive chipsets are available from several manufacturers including Linx, Motorola, National, and Holtek. A remote control encoder, such as the REC9072E from Linx Technologies, encodes a parallel input from a number of pushbuttons into a serial data stream that can be transmitted with the LC modules. The decoder (i.e. REC9071D) receives this serial data stream and updates its parallel outputs to represent the status of the pushbuttons at the encoder.

Most remote control encoders generate a simple serial data stream that can be asynchronously transmitted. The Linx encoder/decoders further encode the serial data stream in a pseudo-manchester format. Manchester encoding maintains a continuous 50% duty cycle in the

data stream output regardless of the data it is encoding. It does this by embedding the data clock in the data stream and using phase information to indicate data states. The benefit of manchester encoding is that when used in conjunction with an LC series transmitter, an FCC - legal design can achieve better range performance by virtue of a higher potential power.

Encoding and decoding can also be performed in microcontrollers. The microcontroller can generate the serial data stream via a UART or by manually toggling an I/O pin at a given rate.

The LC series modules are not capable of sending clocked data, unless the clock is embedded in the data stream as is the case in manchester encoding. Therefore, LC series modules are not suitable for transmitting serial data from a IIC or Microwire bus.

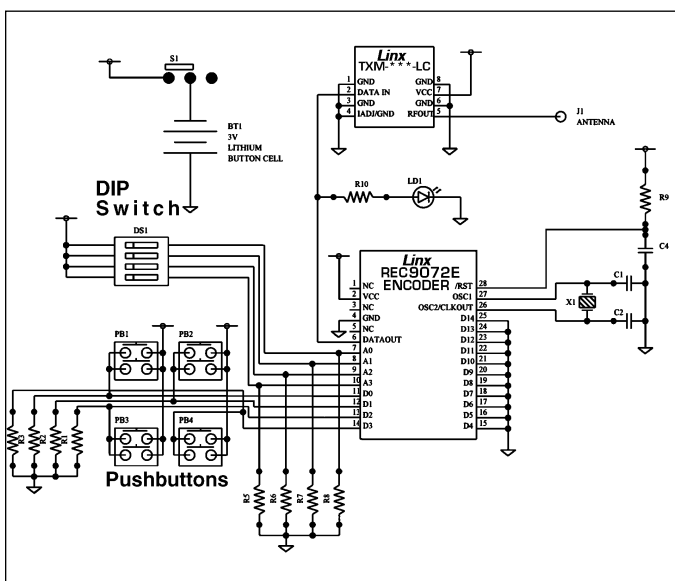


figure 9: Basic Remote Control Transmitter Circuit

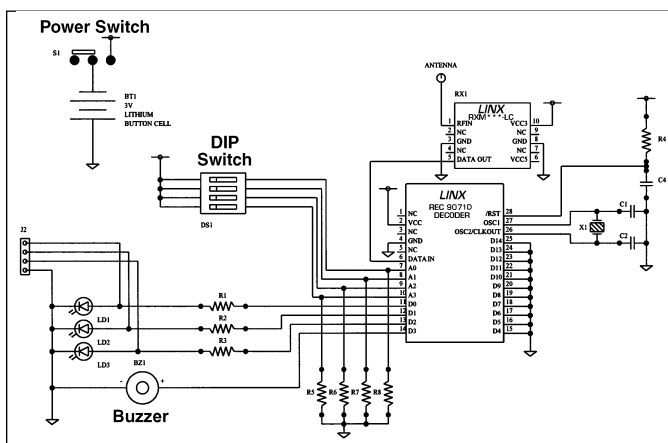


figure 10: Basic Remote Control Receiver Circuit