SHEFFIELD HALLAM UNIVERSITY

SCHOOL OF ENGINEERING

Course Title: BEng Electronic Systems Engineering

Unit Title: Microelectronics

Date: Thursday, 6 September 2001 **Time allowed: 3 hours**
From: 09.30 to 12.45
(Including 15 mins reading time)

INSTRUCTIONS TO CANDIDATES:

1. The normal University examinations apply (see scripts answer book)

2. Do not start writing until instructed to do so by an invigilator.

3. You may answer as many questions as you wish. Maximum credit will be given for the best FOUR answers only. If, however, the total mark is below a normal pass mark, all your answers will be taken into consideration, but only in order to award a bare pass mark.

4. All questions carry equal marks. The maximum attainable mark is 100.

	PLEASE TICK	PLEASE SPECIFY TYPE/NUMBER REQUIRED
TABLES ATTACHED	✓	List of Physical Constants
DIAGRAMS ATTACHED		
FORMULAE BOOKS REQUIRED		
16-PAGE BOOKLETS	✓	
8-PAGE BOOKLETS		
SUPPLEMENTARY BOOKS	✓	
GRAPH PAPER REQUIRED		

UNIT TUTOR: A Hassan/A Nabok

Physical Constants

Electron charge	$e = 1.60\ 10^{-19}$ C
Boltzmann's constant	$k = 8.62 \times 10^{-5}$ eV K^{-1} = 1.38×10^{-23} J K^{-1}
Dielectric permittivity of vacuum	$e_0 = 8.85 \times 10^{-12}$ F m^{-1}
Planck's constant	$h = 4.14 \times 10^{-15}$ eV s
Intrinsic carriers concentration for silicon at room temperature	$n_i = 1.45 \times 10^{16}$ m^{-3}
Relative dielectric permittivity of Si	$e_s = 11.9$
Relative dielectric permittivity of SiO_2	$e_{ox} = 3.9$
Thermal energy at room temperature	$\frac{kT}{e} = 0.0259 V$, $kT = 0.0259\ eV$, $(T = 300K)$

1. Statistics of electrons and holes in semiconductors

(a) Describe the energy distribution of carriers in metals and semiconductors. Give a definition (definitions) of a Fermi level.

[7 Marks]

(b) What is the position of the Fermi level in intrinsic silicon, assuming that the density of states in both conductive and valence bands are equal? Calculate the position of the Fermi level in silicon doped with phosphorous with a concentration of $10^{17}cm^{-3}$?

[8 Marks]

(c) Calculate the room temperature resistance of a planar resistor made by diffusion of phosphorous of 10^{17} cm^{-3} into p-type silicon with $N_D=10^{16}$ cm^{-3}. The depth of p-type diffusion region is 1 μm; the length and width are 100μm and 5μm, respectively. The values of the mobility for electrons and holes in silicon are:

$$\mu_e = 1350\ cm^2V^{-1}s^{-1} \text{ and } \mu_h = 450\ cm^2V^{-1}s^{-1},\ \text{respectively}$$

[10 Marks]

2. MS contact and P-N junction

(a) With the aid of band diagrams describe the difference between Schottky and Ohmic contacts for a n-type semiconductor

[9 Marks]

(b) Write down three major differences between the Schottky diode and the p-n junction diode.

[7 Marks]

(c) Write down the Shockley formula for current-voltage characteristics of an ideal p-n junction. Explain the meaning of the parameters in this expression. Given a reverse saturation current of $2\,nA$ for a p-n junction diode, calculate the current value when a forward biased voltage of 0.5V is applied.

[9 Marks]

3. Bipolar transistor and JFET

(a) What is the difference in operational principles of a bipolar transistor and a JFET? Use appropriate diagrams for your explanation.

[7 Marks]

(b) A *pnp* silicon bipolar junction transistor with effective cross-section area of $3\times10^{-2}\,mm^{-2}$, and an emitter and base widths of $2.5\,\mu m$. The mean doping concentrations of the Emitter, Base and Collector regions are $10^{19}\,cm^{-3}$, $2\times10^{16}\,cm^{-3}$ and $1\times10^{16}\,cm^{-3}$, respectively. Given the minority carriers drift mobility $m_h = 410\,cm^2\,V^{-1}\,s^{-1}$, and intrinsic carrier concentration $n_i = 1.45\times10^{10}\,cm^{-3}$, and using the following formula:

$$I_E = \frac{eAD_h n_i^2}{N_d W_B}\exp\left(\frac{eV_{EB}}{kT}\right),$$

where $D_h = \left[\frac{kT}{e}\right] m_h$, and N_d is the donor concentration in the base region, and W_B is the base width, calculate the emitter current I_E for a bias voltage $V_{EB} = 0.65V$ at room temperature. Also calculate the small signal input resistance r_e of the transistor in the common base configuration.

[10 Marks]

(c) An n-channel JFET is used for an ac amplifier in a common source arrangement. If this JFET has I_{DSS} of 15 mA, a pinch-off voltage V_P of - 4V, a gate dc bias voltage V_{GS} = –2V, calculate the dc drain current I_{DS} using a following formula:

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS\,(off)}}\right)\right]^2$$

and determine the transconductance g_m at this value of I_{DS}

[8 Marks]

4. MIS structures, MOSFET

(a) Describe schematically the CV characteristics of an ideal MIS structure for n-type semiconductor for both low and high frequency. Draw schematic band diagramsof the above MIS structure for different situations on the semiconductor surface.

[10 Marks]

(b) Calculate the flat-band voltage for the real Al-SiO_2-nSi structure, if the oxide thickness is 120 nm, the diameter of an Al electrode is 2.5 mm, and the density of surface charge on the Si-SiO_2 interface is 8×10^{11} cm^{-3}. Use the value of –0.2 V for f_{ms} . What kind of MOSFET can be made on the above MIS structure?

[9 Marks]

(c) Calculate the drain current of the MOSFET based on the above structure with the dimensions Z = 50 µm and L = 10µm at V_{DS} = 10V and V_{GS} = - 7 V using the following formula:

$$I_{DS} = K(V_{GS} - V_{th})^2(1 + lV_{DS}), \quad K = \frac{Zm_h e_s}{2Ld_{ox}}.$$

Assume V_{th}= - 4.5 V and λ= 0.01. The value of mobility of holes is 450 $cm^2V^{-1}s^{-1}$

[6 Marks]

5. Microelectronics technology

(a) The surface of an n-type silicon wafer having $N_D = 10^{16}$ cm^{-3} is doped by ion implantation of boron with a total surface concentration of $Q = 10^{23}$ m^{-2}, and followed by a drive-in diffusion at 1100°C for 60 min. Determine the depth of the P-N junction formed. Impurity concentration *(N)* as a function of distance (*x)* and time (*t)* for a constant quantity of dopant Q is described by Gaussian distribution function: $N = \frac{Q}{(p\,D\,t)^{1/2}}\left[\exp\left(-\frac{x^2}{4Dt}\right)\right]$,
where the diffusion coefficient (*D*) of boron at 1100°C is 3×10^{-17} m^2/s.

[10 Marks]

(b) During the drive-in diffusion (see conditions above), the layer of silicon oxide is growing up. Calculate the thickness of the oxide layer grown, assuming the mechanism of wet oxidation ($t_o = 0$). The thickness of the oxide layer is given by:

$$d = \frac{A}{2}\left[\sqrt{\left(1 + \frac{t + t_o}{A^2/4B}\right)} - 1\right]$$

where *A=0.205mm, B=0.549mm²/h*,

[8 Marks]

(c) The silicon wafer of 300 μm thickness, is thermally oxidised, and the thickness of the obtained oxide layer is 1.5 μm. Then the wafer is then put into HF. What is the resulting thickness of the wafer?

[7 Marks]

6. CMOS FET fabrication

(a) Describe the operation of a CMOS inverter. What is the main advantage of this kind of device?

[9 Marks]

(b) Draw schematically both the cross-section and layout of an n-channel MOSFET.

[9 Marks]

(c) Name four basic technological processes required for MOSFET fabrication?

[7 Marks]