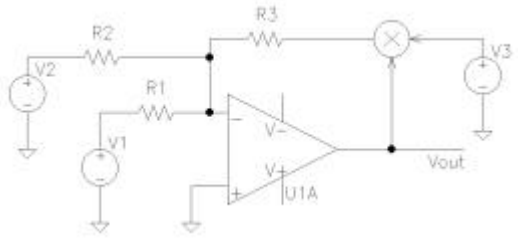
Analogue

Q4 (a)



Output of multiplier is Vout x V3 **2**

Applying KCL at op amp inverting node

$$\frac{V1}{R1}+\frac{V2}{R2}+\frac{Vout\times V3}{R3}=0$$ **2**

$$\frac{Vout\times V3}{R3}=-\frac{V1}{R1}-\frac{V2}{R2}$$

$$\therefore Vout=-\frac{R3}{V3}\left(\frac{V1}{R1}+\frac{V2}{R2}\right)$$ **2**

V1, V2 and V3 can (independently) be of either polarity. The only constraint on the voltages being that the resulting output voltage is within the capabilities of the op amp/power supply. **2**

(b) derive input/output relationship as follows

The output of U1 is $-2V_T \ln\frac{V_{in}}{R_1}+2V_T \ln I_s$.

The output of U3 is $-V_T \ln\frac{V_{out}}{R_3}+V_T \ln I_s$.

The base-emitter voltage of Q3 is therefore **3**

$$-V_T \ln\frac{V_{out}}{R_3}+V_T \ln I_s+2V_T \ln\frac{V_{in}}{R_1}-2V_T \ln I_s.$$

This can also be equated to $V_T \ln I_{C3}-V_T \ln I_s$, giving

$$V_T \ln I_{C3}-V_T \ln I_s=-V_T \ln\frac{V_{out}}{R_3}+V_T \ln I_s+2V_T \ln\frac{V_{in}}{R_1}-2V_T \ln I_s$$ **2**

$$\ln I_{C3}=-\ln\frac{V_{out}}{R_3}+2\ln\frac{V_{in}}{R_1}$$

$$\ln I_{C3}=\ln\left(\frac{V_{in}}{R_1}\right)^2\frac{R_3}{V_{out}}$$

$$I_{C3}=\left(\frac{V_{in}}{R_1}\right)^2\frac{R_3}{V_{out}}$$ **2**

Due to the action of the capacitor, C1, in parallel with R2, the output voltage is the average or mean value of I_{C3} x R2.

$$V_{out} = \overline{\left(\frac{V_{in}}{R_1}\right)^2 \frac{R_3}{V_{out}} R_2} \quad \textbf{2}$$

Since V_{out} and the resistors are constant, the mean value of these elements is the same as the element value itself, hence the bar can be removed:

$$V_{out} = \overline{V_{in}^{\,2}} \frac{R_3 R_2}{R_1^{\,2} V_{out}}$$

$$V_{out}^{\,2} = \overline{V_{in}^{\,2}} \frac{R_3 R_2}{R_1^{\,2}}$$

$$V_{out} = \sqrt{\overline{V_{in}^{\,2}} \frac{R_3 R_2}{R_1^{\,2}}} \quad \textbf{2}$$

or equivalent

(c) Suitable solution should explain that frequency compensation is required for stability. The additional gain and phase shift provided by the transistors in the feedback path of the op amp can cause instability even for an op amp that is already compensated for unity gain. **2**

Normally the (additional) compensation would be applied by placing a capacitor (typically 30-300pF) between the inverting input and the output of U1 and U3. **2**

The circuit is most likely to burst into oscillation with large input signals since the current gain of the transistors generally increases with collector current. **2**

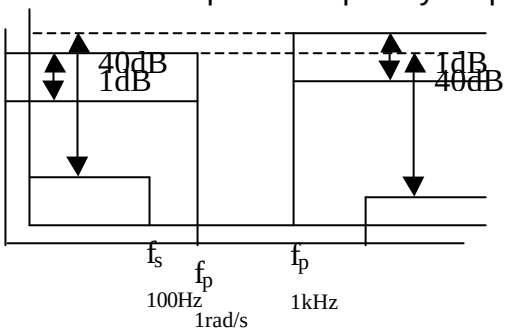
Total	**25**

Q5 (a) Solution should include

- Figure Q5a(i) is a linear regulator – suitable brief description of operation
- Figure Q5a(ii) is a switching regulator – suitable brief description of operation
- suitable discussion and comparison of efficiencies, load on critical components and output voltage current characteristics.

Marked on merit f_s 10rad/s **8**

(b) (i) Sketch of required frequency response



Transforming to normalised low-pass filter prototype:

$$w_s' = \frac{f_0}{f_s}$$

$$\therefore w_s' = \frac{1000}{100} = 10$$

Therefore the low-pass prototype specification is

or equivalent in text form **3**

To get the lowest order filter use the Chebyshev response **2**

$$n \geq \frac{\cosh^{-1}\left[(10^{a\,\min/10}-1)/(10^{a\,\max/10}-1)\right]^{1/2}}{\cosh^{-1}(w_s/w_p)}$$

$$n \geq \frac{\cosh^{-1}\left[(10^{40/10}-1)/(10^{1/10}-1)\right]^{1/2}}{\cosh^{-1}(10/1)}$$

$$\therefore n \geq 1.995798$$

$\therefore$ choose n=2 (Butterworth gives n=3) **4**

from the n=2, 1dB Chebyshev polynomial tables

$$H(s) = \frac{1}{s^2 + 1.09773433s + 1.10251033}$$ **3**

(b) (ii) Transforming normalised low-pass prototype to required high pass response:

using the transformation $s' = \frac{w_o}{s} = \frac{2p \times 1000}{s}$ **1**

$$H(s) = \frac{1}{\left(\frac{2p \times 1000}{s}\right)^2 + 1.09773433\left(\frac{2p \times 1000}{s}\right) + 1.10251033}$$ **2**

Multiply top and bottom by s^2

$$H(s) = \frac{s^2}{(2p \times 1000)^2 + 1.09773433 \times 2p \times 1000s + 1.10251033s^2}$$

re-arranging gives

$$H(s) = \frac{0.90702098s^2}{s^2 + 6.255967e3s + 3.580775e7}$$ **2**

Total	**25**

Q6 (a) Suitable definitions and principal characteristics should include

- static power dissipation
- max theoretical efficiency
- distortion characteristics
- practicality of implementation

Marked on merit **8**

(b) (i) Due to the current mirror action of Q4 and Q5, the current through R3 is 1.463 mA. 1

The voltage drop across R3 is therefore 1.463 x 9.7 = 14.1911 V 1

The base-emitter voltage of Q3 is given by $V_T \ln \frac{I_{C3}}{I_S}$

$= 26\times10^{-3} \ln \frac{1.463\times10^{-3}}{3.59\times10^{-14}}$

=0.6352 V 1

Due to the potential divider action of R4 and R5, the collector-emitter voltage of Q3 (assuming high current gain) is
0.6352 x 2.5 = 1.588 V 1

The voltage at the base of Q2 is –15 + 14.1911 = -0.8089 V 1

The voltage at the base of Q1 is –0.8089 + 1.588 = 0.7791 V 1

(ii) Given the output voltage of 37.25 mV, the base-emitter voltage of Q1 is 0.7791 – 0.03725 = 0.74185 V 2

The collector current is therefore given by $I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$

$\therefore I_{C1} = 3.59\times10^{-14} \exp\left(\frac{0.74185}{0.026}\right) = 88.447\ mA$

Similarly

$I_{C2} = 650\times10^{-18} \exp\left(\frac{0.84615}{0.026}\right) = 88.449\ mA$ 4

(iii) For class A operation of this circuit, the peak current is twice the quiescent current. 2

The maximum amplitude for Vout is therefore given by I_{max} x R1
=0.0885 x 4
=354 mV 3

Total **25**