SALIL KANHERE

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Research Interests

My research interests span the areas of networking, parallel and distributed systems, mobile and wireless computing and computer architecture. I am particularly interested in Quality of Service (QoS) in computer networks, switch and router architectures and mobile ad-hoc networks (MANET).

Education

Drexel University **Philadelphia, PA, USA**
Ph.D in Electrical Engineering Jun. 2003
GPA: 4.0
Dissertation Title: "*Design and analysis of fair, efficient and low-latency schedulers for high-speed packet-switched networks*"

The dissertation proposes a number of novel packet scheduling strategies for providing various Quality of Service (QoS) guarantees in the form of analytically provable bounds on the end-to-end delay and bandwidth allocation. A particular focus of this work is on achieving low implementation complexity for practical use in switches and routers.

Drexel University **Philadelphia, PA, USA**
M.S. in Electrical Engineering Mar. 2002
GPA: 4.0

V.J.T.I., University of Bombay **Bombay, India**
B.E. in Electrical Engineering Jun. 1998

Work Experience

Drexel University **Philadelphia, PA, USA**
Research Assistant, Computer Communications Laboratory Jun. 1999 – present

- Mobile Ad-hoc Networks
  Developed a detailed simulation model of a mobile ad-hoc network (MANET) using OPNET. This work involves a thorough top-to-bottom simulation of all the protocol layers. Used this model to study the effectiveness of existing protocols such as TCP, AODV and WLAN 802.11b in guaranteeing reliable data transmission for mission-critical applications.
- Packet Scheduling Algorithms
  Designed novel fair and efficient scheduling techniques for delivering Quality of Service (QoS) guarantees in ATM switches, Internet routers and the interconnection networks of multi-computer systems. Analyzed performance bounds (fairness, work complexity and latency) and conducted simulation-based evaluation of all the above schemes.

- TCP Fairness in Wireless Networks
  Evaluated various versions of TCP such as Tahoe, Reno, New Reno and SACK for their fairness properties in multi-hop wireless networks. Analyzed the effects of packet size, load, TCP buffer size and RTS/CTS on TCP fairness. The simulation model was developed using OPNET™ Modeler.
- Interconnection Networks
  Investigated and analyzed switch designs for use in interconnection networks of parallel systems as well as IP and ATM networks. Developed an exhaustive simulation model of a switch (written in Java). Designed fair and efficient scheduling strategies for reducing latency in wormhole switches with virtual lanes.

Drexel University **Philadelphia, PA, USA**
Teaching Assistant, ECE Department Sep. 1998 – present

- Responsibilities include conducting recitations and lectures, grading quizzes and assignments, and organizing help sessions for the following courses:
  - Physical Foundations of Engineering I – III
  - Fundamentals of Intelligent Systems
  - Secure Computing Systems
  - Computer and Network Security
  - Computer Arithmetic
  - Computer Hardware
  - Intelligent System Architecture
  - Principles of Computer Networking
  - Performance Analysis of Computer Networks
  - Digital System Projects

Sushobhan Interiors **Bombay, India**
Summer Intern Jun. 1995 – Aug.1995 and Jun. 1996 – Aug. 1996

- Assisted in system administration activities.
- Contributed to the development and maintenance of the company web site.

Publications

(Online copies of all published papers can be found at http://www.ece.drexel.edu/CCL/kanhere/)

Journal Papers

1. S. S. Kanhere and H. Sethu, "Low-Latency Guaranteed-Rate Scheduling using Elastic Round Robin", in *Computer Communications*, vol. 25, no. 14, September 2002, pp. 1315-1322.
2. S. S. Kanhere, H. Sethu and A. B. Parekh, " Fair and Efficient Packet Scheduling Using Elastic Round Robin", in *IEEE Transactions on Parallel and Distributed Systems*, vol. 13, no. 3, March 2002, pp. 324-336.
3. S. S. Kanhere and H. Sethu, "Anchored Opportunity Queuing: A Low-Latency Scheduler for Fair Arbitration among Virtual Lanes", to appear in *Journal of Parallel and Distributed Computing*.
4. S. S. Kanhere and H. Sethu, "On the Latency and Fairness of Pre-Order Deficit Round Robin", submitted to *Computer Communications*, January 2003.
5. S. S. Kanhere and H. Sethu, "Prioritized Elastic Round Robin: An Efficient Low-Latency Scheduling Algorithm with Improved Fairness", submitted to *Computer Networks*, March 2003.

6. H. Shi, H. Sethu and S. S. Kanhere, "An Evaluation of Fair Packet Schedulers using a Novel Measure of Instantaneous Fairness", submitted to *Computer Communications, Special Issue on End-to-End Quality of Service Differentiation*, June 2003.
7. S. S. Kanhere and H. Sethu, "Fair Efficient and Low-Latency Packet Scheduling using Nested Deficit Round Robin", in preparation for submission to *International Journal of Communication Systems.*

Conference Papers

8. S. S. Kanhere and H. Sethu, "On the Latency Bound of Pre-Order Deficit Round Robin", in *Proceedings of the IEEE Conference on Local Computer Networks*, Tampa, Florida, November 2002, pp. 508-517.
9. S. S. Kanhere and H. Sethu, "On the Latency Bound of Deficit Round Robin", in *Proceedings of the International Conference on Computer Communications and Networks*, Miami, Florida, October 2002, pp. 548-553.
10. S. S. Kanhere and H. Sethu, "Fair, Efficient and Low-Latency Packet Scheduling using Nested Deficit Round Robin", in *Proceedings of the IEEE Workshop on High Performance Switching and Routing,* Dallas, Texas, May 2001, pp. 6-10.
11. S. S. Kanhere and H. Sethu, "Fair Efficient and Scalable Scheduling Without Per-Flow State", in *Proceedings of the IEEE International Performance, Computing, and Communications Conference,* Phoenix, Arizona, April 2001, pp. 181-187.
12. H. Sethu, H. Shi, S. S. Kanhere and A. B. Parekh, "A Round-Robin Scheduling Strategy for Reduced Delays in Wormhole Switches with Virtual Lanes", in *Proceedings of the International Conference on Communications in Computing,* Las Vegas, Nevada, June 2000, pp. 275-278.
13. S. S. Kanhere, A. B. Parekh and H. Sethu, "Fair and Efficient Packet Scheduling in Wormhole Networks", in *Proceedings of the International Parallel and Distributed Processing Symposium,* Cancun, Mexico, May 2000, pp. 623-632.

Honors

- Allen Rothwarf Outstanding Graduate Student Award – Drexel University (2003)
- Graduate Student Research Award – Drexel University (2003)
- Teaching Assistant Excellence Award (Special Recognition Award) – Drexel University (2001)
- Teaching Assistant Excellence Award – Drexel University (1999)
- Dean's Fellowship – Drexel University (1998-1999)
- Air India Academic Scholarship (1994-1996)
- Mumbai Higher Secondary Certificate Board Mathematics Award – Bombay HSC Board (1994)
- Dr. Homi Bhabha Young Scientist Silver Medal – Greater Bombay Science Teachers Association, Mumbai (1991)

Presentations

- *Prioritized Elastic Round Robin: An Efficient Low-Latency Scheduling Algorithm with Improved Fairness*, Research Day, Drexel University, April 2003.
- *On the Latency Bound of Pre-order Deficit Round Robin*, IEEE Conference on Local Computer Networks, Tampa, November 2002.
- *Fair, Efficient and Low-Latency Packet Scheduling using Nested Deficit Round Robin,* IEEE Workshop on High Performance Switching and Routing, Dallas, May 2001.

- *Fair, Efficient and Scalable Scheduling Without Per-Flow State,* IEEE International Performance, Computing, and Communications Conference, Phoenix, April 2001.
- *Buffer Overflow Attacks*, Drexel University, February 2001.
- *Instruction Set Principles and Examples*, Drexel University, October 2000.
- *A Round-Robin Scheduling Strategy for Reduced Delays in Wormhole Switches with Virtual Lanes*, International Conference on Communications in Computing, Las Vegas, June 2000.
- *Concepts of Fault Tolerant Computing*, Drexel University, August 2000.
- *Wormhole Routing Techniques in Direct Networks*, Drexel University, June 2000.

Computer Skills

Operating Systems:	UNIX, Microsoft Windows NT, 4.0, 95, 98, 2000 & XP
Programming Languages:	C, C++, Java, VHDL and JavaScript
Software:	OPNET, Matlab, LaTeX, MS Office

Academic Projects

- *Operating System Memory Manager:* Designed and simulated the memory manager module of an operating system. Compared the performance of various memory allocation schemes such as first-fit, best-fit and next-fit. The simulator was developed in Java.
- *IP over ATM:* Completed a research project, which included an extensive literature survey on the various proposals of implementing IP over ATM with a focus on "IP Switching", originally developed by Ipsilon Networks.
- *Networked Database Application*: Designed a networked database as a client-server application using socket programming. The client and the server were developed using C in the Unix environment.
- *Interactive Web Site*: Designed an interactive web site using cascaded style sheets, DHTML and JavaScript for client side scripting. The site included an IP calculator that displayed the IP subnet address given an IP address and a subnet mask.
- *Computer Generated Visual Music:* Simulated a visual aid for learning the piano using a computer keyboard. The software was developed using C++.

Relevant Coursework

Graduate:

- Principles of Computer Networking
- Performance Analysis of Computer Networks
- Advanced Topics in Computer Networks
- Network Programming
- High Performance Computer Architecture
- Parallel Computer Architectures
- Advanced Parallel Computer Architectures
- Fundamentals of Computer Hardware
- Switching Functions: Issues in Combinational Circuit Design
- Finite Automata: Issues in Sequential Circuit Design
- Computer Arithmetic
- Operating Systems
- Stochastic Systems

Undergraduate:

- Digital Signal Processing
- Digital Communications
- Microprocessor Design
- Signals and Systems
- Digital Logic Design

References

Dr. Harish Sethu
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Dr. T. S. Venkataraman
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