

Alpa Parekh

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Home: 9398 1820
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KEY STRENGTHS

- Proven track record in professional software development and delivery of high quality software products.
- Strong communication skills along with the ability to work well in a team environment or autonomously.
- Quick learner with an ambition to expand my skill set.

EDUCATION

M.S. in Computer Science	GPA 4.0/4.0	Jan'02 - Jun'03
M.S. in Electrical Engineering	GPA 4.0/4.0	Sep'98 - Apr'00
Drexel University, Philadelphia, PA, U.S.A.		

B.E. in Electrical Engineering	Jul'94 - Jul'98
V.J.T.I, University of Mumbai, Mumbai, India.	

EXPERIENCE

Software Engineer IV Australian Centre for Unisys Software Unisys, Rhodes, NSW	Jun'04 - Present
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Responsibilities:

- Development, support and maintenance of a large-scale solution designed for transactional systems, conforming to CMMI quality processes using C++ and Visual Studio 2003.
- Unit and integration testing.
- Stress testing with customer system models.
- Maintenance of technical documentation using DOORS.
- Peer code reviews and reviews of product information and education documentation.

Achievements:

- Developed the assigned components of the debugger module as per schedule.
- Improved the fidelity of debugger module by reducing the SIL count by 60.
- Monitored the unit test suite of the debugger module on a timely basis that successfully helped the team reduce the regression failure rate.
- Developed the assigned components of the target builder module for MCP platform as per schedule.
- Supported the target builder for MCP platform during the field test phase by fixing customer raised issues.

Research Assistant Computer Science Department Drexel University, Philadelphia, PA, USA	Jan'02 - Dec'03
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Responsibilities:

- Investigation and analysis of various algorithms for computing the Fast Fourier Transform (FFT) widely used in many digital signal processing (DSP) applications.

Achievements:

- Developed simulation model of a distributed memory processor to compute FFT (written in Matlab).
- Designed an efficient FFT algorithm based on memory access cost function.

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- Successfully proved the superior performance of this algorithm as compared to other FFT algorithms using mathematical modeling and simulations.

Software Engineer
Lockheed Martin Global Telecom
Clarksburg, MD, USA

May'00 - Dec'01

Responsibilities:

- Requirements analysis, detailed design and software development for a terminal simulator project used to conduct testing of the network control centre.
- Design and document the software architecture of the assigned modules.
- Unit and integration testing.
- Peer code reviews and review of design documentation.

Achievements:

- Designed and developed the modules (written in C/C++) of the network terminal to simulate:
 - Asynchronous Transfer Mode (ATM) signaling operations for establishing calls (Q.2931, Q.2971, and UNI 4.0).
 - Address resolution as per Next Hop Resolution Protocol (NHRP).
 - Terminal network entry and exit operations.
 - Beam and regional broadcast message reception.
- Developed a test tool simulating network control centre that helped the integration testing of the terminal simulator.
- Supported factory acceptance test by assisting test engineers in the analysis of test reports.

Research Assistant
Computer Communications Laboratory
Drexel University, Philadelphia, PA

Sep'98 - Apr'00

Responsibilities:

- Investigation and evaluation of the scheduling techniques used in the switch designs for the interconnection networks of parallel systems as well as IP and ATM networks.

Achievements:

- Developed a simulation model of a networked switch (written in Java).
- Designed a fair and efficient scheduling technique for delivering good Quality of Service (QoS) in the interconnection networks of parallel system, ATM switches and Internet routers.
- Analyzed the performance of the proposed scheduler using analytical modeling and simulations. The outcome of this research has been published in a high-quality IEEE journal.

PUBLICATIONS

Journal:

- S. S. Kanhere, H. Sethu, A. B. Parekh, "Fair and Efficient Packet Scheduling Using Elastic Round Robin", in IEEE Transactions on Parallel and Distributed Systems, vol. 13, no. 3, March 2002, pp. 324-336.

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Conference:

- S. S. Kanhere, A. B. Parekh, H. Sethu, "Fair and Efficient Packet Scheduling in Wormhole Networks", in Proceedings of the International Parallel and Distributed Processing Symposium, Cancun, Mexico, May 2000, pp. 623-632.
- H. Sethu, H. Shi, S. S. Kanhere, A. B. Parekh, "A Round-Robin Scheduling Strategy for Reduced Delays in Wormhole Switches with Virtual Lanes", in Proceedings of the International Conference on Communications in Computing, Las Vegas, June 2000, pp 275-278.

M.S. Thesis:

- Alpa Parekh, "Fair and Efficient Packet Scheduling For High Speed Networks", Drexel University, Philadelphia, PA, USA, April 2000.

TECHNICAL SKILLS

- Programming Languages:
 - Microsoft C/C++ 5 years of experience
 - Java 2 years of experience
- Development Environments:
 - gcc and Sun CC on Solaris 2 years of experience
 - Visual Studio 2003 2 years of experience
- Concurrent Software Development Tools:
 - CVS 2 years of experience
 - CMSynergy 2 years of experience
- Packages and Libraries:
 - MATLAB 2 years of experience
- Databases:
 - SQL 2 years of experience
 - Oracle 1 years of experience
- Networking Technologies:
 - Nokia VPN Configuration 6 months of experience

ACADEMIC PROJECTS

- *Client-Server Application* – developed client and a concurrent stateful server (written in C) interacting via the socket interface.
- *Database Model For Retail Store* – designed a data model based on first normal form for a retail store. The designed model also provided SQL queries for the transactional purposes.
- *Memory Manager* – simulated a memory manager (written in Java) to manage memory using variable sized partitions and to compare the first-fit, next-fit and best-fit memory allocation strategies.
- *Prolog Interpreter* – developed an interpreter (written in Java) for a subset of Prolog, a declarative programming language.

HONORS

- Recipient of Dean's Fellowship, Drexel University, 1998-2000.
- Teaching Excellence Award Nominee, Drexel University, 2000.