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## ALPA PAREKH

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### EDUCATION

**Drexel University, Philadelphia, PA** June 2003  
M.S. in Computer Science  
GPA: 4.0

**Drexel University, Philadelphia, PA** May 2000  
M.S. in Electrical Engineering  
GPA: 4.0

**V.J.T.I, University of Bombay, Bombay, India** July 1998  
B.E. in Electrical Engineering

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### WORK EXPERIENCE

**Drexel University, Philadelphia, PA** May 2002- Present  
Research Assistant – Department of Computer Science

- Studied various algorithms for computing the Fast Fourier Transform (FFT) used widely in many digital signal processing (DSP) applications.
- Developed a simulation model of a distributed memory processor to compute FFT (written in Matlab).
- Designed an efficient FFT algorithm based on the memory access cost function.
- Analyzed the performance of the desired algorithm with that of other FFT algorithms via the test results.

**Lockheed Martin Global Telecom, Clarksburg, MD** May 2000- Dec 2001  
Software Engineer – Broadband Network Division

- Participated actively in the requirements analysis, detailed-design, software development, and integration and testing of the Astrolink Terminal Simulator (ATS) project.
- Supported design and documentation of the software architecture for the ATS to simulate Asynchronous Transfer Mode (ATM) signaling operations for establishing calls (Q.2931, Q.2971, and UNI 4.0) and resolving addresses (NHRP) in a secured network (IPSEC) in order to conduct testing of the Network Control Center (NCC) of the Astrolink Broadband Satellite Communication Network.
- Developed software components (written in C/C++) that simulate Astrolink terminal's network entry operations, beam and regional broadcast message reception and address resolution as per Next Hop Resolution Protocol (NHRP).
- Participated in peer code reviews. Conducted unit testing of the developed modules.
- Designed a test tool simulating Astrolink's Network Control Center (written in C) for pre-integration of the ATS. Supported integration and factory acceptance test (FAT) of the ATS by assisting test engineers in the analysis of test reports.

- Investigated and analyzed switch designs for the interconnection networks of parallel systems as well as IP and ATM networks.
  - Developed a simulation model of a switch (written in Java).
  - Designed a fair and efficient scheduling technique for delivering good Quality of Service (QoS) in the interconnection networks of parallel systems, ATM switches and Internet routers.
  - Performed the analysis and evaluation of the simulation results.
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## **PUBLICATIONS**

### **Journal Papers**

- S. S. Kanhere, H. Sethu, A. B. Parekh, “Fair and Efficient Packet Scheduling Using Elastic Round Robin,” in *IEEE Transactions on Parallel and Distributed Systems*, vol. 13, no. 3, March 2002, pp. 324-336.

### **Conference Papers**

- S. S. Kanhere, A. B. Parekh, H. Sethu, “Fair and Efficient Packet Scheduling in Wormhole Networks,” in *Proceedings of the International Parallel and Distributed Processing Symposium*, Cancun, Mexico, May 2000, pp. 623-632.
- H. Sethu, H. Shi, S. S. Kanhere, A. B. Parekh, “A Round-Robin Scheduling Strategy for Reduced Delays in Wormhole Switches with Virtual Lanes,” in *Proceedings of the International Conference on Communications in Computing*, Las Vegas, June 2000, pp 275-278.

### **M.S. Thesis**

- Fair and Efficient Packet Scheduling For High Speed Networks, April 2000.
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## **TECHNICAL SKILLS**

### **Operating Systems**

- Microsoft Windows, UNIX, MS-DOS.

### **Software Programming Languages**

- C, C++, Java, JavaScript, HTML, Matlab.

### **Hardware Programming Languages**

- VHDL.

### **Databases**

- Oracle, MySQL, MS Access.

### **Automated Software Tool**

- Concurrent Versions System (CVS).

### **Application Software**

- MS Office, System Architect.

### **Training**

- Configuration of Nokia Virtual Private Network (VPN) router, model CC5200.

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## ACADEMIC PROJECTS

- **Computer Generated Visual Music:** Simulated piano keys on a computer keyboard using C++. Also intended for the hearing impaired, each of the seven notes of the music was assigned a particular color and a geometric figure. When the user plays the piano, the corresponding figures along with respective colors flash on the screen.
- **Client-Server Application:** Designed a client-server application using the socket interface. Used TCP/IP as the mode of interaction between the client and the server. Designed a concurrent, stateful server that allows the client to store the name and age of the individuals (database). The server then retrieves the data upon the request initiated by the client. Developed both the client and the server using C.
- **Digital Rights Management System:** Surveyed several content protection schemes proposed in the literature. Presented a scheme for content protection based on asymmetric encryption and tamper-resistant software.
- **Database Model for Retail Store:** Designed a data model based on first normal form for a retail store. The designed model also provided SQL queries for transactional purposes.
- **Memory Manager:** Simulated a memory manager, a part of the Operating System that is responsible for managing the memory. This simulation was done using Java. The memory manager was implemented using linked lists and the memory was managed using variable sized partitions. The memory was allocated to the processes depending on the allocation strategy selected by the user. If enough memory was available to execute the process, the process was loaded into memory and the CPU executed the same. When the CPU finished executing the process, the memory was freed. This simulation was used to compare the following three memory allocation strategies, first-fit, best-fit and next-fit allocation strategies.
- **Interactive Web Page:** Designed an interactive web page using cascaded style sheets and DHTML. Used JavaScript for the client side scripting. Designed an IP calculator that displayed the IP subnet address given an IP address and a subnet mask.
- **Prolog Interpreter:** Developed an interpreter for a subset of Prolog, a declarative programming language. The interpreter was written in Java.
- **Stack Processor:** Simulated a processor based on stack architecture. The stack processor was modeled in VHDL. The project included designing the instruction set, memory, control unit and the stack. The user program was loaded in the memory of the processor. The stack processor would then execute this program.

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## HONORS

- Recipient of Dean's Fellowship from Drexel University.
- Excellence in Teaching Assistance Award Nominee.

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## REFERENCES

- Available upon request.