Design Space Exploration for optimization of the PISA architecture for mpeg2 decoder benchmark using wattch simulator

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Steps involved in Design Space Exploration

- Source Code Analysis.
- Intuitive Design on the basis of Analysis.
- Selection of cost Function.
- Selection of simulation parameters.
- Design space definition.
- Analysis of Simulation results.
- Optimal Configuration

Source Code Analysis.

- Bulk processing of encoded image
- Big amount of data
- Lot of nested loops
- Less data dependency

Intuitive Design on the basis of Analysis.

- dl1 block size
  - Related data occurrence.
  - Performance enhancement can be achieved.
- RUU (Register Update Unit) size
  - Less dependency on intermediate values
  - More out of order execution in simulation.
- Il1 cache size
  - Lot of looping instructions.

Selection of cost Function.

- Lot of processing employs energy consideration.
- Performance is measured from Delay.
- Cost function = Energy*Delay.
  - Where Energy is total_power_cycle_cc3.
  - Delay is sim_cycle.

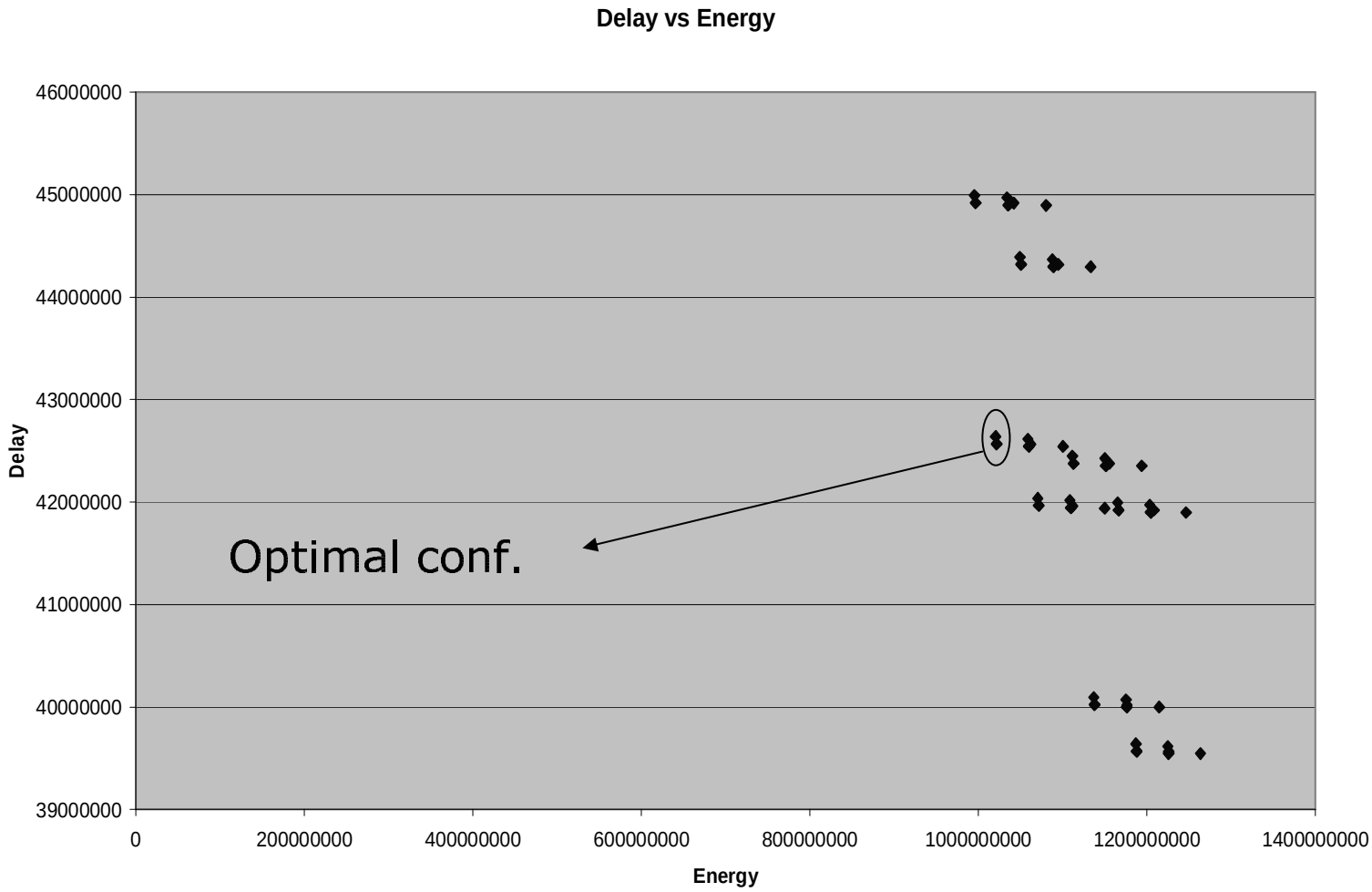
Selection of Simulation parameters.

- L1 data cache parameters.
- L1 Instruction cache parameters.
- L2 Unified cache parameters.
- Register Update Unit (RUU) size
- Number of floating point ALU.

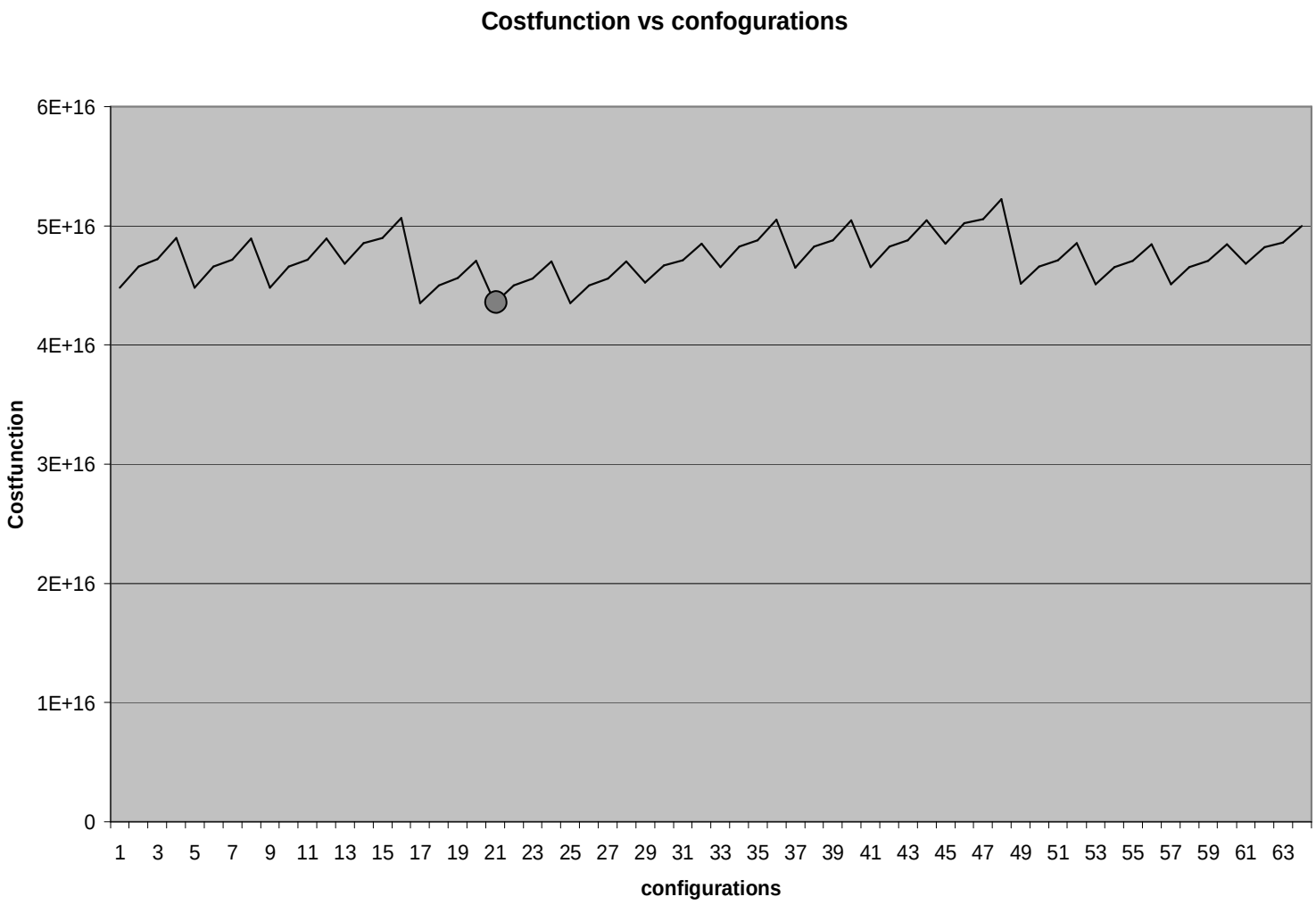
Design Space Definition

- DL1:128{32,64}:4:L
- IL1:{128,256}:32:1:L
- UL2:{1024,2048}:{64,128}:4:L
- RUU:{32,64}
- FPALU:{1,4}

Analysis of Simulation results.



Analysis of Cost Function.



Optimal Configuration

- -cache:dl1 dl1:128:32:4:l
- -cache:il1 il1:256:32:1:l
- -cache:dl2 ul2:1024:64:4:l -cache:il2 dl2
- -ruu:size 32
- -res:fpalu 1

- *-cache:dl1 dl1:128:32:4:l*
- *-cache:il1 il1:256:32:1:l*
- *-cache:dl2 ul2:1024:128:4:l -cache:il2 dl2*
- *-ruu:size 32*
- *-res:fpalu 1*

- -cache:dl1 dl1:128:32:4:l
- -cache:il1 il1:256:32:1:l
- -cache:dl2 ul2:2048:64:4:l -cache:il2 dl2
- -ruu:size 32
- -res:fpalu 1

Optimal Configuration

- **dl1:128:32:4:l**
- **il1:256:32:1:l**
- **ul2:1024:128:4:l**
- **ruu size 32**
- **fp-alu 1**

Conclusion

- Increasing the l1 instruction cache number of sets gives better performance.
- L2 caches separation gives no significant improvement.
- No difference on increasing no. of iALUs.
- Significant performance improvement on increasing L1 data cache block size.
- Increasing RUU size improves performance but also greatly increases Energy Consumption.