Discussion of results: We refer to Figs. 2 and 3. Fig. 2 shows the normalised amplitude distribution of the field E_t as a function of position across the slot narrow dimension for two different offsets. The case $y_0 = 4$ m shows a behaviour similar to that assumed in Reference 6. That for $y_0 = 0{\cdot}25$ mm (for which the slot overlaps the waveguide centreline) exhibits an E_t that is asymmetrical with respect to the slot narrow dimension. More importantly, Fig. 3 shows the phase of E_t as a function of ζ for a number of y_0 values. Observe that although this phase variation is small for $y_0 \geq 2$ mm, it becomes increasingly severe for the slots $y_0 = 0{\cdot}5$, $0{\cdot}25$ and $0{\cdot}0$ mm which overlap the waveguide centreline. It would appear correct to state that the expansion functions for the slot field distribution used in the usual moment method formulations [5, 6] would need to be altered so that they are able to represent such a phase variation if the technique is to be used to compute the properties of small-offset slots of the type used in existing arrays [3]. We note that it was observed that E_t is indeed almost zero over most of the slot except for points extremely close to the shorter edges of the slot, where it shows an 'edge condition' type behaviour. Also, E_t was observed to have the expected cosinusoidal distribution along the slot for the offsets examined.

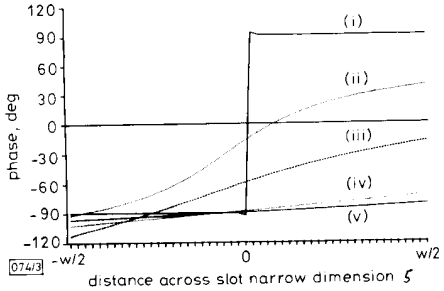

Fig. 3 *Phase distribution of field E_t as function of position ζ across narrow dimension of slot, with slot offset y_0 as parameter*

Waveguide dimensions are $22{\cdot}86 \times 5{\cdot}08\,mm^2$ (half height) and computations were performed at 9 GHz

(i) $y_0 = 0{\cdot}0$ mm
(ii) $y_0 = 0{\cdot}25$ mm
(iii) $y_0 = 0{\cdot}5$ mm
(iv) $y_0 = 2{\cdot}0$ mm
(v) $y_0 = 4{\cdot}0$ mm

Conclusions: It has been theoretically demonstrated that the field distribution is a small-offset longitudinal slot in the broad wall of a rectangular waveguide has significant phase variation across the slot width (narrow dimension). If small-offset slots which overlap the host waveguide centreline are to be used in an array design the slot data used should be obtained from an integral equation moment method analysis that uses expansion functions that permit such phase variations. This requirement would entail the enhancement of existing integral equation based numerical analyses [5, 6] of such slots.

17th October 1991

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X-BAND DIRECTIVE SINGLE MICROSTRIP PATCH ANTENNA USING DIELECTRIC PARASITE

R. Afzalzadeh and R. N. Karekar

Indexing terms: Antennas, Microstrip, Dielectric devices

A new method to enhance the gain of a single microstrip patch antenna using spaced superstrates as a dielectric parasite is presented. The experimental results of radiation pattern using alumina parasites with different thicknesses and spacings are given. The minimum beamwidth obtainable with a single patch using present studies is only 18° with symmetric lobes in the H and E planes. This simple method can also be used to vary the beamwidth of the patch between 18 and 125° with proper choice of parasite parameters.

Introduction: One of the major disadvantages of the microstrip patch antenna (MPA) is its low gain. To enhance the gain of this antenna, an array of patch elements normally is used. For example a planar array of 4 × 4 elements gives a beamwidth of 15° in both planes [1]. Other methods reported recently use two [2] and three [3] layers of metallic parasitic directors or using a thick layer of magnetised ferrite overlay [4] on the patch giving beamwidths of 50, 35 and 30°, respectively (H plane).

This Letter reports an experimental study on the radiation pattern of an X-band rectangular MPA using, as the parasitic elements, spaced superstrates made from alumina sheets of two different sizes, with various thicknesses and also various spacings between the MPA and PE.

Experimental results: The rectangular MPA, designed using the modal expansion cavity model, is fabricated [5] on a $25{\cdot}4 \times 25{\cdot}4\,mm^2$ substrate ($\varepsilon_r = 9{\cdot}8$, $h = 0{\cdot}635$ mm and $\tan\delta = 0{\cdot}0001$) using the inset method for feeding. The dimensional parameters of the MPA, namely width, length and inset, are 7·953, 4·584 and 1·54 mm, respectively, giving a resonance frequency f_r of 9·76 GHz ($\lambda_0 = 30{\cdot}7$ mm).

Spaced alumina superstrates ($C_r = 9{\cdot}8$) are used as the parasitic elements (PEs) (Fig. 1) with sizes of $51 \times 51\,mm^2$ or $25{\cdot}4 \times 25{\cdot}4\,mm^2$ having thickness d up to $0{\cdot}52\lambda_m$ (where $\lambda_m = \lambda_0/\sqrt{(\varepsilon_r)}$). The spacing s between the MPA and the dielectric

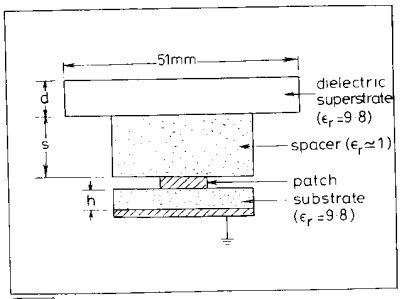

Fig. 1 *Geometric arrangement for rectangular microstrip patch antenna, with spaced dielectric superstrate used as parasitic element*

PE is varied up to $1.95\lambda_0$, using expanded thermocoal ($\varepsilon_r \simeq 1.05$) as the spacer. This spacer does not show any significant effect on other parameters of the antenna. Also the changes in f_r and reflection coefficient with dielectric PE, for $S > 0.5\lambda_0$, are negligible.

About 80 radiation patterns are recorded both with and without PE all being fed at their corresponding f_r. Table 1 summarises the data. The relative gain A_n in Table 1 is the ratio of peak amplitude of the pattern with PE to that without PE.

Table 1 SOME TYPICAL MEASURED VALUES FOR RECTANGULAR MPA WITH DIELECTRIC PARASITE ($\lambda_0 = 30.7$ mm, $\lambda_m = 9.8$ mm)

Size of parasitic element ($L \times W$) (mm^2)	Relative spacing (S/λ_0)	Range of relative thicknesses (d/λ_m)	Range of lobewidths (HP) (deg)	Range of normalised amplitudes (A_n)
Without superstrate	—	—	60 H plane 90 E plane	1 1
(H plane)	0.00	0.065–0.19	55–125	0.12–0.76
	0.10	0.065–0.52	116–41	0.30–1.36
51 × 51	0.81	0.065–0.52	85–23	0.40–4.70
	0.98	0.065–0.52	38–21	1.70–5.40
	1.46	0.065–0.52	39–21	1.30–5.20
	1.95	0.065–0.52	37–18	1.50–4.60
(H plane)	0.81	0.52	32	2.50
	0.98	0.52	31	2.50
25.4 × 25.4	1.45	0.52	33	1.90
	1.95	0.52	29	2.00
(E plane)	0.81	0.52	22	4.70
	0.98	0.065–0.52	39–22	0.95–5.40
51 × 51	1.95	0.065–0.52	27–18	1.40–4.60

Some typical radiation patterns are given in Fig. 2 which show that for a PE of certain size, the beamwidth is smaller for a larger value of S/λ_0 (curve (iii)) compared to that for smaller S/λ_0 (curve (ii)). Further, for the same S/λ_0 the beamwidth is larger for a smaller size of PE (curve (iv)) compared to that for larger PE (curve (iii)). The results for the radiation pattern in the E plane show nearly the same beamwidth under similar conditions (see Table 1). The sidelobes are normally small (about 6–15 dB down).

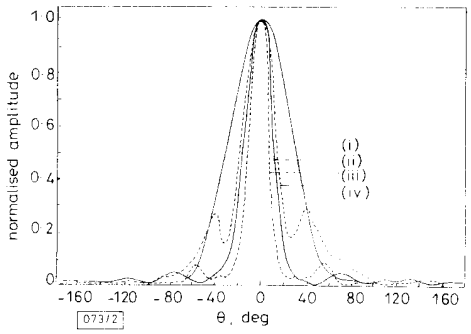

Fig. 2 *Normalised typical radiation patterns of rectangular MPA with alumina parasite*

$d/\lambda_m = 0.52$
(i) no parasite
(ii) $S = 0.98\lambda_0$ $L_1 = W_1 = 51$ mm
(iii) $S = 1.95\lambda_0$ $L_1 = W_1 = 51$ mm
(iv) $S = 1.95\lambda_0$ $L_1 = W_1 = 25.4$ mm

The variations of H-plane beamwidth (HP_H) with S/λ_0 are given in Fig. 3 for different d/λ_m values, which show damped sinusoidal dependence on S/λ_0, the damping being higher at larger S/λ_0 and d/λ_m. All curves show minima at $S/\lambda_0 = n/2$ and maxima at $S/\lambda_0 = (2n+1)/4$. The curve for $d/\lambda_m = 0.52$ apparently shows continuous decrease in lobewidth with increase in S/λ_0. The observed maxima and minima with respect to S/λ_0 appear to be due to the interference effects in spacer region. Similar trends are observed for variations with respect to d/λ_m, and for corresponding A_n variations [6].

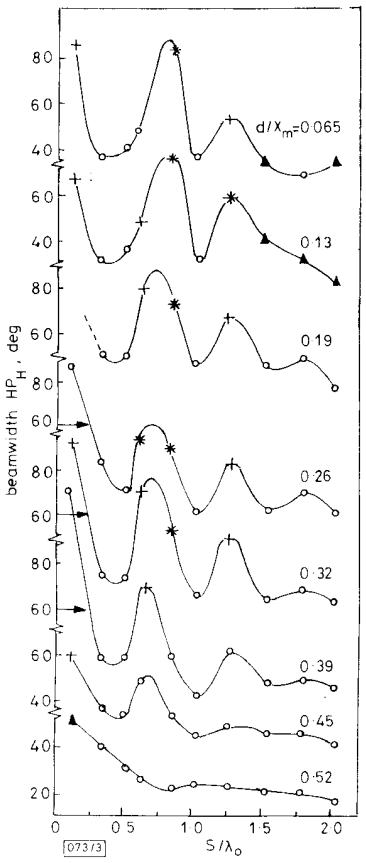

Fig. 3 *H-plane beamwidth variations of rectangular MPA with dielectric PE against S/λ_0 for different d/λ_m*

PE size is 51 × 51 mm^2
▲, + and ✱ indicate successively higher levels of distortions in observed patterns

As can be seen from Table 1 the range of variation of lobewidth is from 18 to 125°; hence the data [6] can be used to choose the required beamwidth of MPA with proper choice of PE parameters.

The gain is enhanced by use of a dielectric PE with higher S and d (Table 1) which acts as a secondary parasitic antenna. The main difference from a metallic parasite [2, 3] is the transmission of part of the radiated power through the dielectric PE in addition to that from the sides of the PE.

Conclusions: The experimental results indicate that gain of a single microstrip patch antenna can be considerably enhanced by using spaced superstrate as the parasitic element. The beamwidth reduces to 18° in both the planes from about 60 and 90° in the H and E planes, respectively. The beamwidth of the antenna can be varied over a wide range from 18 to 125° with proper choice of parameters, although the variations are oscillatory in nature due to interference effects.

Acknowledgments: The authors would like to thank S. A. Gangal and R. C. Aiyer for their kind help during the work, and USIC of this University for fabrication of the positioner.

17th October 1991

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HOT-CARRIER RELIABILITY IN DOUBLE-IMPLANTED LIGHTLY DOPED DRAIN DEVICES FOR ADVANCED DRAMs

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Indexing terms: Semiconductor devices and materials, Integrated circuits, Memories

Hot-electron degradation in short-channel (0·50 μm and 0·83 μm) double-implanted lightly doped drain (DI-LDD) devices was characterised using DC stress tests. Compared to lightly doped drain (LDD) devices of the same effective channel length L_{eff}, the measurements indicate that channel hot-electron injection is more prevalent in devices with the p^+-pocket implant due to a higher peak channel electric field. Degradation is more severe in both the drain current and transconductance. However, an improvement in short-channel effects was seen in DI-LDD devices over LDD devices. For the same L_{eff}, the punch-through voltage was higher and the subthreshold swing lower for the DI-LDD devices.

There is considerable concern about the reliability of submicrometre devices, particularly for advanced dynamic random access memories (DRAMs), as channel lengths are dramatically reduced in the continued scaling of very large scale integrated (VLSI) circuits. Hot-electron induced instability, resulting in threshold voltage shifts and reduction in transconductance and drive currents, is a major concern in scaled metal–oxide–semiconductor (MOS) devices. The driving force behind hot-electron induced degradation is the maximum or peak channel electric field E_m located near the drain region. Lightly doped drain-source (LDD) structures have been successfully used to suppress this electric field [1–4]. However, without appropriate scaling of the supply voltage, the off-state leakage current is still a potential problem, particularly in submicrometre devices.

Double-implanted lightly doped drain-source (DI-LDD) structures have been proposed to improve short-channel effects and increase the punch-through voltage of submicrometre devices [5, 6]. A p^+ pocket or halo implant decreases the drain depletion width, thereby increasing the punch-through voltage V_{pt} and decreasing the short-channel threshold voltage falloff. It has been suggested [7] that extremely small structures (0·2–0·3 μm) can be obtained by using DI-LDD structures. However, the impact of the halo implant on hot-carrier reliability has not been fully investigated. We present detailed findings pertinent to hot-carrier and short channel effects of 0·50 and 0·83 μm devices processed with both LDD and DI-LDD techniques for advanced DRAMs.

Test procedures: n-channel LDD MOS field-effect transistors (MOSFETs) are built with a conventional twin-well complementary MOS (CMOS) technology including a boron punch-through implant to minimise short-channel effects. After gate etch, a 150 nm thick oxide layer is deposited by low pressure chemical vapour deposition (LPCVD), followed by a $1{\cdot}5 \times 10^{13}\,cm^{-2}$ phosphorus LDD implant at 120 keV. The oxide layer is then densified with a 5 min wet oxidation at 907°C. Finally, a second 300 nm thick oxide layer is deposited, dry etched to form a spacer, then followed by a $9 \times 10^{15}\,cm^{-2}$ arsenic source/drain implant at 30 keV. The n-channel DI-LDD devices are built with the same process except that the punch-through implant is replaced with a $3 \times 10^{12}\,cm^{-2}$ selfaligned boron halo implant at 50 keV performed immediately after the gate definition. This boron implant effectively reduces off-state leakage currents by creating a selfaligned p halo around the LDD structure. In addition, all the devices in our study received various annealing steps that simulate the thermal treatments encountered in advanced stacked DRAM manufacturing steps. We used devices with an effective channel length L_{eff} of 0·50 and 0·83 μm, an effective gate width of 25 μm, and an oxide thickness of 20 nm. No substantial difference was observed in L_{eff} values for the same channel length between DI-LDD and LDD devices. The junction depth was 0·37 μm, and the channel doping was $3 \times 10^{16}\,cm^{-2}$.

Accelerated DC stress tests, with drain voltage V_d ranging from 7·5 to 8·5 V and gate voltage V_g set at maximum substrate current I_{sub}, were conducted to evaluate the hot-electron degradation. A 10% degradation in both transconductance G_m and drain current I_{ds} was selected as the failure criterion. I_{ds} was measured at $V_d = 0{\cdot}1$, $V_g = 5{\cdot}0$ V as the degradation in the linear region was much more severe than that in the saturation region. Minimal degradation was observed in V_t and therefore the data are not reported.

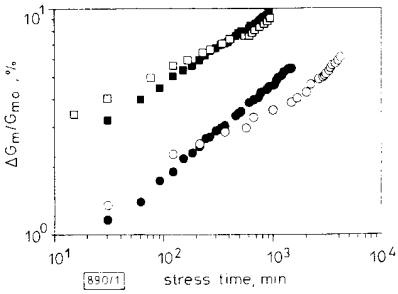

Fig. 1 *Percentage degradation in G_m as function of stress time*
Stress level: 0·5 μm, $V_d = 7{\cdot}75$ V; 0·83 μm, $V_d = 8{\cdot}25$ V
■ 0·5 μm, DI-LDD
● 0·5 μm, LDD
□ 0·83 μm, DI-LDD
○ 0·83 μm, LDD

Results and discussion: Fig. 1 shows the degree of degradation in G_m as a function of stress time on both 0·50 and 0·83 μm devices stressed at 7·75 and 8·25 V, respectively. It is seen that ΔG_m follows a power-law relationship; it increases with t^n where t is the stress time. The parameter n was extracted from the plots and found to range between 0·38–0·45 which is slightly lower than values (0·50–0·75) reported by Hu *et al.* [8]. From Fig. 1 it is quite apparent that the DI-LDD devices (0·5 μm and 0·83 μm) degrade much faster than the LDD devices. The measured peak I_{sub} values (seen in Table 1) were much higher for the DI-LDD devices. A 2-D simulation of the channel electric field distribution for both LDD and DI-LDD devices was conducted using SUPREM-4 and PISCES-2B. The maximum field point for the LDD devices was observed right at the drain edge, and for the DI-LDD devices approximately 0·05 μm from the drain edge inside the n region underneath the gate. From an E_m location point of view, both device types would tend to indicate minimal electron injection into the spacer oxide. Spacer-induced degradation by injected carriers can increase the parasitic resistance of the lightly doped regions and result in reduction in current drive capability [9]. However, the DI-LDD devices exhibited a larger magnitude in E_m than the LDD devices at identical stress levels, as