TRANSISTER BIASING

The main application of transistor is in amplification. The process of raising the strength of weak signal without any change in its general shape is reffered to as "faithful amplification".

For faithful applications three conditions must be satisfied
i) the EB junction should be forward biased.
ii) the CB junction should be reverse biased.
iii) there should be proper zero signal collector current

TRANSISTOR BIASING :- The proper flow of zero signal collector current and the maintanance of proper CE voltage during the passage of signal is known as Transistor Biasing.

BIAS STABILIZATION :- The operating point does not remain fixed even if it is properly biased due to various reasons :-

(1) **Temperature Dependance of I_C :-** The collector current increases with the rise in temperature.

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$I_C = \beta I_B + I_{CEO} \qquad * I_{CO} = I_{CBO}$$

$$\because I_{CEO} = (1+\beta) I_{CBO}$$

(a) I_{CO} doubles for every rise of 10°C (leakage Current)
(b) β increase with temperature rise
(c) V_{BE} decreases by 2.5 mV per °C

2) **Individual Variations :-** When the transistor is replaced by another transistor of same type, the value of β and V_{BE} are not exactly same. Hence the operating point will change.

3) **THERMAL RUNAWAY :-** Flow of current in the collector circuit produced heat at the collector junction. This increases the temperature. More minority carriers are generated in the base collector region. The leakage current I_{CBO} increases

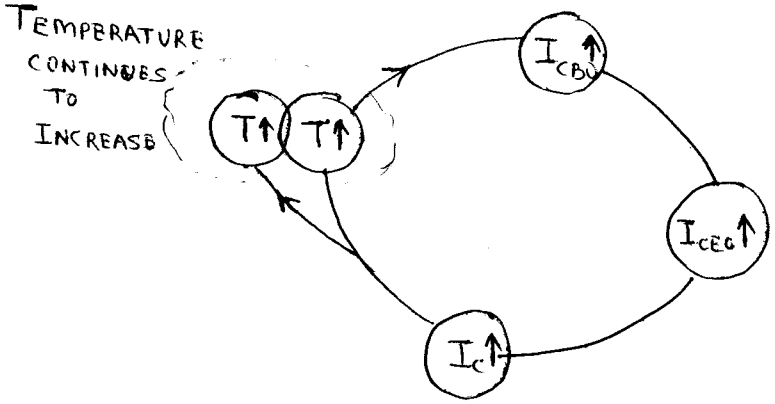
$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad ; \quad I_{CEO} = (1+\beta) I_{CBO}$$

I_{CEO} and I_C will increase as I_{CBO} is increasing

The increase in I_C will increase the temperature which in turn increases I_{CBO}. Such a cumulative increase in I_C will ultimately shift the operation point into saturation region. The transistor can even burn. This situation is called "THERMAL RUNAWAY".

Ge Transistor between 60° to 100°C

Si transistor between 150°C to 225°C



Explanation of Thermal Runaway

TWO TECHNIQUES FOR STABILIZATION

STABILIZATION TECHNIQUES

This technique consists use of a resistive biasing circuit which permits such a variation of base current I_B as to maintain I_c almost constant inspite of variation of I_{co}, β, V_{BE}

COMPENSATION TECHNIQUES

In this technique temperature sensitive devices such as diodes, transistor thermister etc. are used. Such devices produce compensating voltages and current in such a way the operating point is maintained stable.

STABILITY FACTOR (S)

It is defined as the rate of change of collector current I_c with respect to the reverse saturation current I_{co}, keeping β and V_{BE} constant.

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}} \Bigg|_{\beta, V_{BE} = \text{Constant}}$$

The value of 'S' should be kept as small as possible, higher the value more is unstability. The lowest value of 'S' is unity. Closer the value of 'S' to unity, lesser will be the variation of operating point with temperature.

2) Stability factor (S_β): This is defined as the rate of change of I_c with β keeping I_{co} and V_{BE} constant,

$$S_\beta = \frac{\partial I_c}{\partial \beta} \approx \frac{\Delta I_c}{\Delta \beta} \Bigg|_{I_{co}, V_{BE} = \text{Constant}}$$

3) Stability factor (S_V) :- The rate of change of I_c with V_{BE}, keeping I_{co} and β constant.

$$S_V = \frac{\partial I_c}{\partial V_{BE}} \Bigg|_{I_{co}, \beta = \text{Constant}}$$

Expression for Stability factor (S)

When a transistor is biased in the active region of its characteristics then its I_c

$$I_c = \beta I_B + (1+\beta) I_{co}$$

differentiating w.r.t I_c considering β = constant

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{1}{S} \qquad \left[\because 1/S = \frac{dI_{co}}{dI_c} \right]$$

$$1 - \beta \frac{dI_B}{dI_c} = (1+\beta) \frac{1}{S}$$

$$\boxed{S = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_c}}}$$

Expressions for Stability factor S_β :-

$$I_c = \beta I_B + (1+\beta) I_{CO}$$

differentiating the above equation w.r.t I_c keeping I_{CO} = Constant

$$1 = \beta \frac{dI_B}{dI_c} + I_B \frac{d\beta}{dI_c} + I_{CO} \frac{d\beta}{dI_c}$$

$$1 - \beta \frac{dI_B}{dI_c} = \frac{d\beta}{dI_c} (I_B + I_{CO})$$

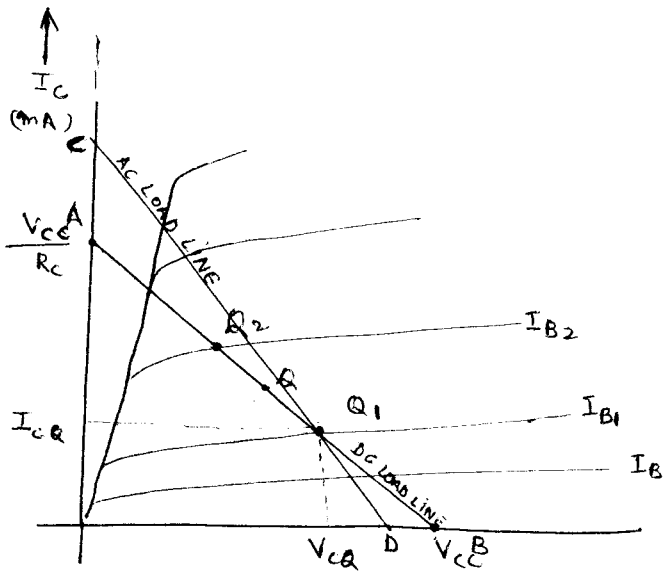
$$\left[\because \frac{d\beta}{dI_c} = \frac{1}{S_\beta} \right]$$

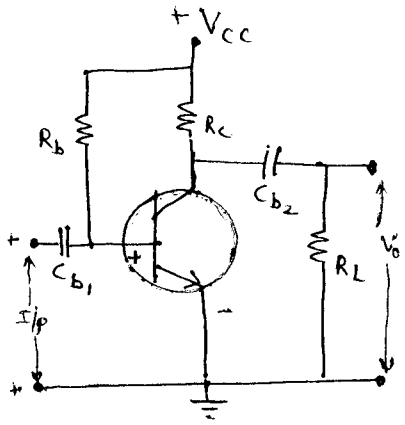
$$\boxed{S_\beta = \frac{I_{CO} + I_B}{1 - \beta \frac{dI_B}{dI_c}}}$$

OPERATING POINT

To use transistor as an amplifier, It is used in active Region. To establish an operating in this region it is necessary to provide appropiate direct potentials and currents, using external sources. Once an operating point in this region, time-varying excursions of the input signal should cause an output signal of the same wave form. If the output signal is not a faithful reproduction of the input signal for example, if it is clipped on one side, the operating point is unsatisfactory and should be relocated on the collector characteristics..

Static Load line (DC load line) :- (AB) The Quiescent Collector current and voltage are obtained by drawing dc loadline corresponding to R_C through the point $i_c = 0$, $V_{CE} = V_{CC}$, as shown in figure.





C.E Characteristics

If $R_L = \infty$ and if the input signal is large and symmetrical, we must locate the operating point Q_1 at the loadline. In this way the collector voltage and current may vary approximately symmetrically around Q-point values V_{CQ} and I_{CQ}.

DYNAMIC LOAD LINE (AC load line) :- If $R_L \neq \infty$ however a dynamic (AC) load line must be drawn. Since we have assumed that at the signal frequency, C_{b_2} acts as a short circuit, the effective load R_L' at the collector is R_c in parallel with R_L. The dynamic load line must be drawn through the operating point Q_1 and must have a slope corresponding to $R_L' = R_c // R_L$. This load line is AC load line (CD).