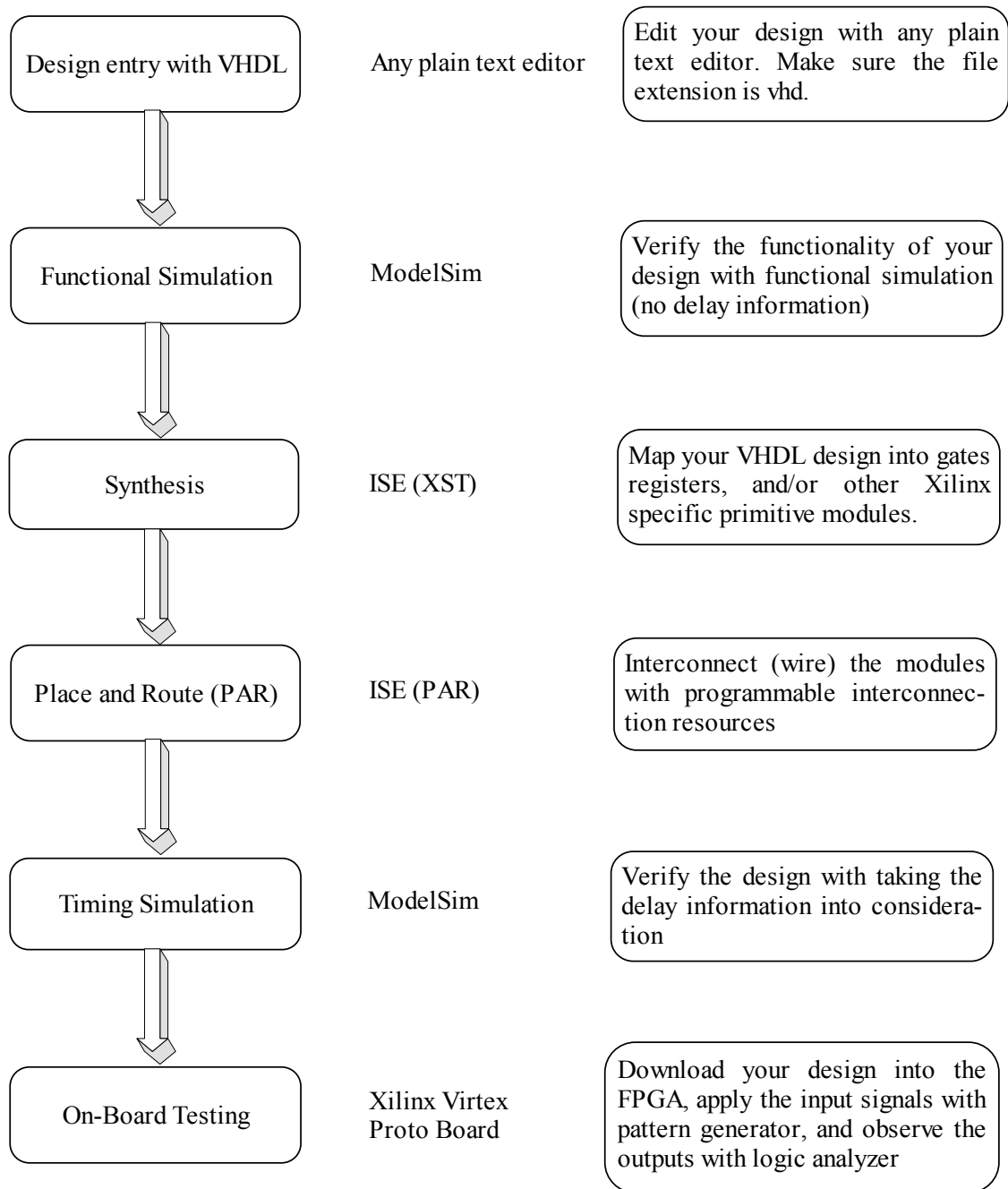


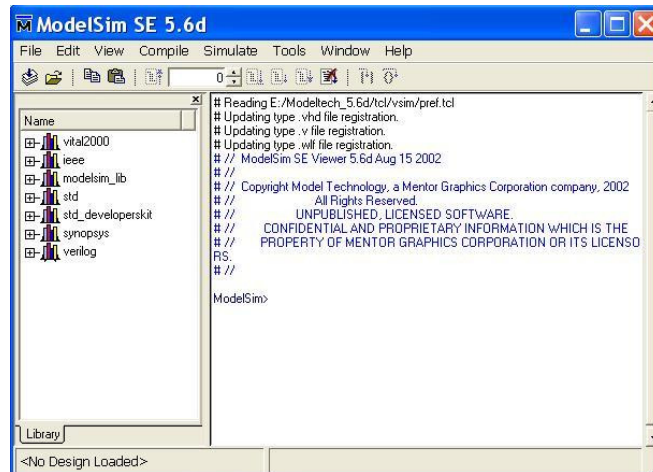
Introduction to the Flow of FPGA-Based Hardware Design



Functional Simulation

▼ Save all design files in your working directory.

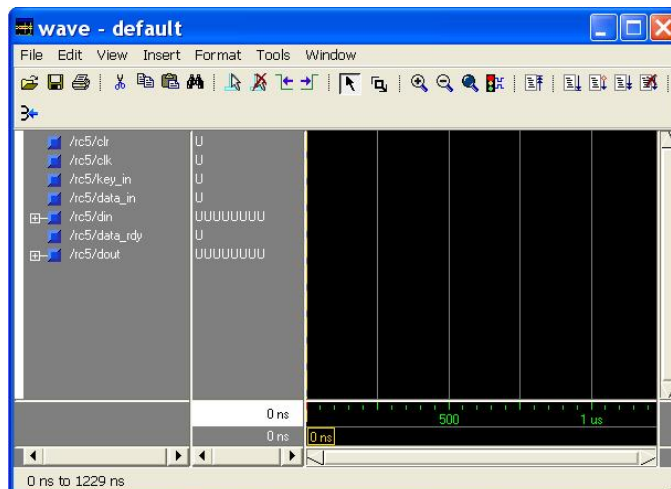
1. Launch ModelSim by double clicking the icon on the desktop, ModelSim console window appears as shown below.



2. Execute the following commands in sequence (in ModelSim console window).

```
cd {your working directory}
vlib work
vcom rc5_pkg.vhd key_exp.vhd rc5_enc.vhd rc5_dec.vhd rc5.vhd
vsim rc5
view wave
add wave clr clk key_in data_in din data_rdy dout
```

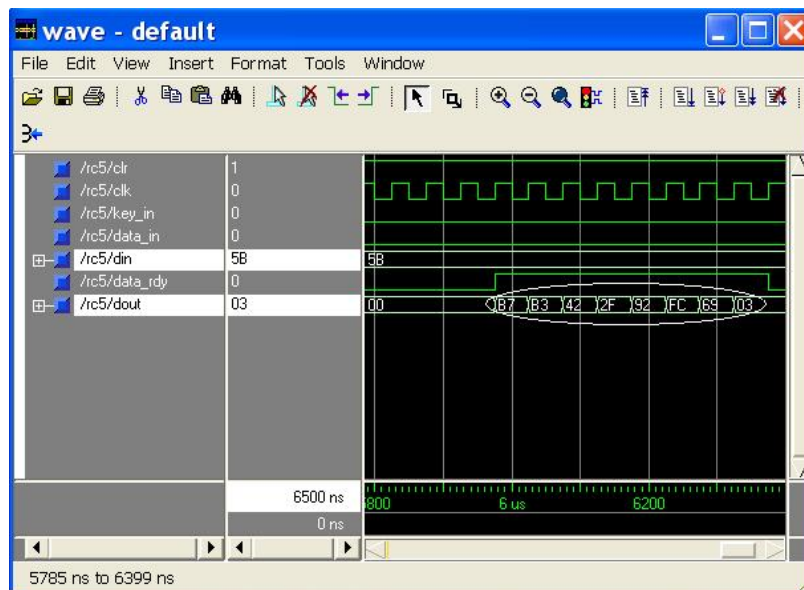
You will see a waveform window appears, as shown below.



3. Continue to execute the following commands in sequence.

```
force clr 0 0, 1 200
force clk 0 0, 1 25 -repeat 50
force enc 1 0
force key_in 0 0, 1 200, 0 300
force data_in 0 0, 1 4900, 0 5000
force din 16#00 0, 16#E7 200, 16#48 250, 16#33 300, 16#78 350, 16#2F 400, 16#0F 450, 16#EB 500,
16#5A 550, 16#BB 600, 16#69 650, 16#B1 700, 16#D7 750, 16#87 800, 16#67 850, 16#C1 900,
16#8D 950, 16#AC 4950, 16#13 5000, 16#C0 5050, 16#F7 5100, 16#52 5150, 16#89 5200, 16#2B
5250, 16#5B 5300
run 6500
```

4. Verify the simulation result, compare it to RC5 document.

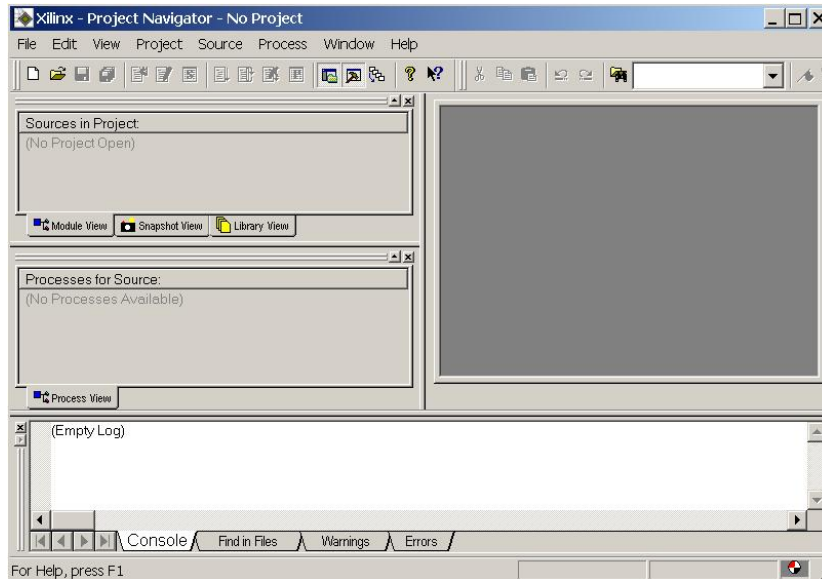


Synthesis and PAR (Place and Route)

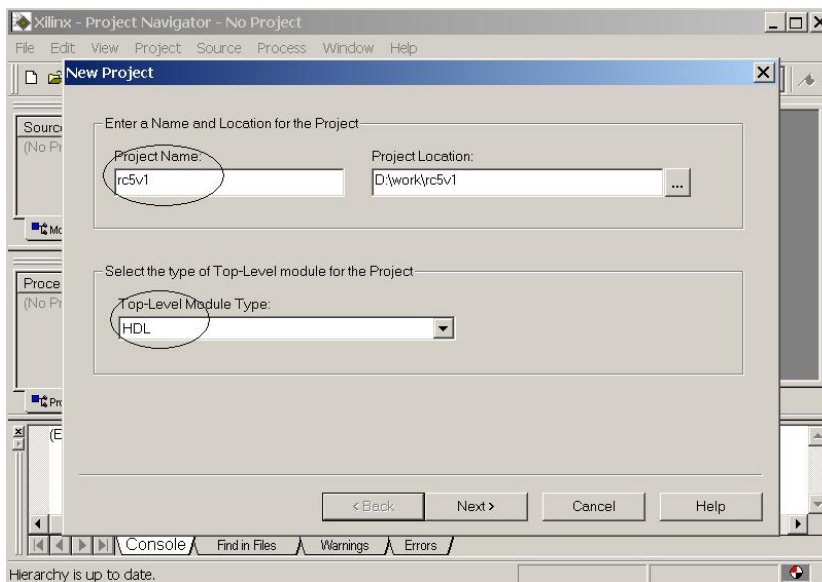
▼ These two steps are done with Xilinx ISE (Integrated Synthesis Environment).

1. Launch Xilinx ISE by double clicking the *Project Navigator* icon on the desktop.

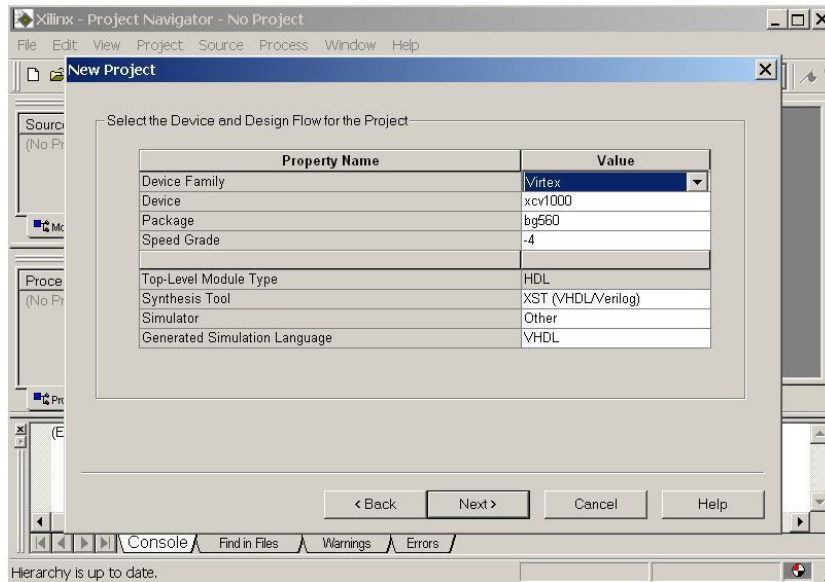
Xilinx *Project Navigator* window appears as shown below.



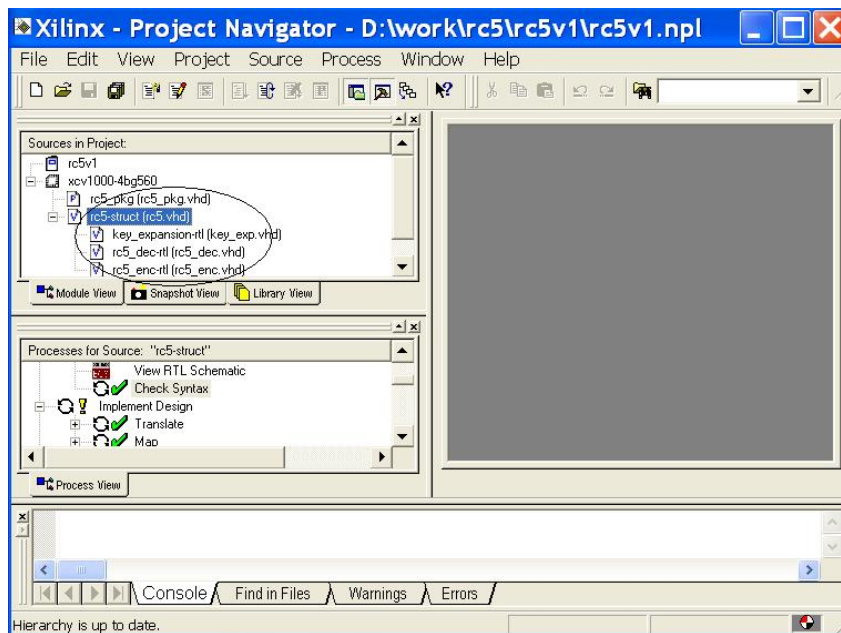
2. Select *File->New Project...* You will see the *New Project* window. Name the project as “rc5v1”, set the project location, and select HDL as the *Top-level Module Type*. Click *Next*.



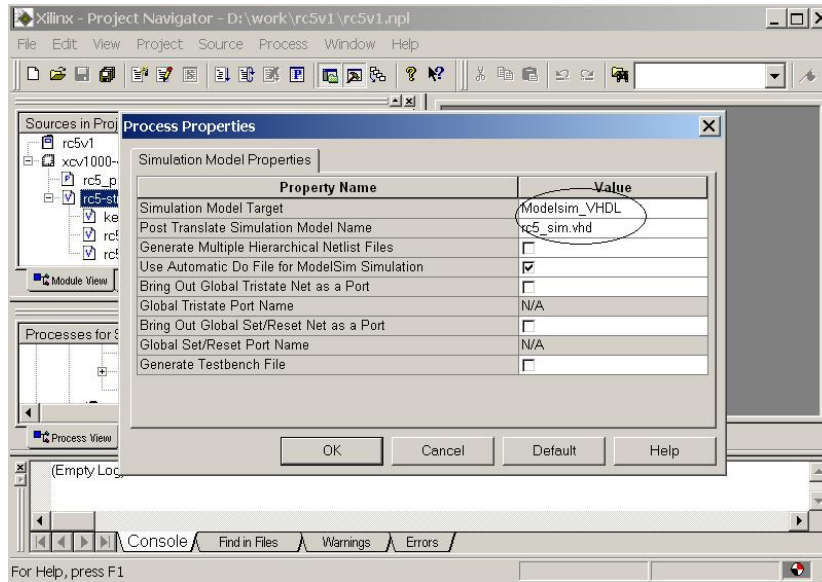
3. Select the *Device and Design Flow for the Project*, as shown in the figure below. Add all source files, finish remaining steps to create a new project.



4. When the new project is created successfully, you will see the following window.



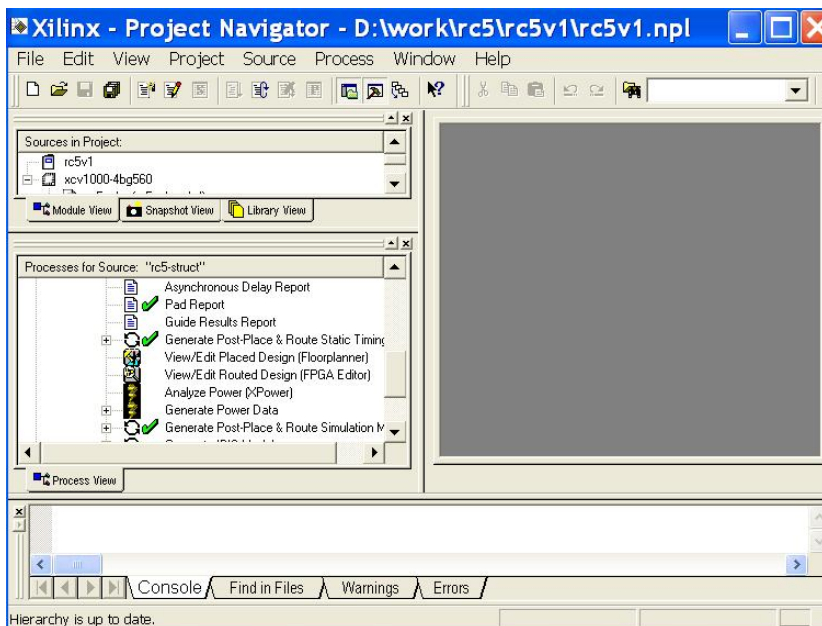
- In the *Sources in Project* column, select the top-level design file “rc5-struct (rc5.vhd)”.
- In the *Process for Source* column, flatten the *Implement Design* tree, select *Generate Post-Translate Simulation Model*. Right-click it, select *Properties...* You will see the window below.



5. Set the *Simulation Model Target* to Modelsim_VHDL. ModelSim is the simulator we use. Name the simulation model as “rc5_sim.vhd”

6. Double click *Generate Post-Translate Simulation Model*, the synthesis and PAR processes will start.

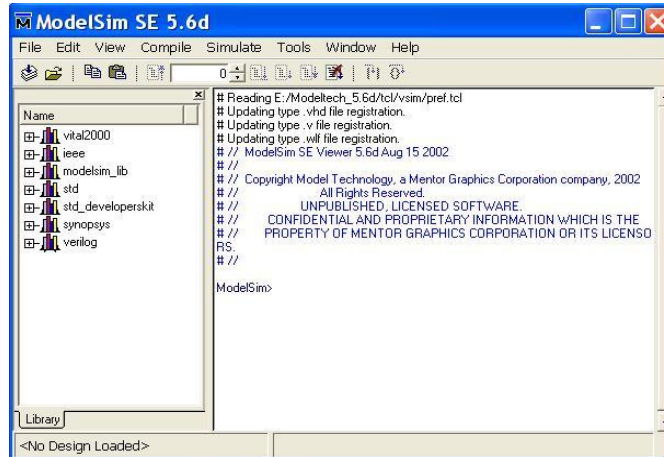
If everything goes smoothly, you will see the following window. The check marks mean these steps finish successfully.



Timing Simulation

▼ Make sure rc5_sim.vhd and rc5_sim.sdf are in your working directory.

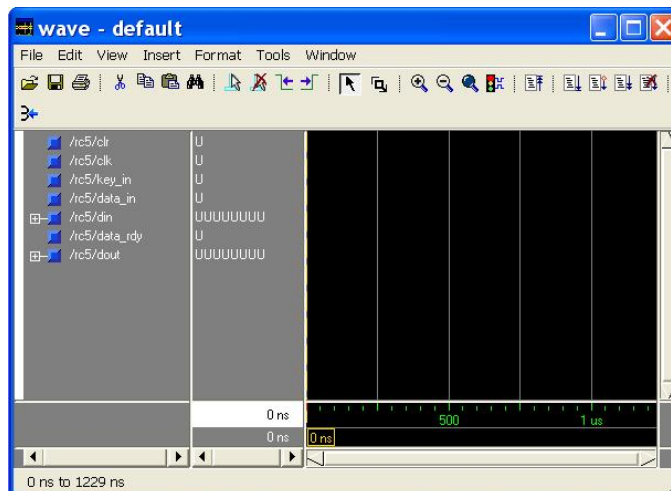
1. Launch ModelSim by double clicking the icon on the desktop, ModelSim console window appears as shown below.



2. Execute the following commands in sequence (in ModelSim console window).

```
cd {your working directory}
vlib work
vmap simprim {modelsim dir}/xilinx/simprim
vcom rc5_sim.vhd
vsim -sdftyp /= {your working directory}/rc5_sim.sdf work.rc5(structure)
view wave
add wave clr clk key_in data_in din data_rdy dout
```

You will see a waveform window appears, as shown below.



3. Continue to execute the following commands in sequence.

```

force clr 0 0, 1 200
force clk 0 0, 1 25 -repeat 50
force enc 1 0
force key_in 0 0, 1 200, 0 300
force data_in 0 0, 1 4900, 0 5000
force din 16#00 0, 16#E7 200, 16#48 250, 16#33 300, 16#78 350, 16#2F 400, 16#0F 450, 16#EB 500,
16#5A 550, 16#BB 600, 16#69 650, 16#B1 700, 16#D7 750, 16#87 800, 16#67 850, 16#C1 900,
16#8D 950, 16#AC 4950, 16#13 5000, 16#C0 5050, 16#F7 5100, 16#52 5150, 16#89 5200, 16#2B
5250, 16#5B 5300
run 6500

```

4. Verify the simulation result, compare it to RC5 document.

