Synopsis Report

1. Subject	:	Electronics
2. Name of the Student	:	Mr. Sunoj P. Raikar
Qualification	:	
Address	:	
3. Research Guide	:	Dr. R.K. Kamat
Qualification	:	M.Sc. Ph.D.
Address	:	Reader in Electronics, Department of Electronics, Shivaji University, Kolhapur – 416 004
4. Title of Proposed Thesis	:	Hardware Software Codesign for Real Time Hetregenous Embedded Systems

Hardware Software Codesign for Real Time Hetregenous Embedded Systems

Introduction:

Embedded Systems are now omnipresent: from cellular phones to pagers, from microwave ovens to PDAs, almost all the devices we use are controlled by embedded systems. Many embedded systems have to fulfill strict requirements in terms of performance and cost efficiency. Intelligent and self-organizing embedded computing systems capable of interacting with each other and their environment are expected to become the major consumer of communication bandwidth in the near future. Enabled by the recent advances in engineering, these systems will find their way into a new, rich and diverse set of applications like never before. One of the main challenges of above mentioned embedded systems is bridging the gap between the state of the art engineering technologies and their corresponding applications. This calls for innovative interdisciplinary systems research with positive impact in other fields. The advances in silicon technologies predicted by Moore's Law are maturing to a level capable of facilitating "orthogonal spikes of progress" in other fields in the sciences by enabling the creation of new tools and approaches in ways that were not possible before.

Many embedded systems have requirements that differ significantly both in details and in scope from desktop computers. In particular, the demands of the specific application and the interface with external equipment may dominate the system design. Also, long life-cycles and in some cases extreme cost sensitivity require more attention to optimization based on these goals rather than maximizing the computational throughput.

Embedded Systems for Sensors and Actutaors:

Presently we are in an era of massive embedding of digital technology and microcontrollers for sensors, actuators which has witnessed an unprecented improvement in their functinoning. The control is now implemented by programming the microcontrollers to react to stimuli from the environment with a response that make the artifact function as intended. Examples include an airbag controller of a car, a remote controller for an audio/video device, and a game computer. A number of microcontrollers might be included in a system to obtain the desired functionality. Netwrked embedded systems are more relevant for the sensors as their web will be the most common system in near future.

Hwever in order to obtain maximum throughput in a sensor sensor web their interfacing with microcontrollers is not enough. Emerging designs are now based on heterogeneous architectures that integrate multiple programmable processors and dedicated hardware components. For it to gain broad acceptance, the differences between heterogeneous processing architectures and conventional systems have to be appreciated. Conventional computers are based on fixed processor architectures performing different functions according to what instructions are given. The underlying hardware on which the software must execute is fixed. In contrast, heterogeneous processing computers are essentially composed of the raw building blocks of logic-based systems. These can be harnessed in any way required to complete the task. As a result, heterogeneous computers are almost completely flexible and scalable at all levels, and hence, far more suited to almost any task.

Research Problem:

The focus of the research problem is modeling, simulation, and design of concurrent, real-time, autonomous embedded systems dedicated to sensor webs. Networks of sensors is a collection of dynamical systems that react to and interact with their environment. The individual sensors in the network are configured in the active or passive mode depending on the need. This kind of reconfigurable operation helps in minimizing the use of resources like memory, power etc. and ensures ovarall maximum throughput for the sensor system.

As the sensor webs bulk up in complexity and move toward distributed software environments, they are in need of running multiple compute nodes within the same system to form a heterogeneous computing environment. And as systems with multiple processors grow more common, the issues surrounding heterogeneous computing are moving to the forefront. The proposed research work will investigate hardware and software issues pertaining to hetregenous multiprocessor embedding system dedicated for sensor web.

The research work will be concentrated on assembly of concurrent components by using reconfigurable processing blocks like FPGA’s and CPLD’s. It is planned to interface these reconfigurable digitial blocks to suitable family of microcontrollers like Atmel, PIC and ARM. The key underlying principle in the research work will be the use of well-defined models of computation that govern the interaction between these processors. Co-processing aspects will be impelmented in this networked system of hetregenous processors by developing suitable protocols and device drivers.

Investigations will also be undertaken on aspects of scheduling and communication as well as developing a tiny operating system (RTOS) for the above mentioned hetregenous embedded real-time multiprocessor system. The main abstraction exported by the OS to the application programme will be interms of Microcells. These Micorcells will act as the equivalent of tasks in traditional operating systems. They will begin their life-cycle as inactive software components with a specific application-dependent function (implemented by microcell code). They may initially reside on randomly selected host nodes until activated and will be activated by stimuli in the environment, as well as by events in the computing system (such as specific changes in resource utilization). Once a microcell is activated, the stimulus of interest can cause it to perform self-replication, migration, or grouping. The mechanisms for micorcell replication, migration, and coordination are supplied by the underlying software infrastructure. It is also planned to develop a TCP/IP which will be integrated to this tiny RTOS to facilitate communication with the internet.

Although the above mentioned hetregenous embedded system is planned as an universal interface for any sensor system, the same will be tested for marine sensors.

Significance of Research Work:

The complex issues of heterogeneous embedded systems pose unique hardware and software design challenges. The processors employed have diversified architectural considerations and spread across multiple processing nodes, to serve specialized purposes. Complicating matters further, these processors typically run different and incompatible operating systems. Part of that's due to reasons of legacy, but often the various processing nodes have different purposes and therefore have distinct operating system needs.

The main contribution of this research work will be the real-time network coordination and control middleware that abstracts, controls, and ultimately guarantees the desired behavior of large unreliable networks composed of sensors and actuators. The networks of sensors and actuators differ from the traditional networked systems in that, in aggregate, they must be highly adaptive, must cope with high rates of component failure, mobility, and reconfiguration, and must export a highly configurable set of parameterized services that may involve coordinating a rich set of sensors and actuators in the network core.

Literature Survey:

1. Buck, J.T. "A Dynamic Dataflow Model Suitable for Efficient Mixed Hardware and Software Implementations of DSP Applications", in Third International Workshop on Hardware/Software Codesign. 1994. Grenoble, France: IEEE Computer Society Press, 165-172.

2. Calvez, J.P. and D. Isidoro. "A Codesign Experience with the MCSE Methology", in Third International Workshop on Hardware/Software Codesign. 1994. Grenoble, France: IEEE Computer Society Press, 140-147.

3. Caron, O. and e. all. "New architectures for smart cards: the OCEAN approach", in Third International Workshop on Hardware/Software Codesign. 1994. Grenoble, France: IEEE Computer Society Press, 148-155.

4. Coelho, C.N. and e. all. "Redesigning Hardware-Software Systems", in Third International Workshop on Hardware/Software Codesign. 1994. Grenoble, France: IEEE Computer Society Press, 116-123.

5. D'Ambrosio, J.G. and X. Hu. "Configuration-Level Hardware/Software Partitioning for Real-Time Embedded Systems", in Third International Workshop on Hardware/Software Codesign. 1994. Grenoble, France: IEEE Computer Society Press, 34-41.

6. Y. Xu, J. Heidemann, and D. Estrin, Adaptive Energy-Conserving Routing for Multihop Ad Hoc Networks, USC/Information Sciences Institute, October 2000

7. A. Cerpa and D. Estrin, ASCENT: Adaptive Self-Configuring sEnsor Networks Topologies, INFOCOM'02, June 2002

8. Chen, K. Jamieson, H. Balakrishnan, and R. Morris, Span: an Energy-Efficient Coordination Algorithm for Topology Maintenance in Ad Hoc Wireless Network, ACM Wireless Networks Journal, 8, 5, 481-494, September 2002

9. Y. Xu, S. Bien, Y. Mori, J. Heidemann, and D. Estrin., Topology Control Protocols to Conserve Energy in Wireless Ad Hoc Networks, CENS Technical Report 0006, January 2003

10. Wen-Zhan Song, Yu Wang , Xiang-Yang Li, Localized Algorithms for Energy Efficient Topology in Wireless Ad Hoc Networks, MobiHoc, May 2004

11. Anindya Basu, Brian Boshes , Sayandev Mukherjee, Sharad Ramanathan, Network Deformation: Traffic-Aware Algorithms for Dynamically Reducing End-to-end Delay in Multihop, MobiCom, September 2004

12. S. Park, A. Savvides, and M.B. Srivastava., SensorSim: A Simulation Framework for Sensor Networks., MSWiM'00, August 2000

13. P. Levis, N. Lee, M. Welsh, and D. Culler., TOSSIM: Accurate and Scalable Simulation of Entire TinyOS Applications., The First ACM Conference on Embedded Networked Sensor Systems (Sensys03), November 2003

14. Benjamin Greenstein, Eddie Kohler, Deborah Estrin, A Sensor Network Application Construction Kit (SNACK), ACM Sensys, November 2004

15. Jonathan Hui, David Culler, The Dynamic Behavior of a Data Dissemination Protocol for Network Programming at Scale, ACM Sensys, November 2004

16. Victor Shnayder, Mark Hempstead, Bor-rong Chen, Geoff Werner-Allen, Matt Welsh, Simulating the Power Consumption of Large-Scale Sensor Network Applications, ACM Sensys, November 2004

17. Jason Hill, Robert Szewczyk, Alec Woo, Seth Hollar, David E. Culler and Kristofer S. J. Pister. System Architecture Directions for Networked Sensors. In Architectural Support for Programming Languages and Operating Systems, pages 93-104, 2000.

18. J. Kahn, R. Katz and K. Pister. Emerging Challenges: Mobile Networking for `Smart Dust'. J. Comm. Networks, 2(3):188-196, 2000.

19. Deborah Estrin, Ramesh Govindan, John S. Heidemann and Satish Kumar. Next Century Challenges: Scalable Coordination in Sensor

Networks. In Mobile Computing and Networking, pages 263-270, 1999.

Methodology / Laboratory Work (Experimental / Theoretical):

The proposed research work will be divided into several phases as follows:

- Simulation using standard open source tools like OMNeT++, ns2, GloMoSim etc.
- Building Hardware comprising of the processors with architecturally diferent orientations.
- Assigning appropriate task of the sensor web to the above mentioned processors.
- Writing device drivers to enable the coprocessing of the nodes
- Developing a tiny OS to facilititate overall working of the system
- Developing or using a suitable TCP/IP stack to enable the communication with internet.
- Testing the system with a sensor bed in industry or in National Institute of oceanography.

Organization of Field Work:

Following places have been identified for the field work:

1. Library of Indian Institute of Science for exensive literature survey on the topic.
2. Prof. Asokan's Laboratory in the Instrumentation Department of Indian Institute of Science for consultation.
3. Centre for Electronics Design and Technology (CEDT) at Indian Institute of Science for Consultation
4. National Institute of Oceangraphy for Literature Survey as well as testing of the hardware.
5. Hyloc Hydrotechnic Pvt Ltd, Belgaum where the testing will be done for the ongoing aircraft project.

Outline of the proposed research work (Time frame):

0 – 6 Months	: Literature Survey, Planning and Consultation with experts.
6-12	: Skill acquisition with respect to tools
12-18	: Months Building Hardware comprising of different microcontrollers and testing software for the same
18-24	: Building systems with FPGA-Microcontroller or CPLD- Microcontroller co-processing.
24-30	: Testing with the sensor array at NIO or Industry
30- 36	: Deveoping tiney OS, Identifying TCP/IP stack, Writing Dissertation

Ph.D. Guide
(Dr. R.K. Kamat)

Ph.D.Student
(S. P. Raikar)