Analog Mixed Signal (AMS) simulator integration in Analog Design Environment (ADE)

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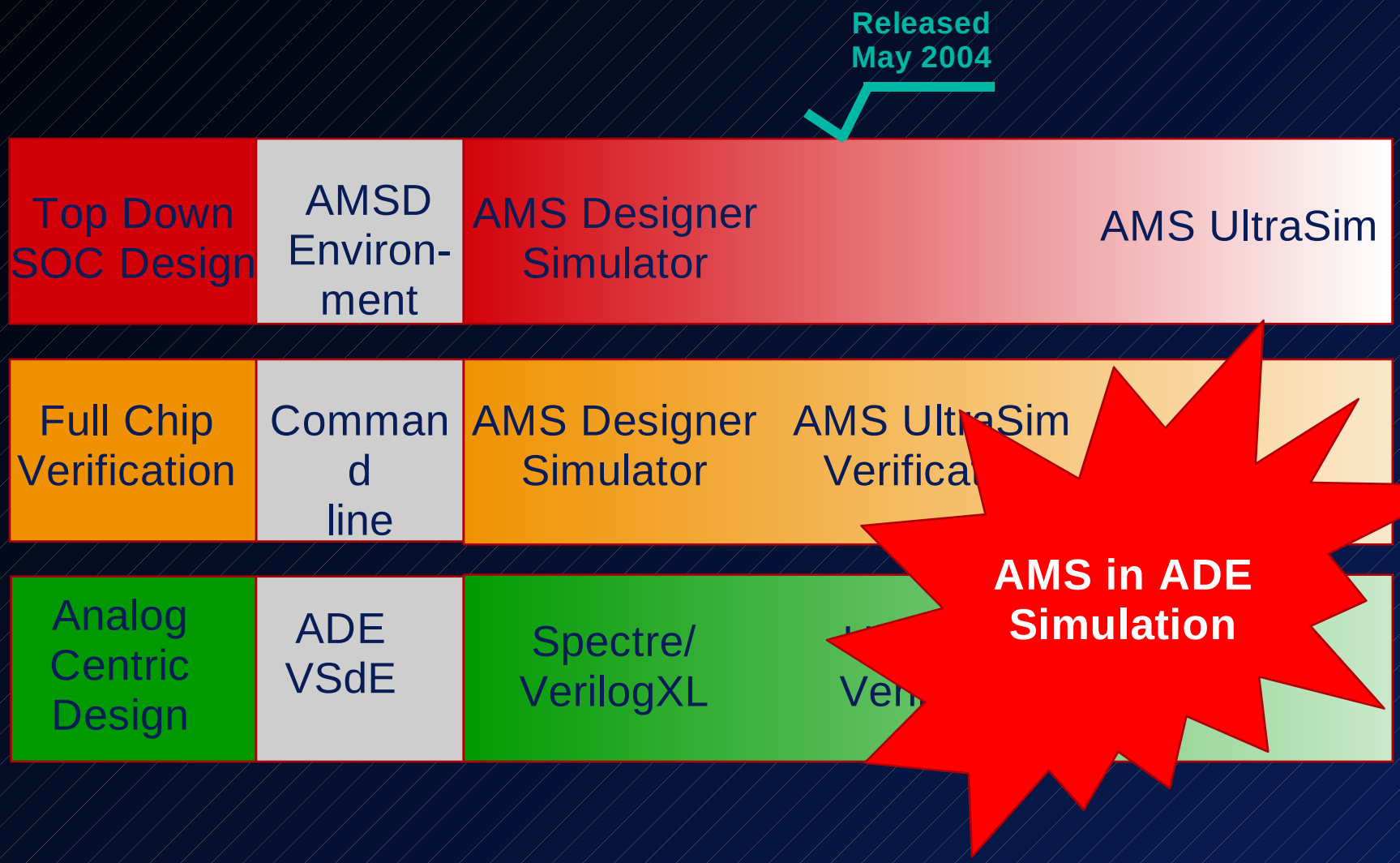
TECCI 2005

cadence

Mixed Signal Simulation Technology

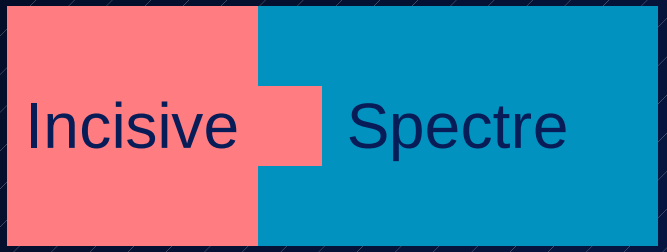


AMS Simulator

High Performance SOC Development and Verification

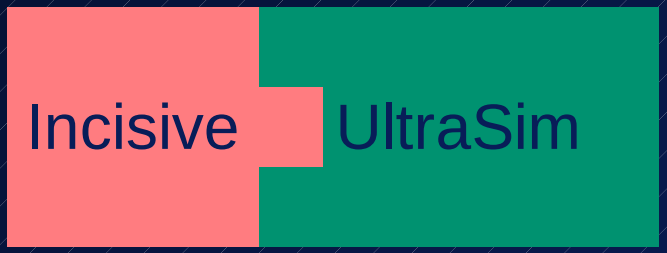
- Dual mode Simulator
- User selects which analog engine to use (for everything analog in the whole design)
- Supports Spectre, SPICE, Verilog-AMS, VHDL-AMS, Verilog-A, Verilog, VHDL in both modes identically
- Identical use models

Spectre Mode



AMS-Spectre

New additional UltraSim mode



AMS-UltraSim

ADE Integration of AMS Simulator

More Convenient Use Model for Mixed Signal Design and Verification

- Next generation, high speed, high capacity simulator integration, via OASIS Technology
- Integration of Eden Cell Based Netlister in DFII
- Targeted for both Big-A/small-d and Big-D/small-a audience
- Mixed Signal support: Analog and Digital simulator support
- Mixed Language Support : Verilog AMS and VHDL AMS
- Mixed Mode support: Accurate Table model/new front end (SFE) support
- Dual Analog Solver support : Spectre(accurate) and UltraSim (fastSpice)

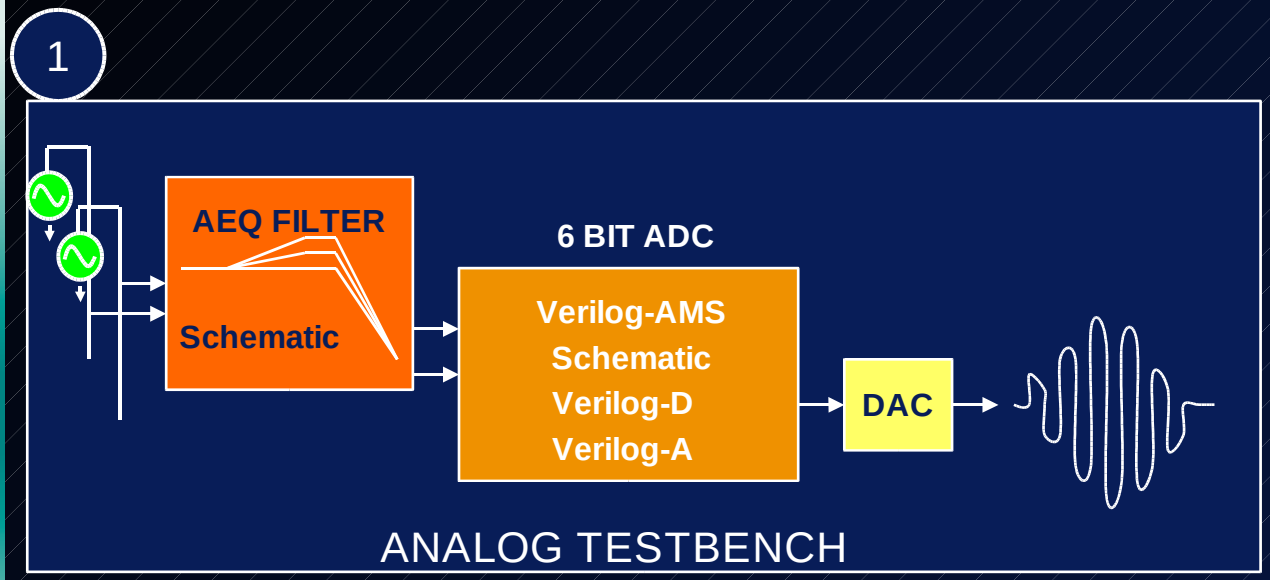
ADE Integration of AMS Simulator (Cont..)

- Classical ADE support : analyses, save states, save/plot, cross-probing
- Integration keeps the major advantages of HED based use model
- Integration of waveform tools - Wavescan, AWD & SimVision
- Incremental and Non-Incremental - Compilation, Elaboration and simulation run support
- Post-processing support for dual data format - PSF and SST2
- Mixed-signal Partitioner, Operating Point Back annotation
- Batch mode scripting simulation support - OCEAN
- ADE Advance Tool support - Parametric Analysis, Distributed Processing, Corners, Optimizer

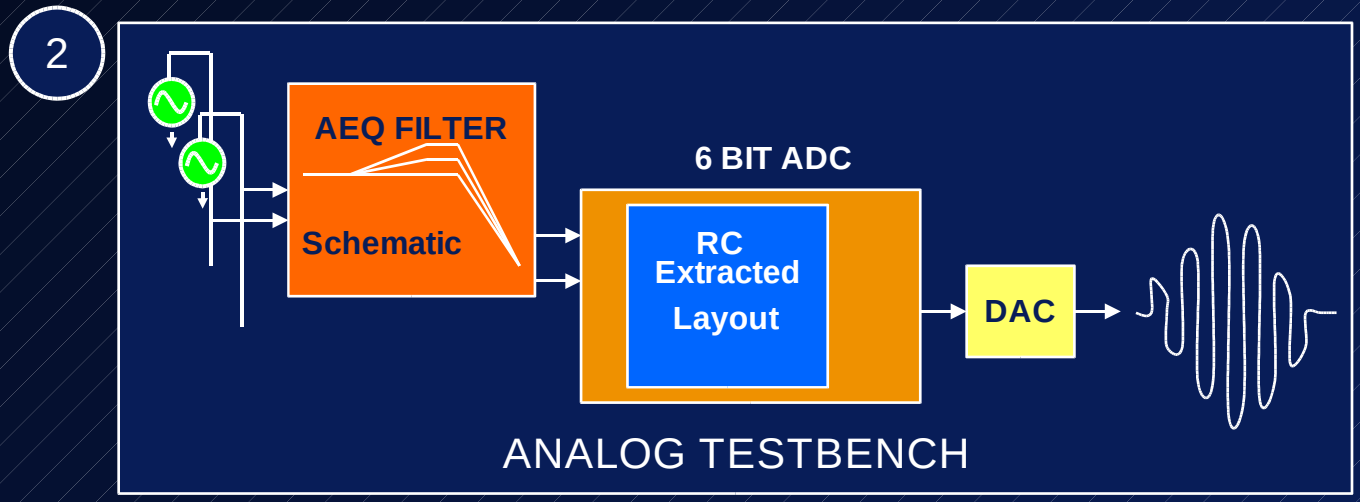
Demo details

- Programmable, differential anti-aliasing filter (AEQ) filtering the front end of a differential 6-bit ADC.
- There are two phases of the demo:
  - Phase 1: Design Validation
    - Schematic level simulation with Accurate analog Spectre solver
    - Display Partition functionality, Wavescan data display.
  - Phase 2: Design Verification
    - Actual schematic level simulation with FastSpice UltraSim solver
    - FastSpice Simulation using an Analog extracted view (from Assura/RCX) & reference layout view

ADC/AEQ Block Authoring Testbench



Analog Testbench consists of a part of 10/100 SOC chip showing ADC/AEQ filter



Summary

- AMS solution enables accurate & high performance mixed signal full chip simulation
- Easy to use accelerated AMS technology in all use models
- Tight integration of high performance analog and high performance digital simulators
- Common device models implementation for all simulators ensures best accuracy

Design and accurately verify your mixed signal designs faster

Demo details (contd.)

- Phase 1: Design Validation
  - Design a differential 6 bit ADC with differential anti-aliasing filter AEQ block on the front end.
  - We will drive our filter with differential signals and filter down the input about -6dB for a differential input to our ADC. We will use a 6 bit DAC on the output of the ADC to reconstruct our differential input stimulus.
  - Verify this graphically with next generation waveform tool - WaveScan.
  - Run initial transient analysis followed by true mixed-signal AC analysis. Design consists of about 400 transistors and 2500 passive components with mostly highly abstracted behavioral models in VerilogAMS.

Demo details (contd.)

- Phase 2: Design Verification
  - Verification phase of the block level design by introducing fastspice capabilities using AMS-UltraSim. Mix of VerilogD, VerilogA and schematic representing the verification testbench.
  - Use HED to assign specific speed (*speed:1,2,3,4..8*) and accuracy options (*sim_mode:s,a,amr,ms,da,df*) for cells needing detailed verification.
  - Perform an intermediate verification step by switching about 4000 devices and 3000 passive components and simulate to show ease of configuring ADE for verification.
  - Insertion of av_extracted_rc layout view (from Assura RCX) with parasitics back-annotated onto the layout, for re-simulation without changing test benches. The parasitic intensive block with passive count up to about 8000 components with a device count of still about 4000.