Active Compensation of Unbalanced Supply Voltages for Two-Stage Direct Power Converters Using the Clamp Capacitor

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***Abstract* - Unbalanced supply voltages can be fully compensated in boost type power converters with active front end if sufficient energy storage is provided by the DC-link capacitor. In converters that have no energy storage, for example in a matrix converter, the maximum voltage transfer ratio will be reduced if one or more input lines is at a reduced voltage. Control techniques to compensate the effect of unbalanced voltage supply for matrix converters allow for a limited output voltage and power capabilities, which depends on the level of unbalance. This paper proposes the utilization of the clamp capacitor, which is normally needed only to protect a Direct Power Converter (DPC), to extend the operating range of a Two-Stage DPC during unbalanced supply conditions preserving its theoretic maximum voltage transfer ratio capability. This solution is validated through simulations.**

I. INTRODUCTION

Currently, the most successful converter topology used in Adjustable Speed Drives (ASDs) consists of a diode bridge rectifier supplying a Voltage Source Inverter (VSI) via a high storage capacitor bank. It has the advantage of being very simple and cheap but as the percentage of nonlinear loads (ASDs with diode rectifiers) increases, negative effects on the mains (current distortion, EMI) have been observed [1]. These shortcomings, in conjunction with the lack of robustness against unbalanced supply voltage require the use of controlled active front-end stages in next generation of ASDs. Extension of the VSI, the two-level PWM rectifier may offer an easy upgrade solution, but the installed energy in passive components remains high.

An alternative to this is the direct power conversion (DPC) approach with forced commutated semiconductor devices (IGBTs, GTOs, etc). The matrix converter [2]-[8], which is the most known DPC representative, has challenged the research in the last 25 years due to the many unsolved implementation aspects, which were solved lately but implies a higher cost. Another possibility to implement DPC providing similar input and output performance as a standard single-stage matrix converter is the two-stage DPC [9]-[13], also referred in the literature as “indirect MC”, “dual bridge MC” or “sparse matrix converter” which consists of a current source type rectifier stage directly linked to a voltage source type inverter stage. It has been shown already that this two-stage DPC allows for reducing the number of IGBTs [12], much simpler commutation of the switches compared to a single-stage matrix converter [11], possibility to build more complex converter structures with multiple supply and load ports [13].

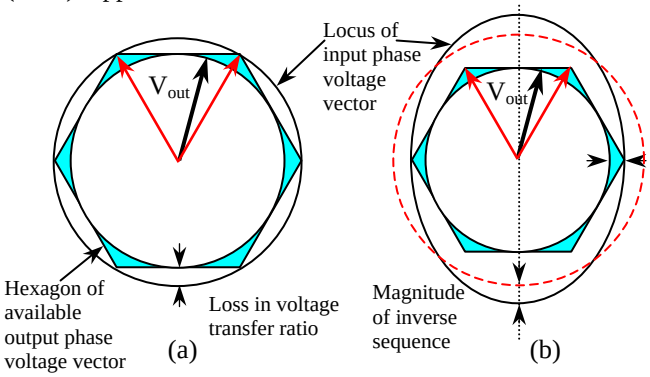

Fig. 1. Locus of the input phase voltage vector, the hexagon of the output voltage vector which has its corners tangent to the input phase voltage vector and the resulting circular output voltage vector which is tangent to the hexagon obtained by applying SVM in three situations: a) balanced input voltage; b) unbalanced voltage system.

Unbalanced voltage supply can be fully compensated in boost type power converters with active front end where enough energy storage is installed in the DC-link capacitor. In DPCs, which have no energy storage (e.g. matrix converter), it is expected that the converter output voltage capability will be affected. Control techniques to compensate the effect of unbalanced voltage supply for matrix converters [14]-[16] allow for a limited output voltage and power capabilities, which depends on the level of unbalance. This is illustrated in Fig. 1, where the input voltage locus, the hexagon of the output voltage vectors and the output voltage locus are shown in two situations, when the input voltages are balanced and the input voltage locus describes a circle (Fig. 1a) and when a certain degree of unbalance exists making the input voltage locus to describe an ellipse while the available output voltage describes a circle of smaller radius (Fig. 1b) which results in smaller voltage transfer ratio [17].

This paper proposes the utilization of the clamp capacitor, which is normally needed to protect a Direct Power Converter (DPC), to extend the operating range of a Two-Stage DPC under unbalanced supply conditions while preserving its theoretical output voltage capability. First, the topology of a Two-Stage DPC with a clamp circuit placed in the dc-link is described and then the solution to activate the clamp capacitor is introduced. The standard Space Vector Modulation (SVM) for the 2-stage DPC is presented, followed by a modified modulation scheme that allows the utilization of the clamp capacitor voltage. A mathematical model for determining the variation range of the clamp

capacitor duty-cycle and the design of the clamp capacitor in order to provide full compensation of the voltage transfer ratio dependent on the unbalance is developed. Simulation results confirm the viability of the solution, followed by initial experimental results.

II. Two-Stage DPC Topology With a Clamp Circuit

In [3], [4], [7], [8] has been shown that a clamp circuit is needed to allow safe shutdown of a DPC that supplies an inductive load, while the size of the clamp capacitor depends on the amount of magnetic energy stored in the load inductance. Normally, the clamp circuit consists of a three-phase diode bridge connected to the load terminals on the AC side and to the clamp capacitor on the dc-side. This clamp circuit is also needed on the input side in order to protect the DPC from possible grid disturbances. Therefore, in most of the applications, it consists of twelve diodes and a capacitor. In [16] it has been proposed to use an IGBT connected in anti-parallel to the clamp capacitor diode to allow circulation of the magnetic load energy when the power factor is poor, because that application utilized a unidirectional rectification stage.

As in this case the objective is to increase the output voltage capability during unbalanced voltage supply, the utilization of clamp capacitor to store a certain amount of energy is desired. The equivalent scheme of the topology shown in Fig. 2, when the clamp capacitor IGBT is off/on is shown in Fig. 3. When the IGBT is off, the converter topology is equivalent to the standard 2-stage DPC (Fig. 3a), and this will be used when operating in the region where the inverse sequence cause the increase of the magnitude of the input voltage vector (see Fig. 1b). During this period, the clamp capacitor voltage will be charged to the maximum available voltage level. When the input voltage vector magnitude decreases below the desired output voltage level, it is necessary to utilize also the clamp capacitor voltage to boost up the average value of the dc-link voltage seen by the inversion stage. Therefore, the equivalent scheme of that switching sequence becomes as shown in Fig. 3b.

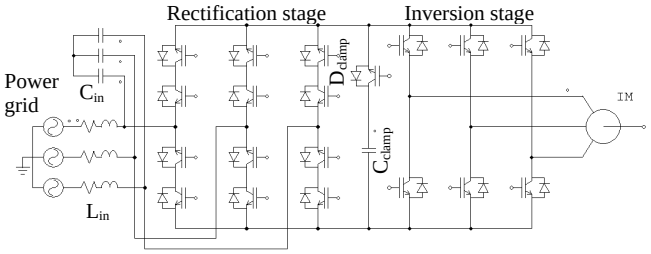

Fig. 2. Topology of a two-stage DPC with a clamp circuit consisting of a capacitor, a diode and a transistor which enables the clamping of the inductive energy from the load and the possibility to feed back energy to the inverter stage similar to what was proposed in [17].

III. Space Vector Modulation for a Two-Stage DPC

A. Operation with Sinusoidal& Balanced Input Voltages

In [11], it has been shown that the implementation of Space Vector Modulation (SVM) for a two-stage DPC is identical to the case of a matrix converter controlled by an indirect SVM [5]-[6], therefore only the final equations are presented here. SVM produces a combination of two adjacent active vectors and a zero-vector to synthesize a reference vector of variable amplitude and angle. The proportion between the duty-cycles of the two adjacent vectors gives the direction and the duty-cycle of the zero-vector determines the magnitude of the reference vector. The input current vector I_{in} (only its angle) is the reference of the rectification stage (Fig. 4a) and the output voltage vector V_{out} is the reference of the inversion stage (Fig. 4b). The duty-cycles of the active switching vectors for the rectification stage, I_γ, I_δ are given by (1) and the duty-cycles of active switching vectors for the inversion stage, V_α, V_β are given by (2).

$$d_\gamma = m_I \cdot \sin\left(\pi/3 - \theta^*_{in}\right) \qquad d_\delta = m_I \cdot \sin\theta^*_{in} \tag{1}$$

$$d_\alpha = m_U \cdot \sin\left(\pi/3 - \theta^*_{out}\right) \qquad d_\beta = m_U \cdot \sin\theta^*_{out} \tag{2}$$

where m_I =1 and m_U are the rectification and inversion stage modulation indexes, θ^*_{in} and θ^*_{out} are the angles within their respective sectors of the input current and output voltage reference vectors. In the rectification stage, the zero-

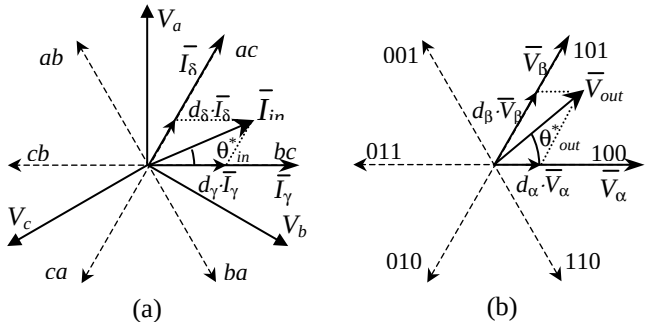

Fig. 4. Generation of the reference vectors in a two-stage Direct Power Converter using SVM: (a) rectification stage; (b) inversion stage.

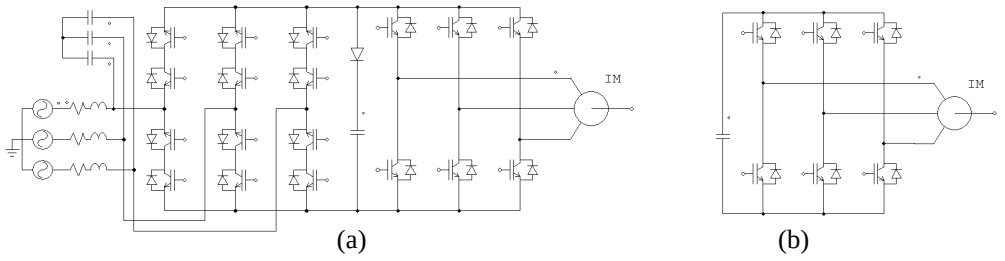

Fig. 3. Equivalent scheme of the two-stage DPC when: a) the transistor in the clamp circuit is OFF and the rectification stage is operated in normal DPC mode; b) the rectification stage is turned OFF and the transistor in the clamp circuit is turned ON (Voltage Source Inverter mode).

vector is eliminated and the switching sequence consists only of the two adjacent current vectors, actually the corresponding line-to-line voltages that will be selected as dc-link voltage by the rectification stage, (e.g. “ac” means V_{pn}=Vac). The zero-vector is produced only by the inversion stage in order to produce the desired output voltage.

By using (1), the adjusted rectification stage duty-cycles are found (3), where the modulation index of the rectification stage used in (1) is now unity.

$$d_{\gamma}^{R} = \frac{d_{\gamma}}{d_{\gamma}+d_{\delta}} \qquad d_{\delta}^{R} = \frac{d_{\delta}}{d_{\gamma}+d_{\delta}} \tag{3}$$

These duty-cycles multiply with the switching period and the resulting ON-times directly drive the rectification stage switches. Since the average voltage in the DC-link is not constant anymore due to the cancellation of the zero-vector in the rectification stage, it is necessary to calculate its value to compensate the modulation index of the inversion stage:

$$V_{PN\text{-}avrg} = d_{\gamma}^{R} \cdot V_{line\text{-}\gamma} + d_{\delta}^{R} \cdot V_{line\text{-}\delta} \tag{4}$$

$$m_U = \sqrt{2} \cdot V_{out} / V_{PN-avrg} \tag{5}$$

The inverter stage may use a double-sided asymmetric PWM switching sequence 0_{γ}-α_{γ}-$\beta_{\gamma+\delta}$-α_{δ}-0_{δ}, but with unequal sides because each side corresponds to a rectification switching sequence which has a different DC-link voltage. Therefore, the value of the modulation index m_U in (2) has to be corrected with the momentary average DC-link voltage $V_{PN\text{-}avrg}$ (4), which takes into account its variation. The inversion stage duty-cycles are given in (6):

$$d_{0\gamma} = \frac{d_{\gamma} \cdot \left[1-\left(d_{\gamma}+d_{\delta}\right)\cdot\left(d_{\alpha}+d_{\beta}\right)\right]}{d_{\gamma}+d_{\delta}} \qquad d_{\alpha\gamma} = d_{\gamma} \cdot d_{\alpha}$$

$$d_{\beta(\gamma+\delta)} = (d_{\gamma}+d_{\delta}) \cdot d_{\beta} \qquad d_{\alpha\delta} = d_{\delta} \cdot d_{\alpha} \tag{6}$$

B. Operation with Unbalanced Supply Voltage

As mentioned before, the key to obtain the desired output voltages is to handle the generation of the zero voltage vector by the inversion stage accordingly, compensating for the variation of the average dc-link voltage delivered by the rectification stage as expressed by (4). This is done by adjusting the modulation index of the inversion stage (5), which in fact is a feed-forward compensation [7]. Besides the normal variation of the average dc-link voltage, this method allows for the rejection of any disturbance present in the input voltage supply, including low-order (5^{th}, 7^{th}, etc) distortion or unbalance (inverse voltage sequence).

The other objective is to obtain input currents with a shape as close as possible to a sinus, which is not that easy to obtain. In [15] it has been shown that in order to improve the quality of the input currents is necessary to decouple the angle of the input current reference vector from the angle of the input voltage vector, which now due to the presence of harmonics and inverse sequence does not rotate with constant instantaneous frequency. This is why it is essential to detect the angle of the direct sequence of the fundamental input voltage vector and use that as the angle of the input current reference vector θ_{in}, which is what was adopted in the simulations shown throughout this paper and referred as “passive compensation”.

IV. Utilization of the Clamp Capacitor Voltage to Compensate the Effect of Unbalanced Supply

The illustration of the voltage transfer limitation is given in Fig. 5, where the three phase voltages (upper) and the dc-link instantaneous voltage and its average (bottom) are shown in two situations: balanced supply voltage (Fig. 5a) and 10 % voltage unbalance (Fig. 5b). It is therefore clear that the output voltage generation capability is decreased when the dc-link average voltage is minimum and that in the case of unbalanced supply, this is further decreased.

Passive compensation of unbalanced voltage supply consist in mixing the two line to line voltages in order to provide a constant average DC-link voltage to the inversion stage (4), or to perform the compensation of the variable average DC-link voltage which is an effect of having unbalanced voltage supply by the modulation index of the inversion stage (5). In order to compensate the effect of unbalance that will reflect on the quality of the input current, a different reference angle of the input current vector has to be chosen. In [14], [15] it has been proven that it is possible to compensate the effect of unbalanced voltage supply on the quality of output voltage, while the output voltage capability decreases compared to the ideal voltage supply, while limited compensation of the unbalance in the quality of the input currents may be achieved. In [16] it has been proposed to use an IGBT in anti-parallel with the diode

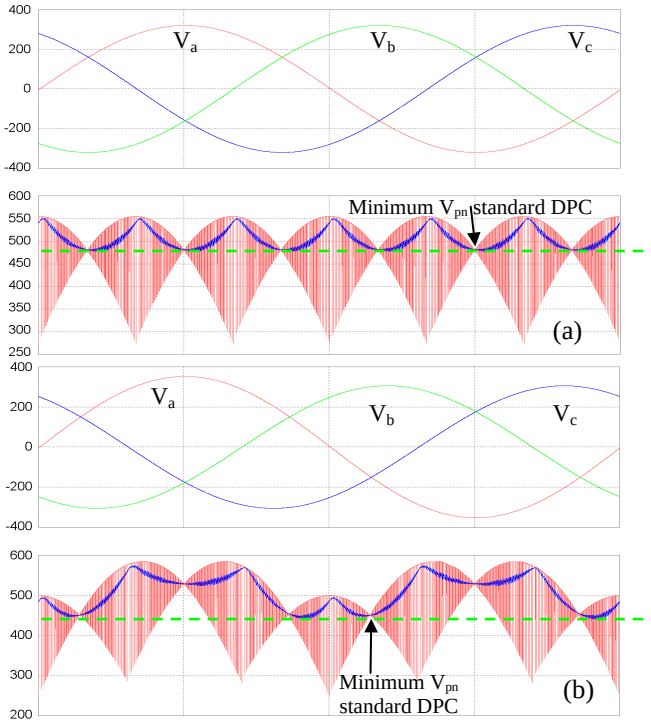

Fig. 5. Input phase voltages, the resulting dc-link voltage and its average value into a two-stage DPC presented in two situations: a) balanced and b) 10 % unbalanced voltage supply, showing where the voltage transfer ratio is limited: a) 480 V and b) 450 V.

in the clamp circuit in order to feed back the energy that returns into the clamp capacitor from the load when the power factor is below 0.5, which is typical to an AC motor operating at light load. The clamp capacitor voltage was utilized when its level exceeded a threshold level, which controlled the turn-on of the transistor mounted in anti-parallel with the diode of the clamp circuit. As the rectification stage was unidirectional and as the clamp circuit voltage was higher than any line-to-line input voltages, it forced the diodes in the rectifier stage to be reverse biased, causing short term (more than a few switching periods) disconnection of the inverter stage from the mains, reflected on having discontinuous input currents.

In this section it will be presented the utilization of the same technique to use the clamp circuit in order to extend the operation range of the 2-stage DPC during unbalanced voltage supply, but employing a new pulse generation technique [13] which ensures the rectifier does not disconnect from the inverter for more than a switching period. The principle of operation is as follows: the clamp capacitor is assumed to be charged at the highest level of the line-to-line voltages remaining charged during the time the inverse sequence causes the loss in magnitude of the input voltage vector. Therefore, when the input voltage vector is too small to produce the desired output voltages, it is possible that instead of combining only the two line-to-line voltages that normally produce the dc-link voltage seen by the inverter stage which now will result in a lower average dc-link voltages, to utilize a third voltage in addition to the two already mentioned: the clamp capacitor voltage. This is illustrated in Fig. 6, where the switching states succession of the rectification stage and the inversion stage are shown separately, and the resulting switching state combination of the two-stage DPC is shown. It is therefore possible to boost up the average dc-link voltage and provide improved compensation capability of the two-stage DPC. As the three voltages are always combined within the switching period, the input current will not loose continuity as happened in [16], which will limit the damage to the input current waveform. It is necessary to prevent the discharge of the clamp capacitor below the instantaneous rectified input voltage in order to avoid a short-circuit of two voltage sources (selected input line voltage and clamp capacitor).

It should be noted that the same technique might be used to slightly increase the voltage transfer ratio of the 2-stage DPC above the theoretical limit of 0.866, but due to the fact that the recharge of the clamp capacitor cannot be controlled, it will result in important input current distortion.

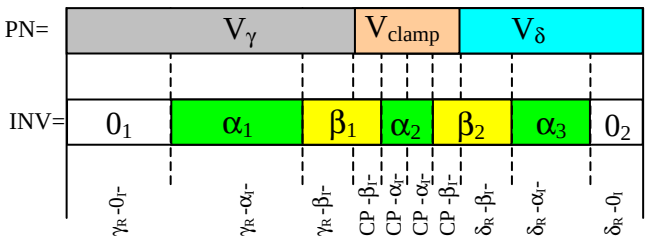

Fig. 6. Combination of the switching state succession in a two-stage DPC in order to perform active compensation of unbalance

A mathematical model is developed below in order to determine the amount of capacitance needed to store enough energy in order to provide active compensation of a given level of unbalance. Lets consider first the standard case with no compensation and balanced supply conditions. The average dc-link voltage is given by (4). The worst situation takes place in the middle of the sector when the angle of the input voltage vector is $\pi/6$ and:

$$d_\gamma = d_\delta = 0.5 \quad V_{PN-REC\_\min} = V_\gamma = V_\delta = \sqrt{3}/2 \cdot V_{line-pk} \quad (7)$$

Lets consider the case when we use the clamp capacitor voltage in order to compensate the effect of unbalance on the average dc-link voltage level:

$$V_{PN-INV} = d_{clamp} \cdot V_{clamp} + \left(1 - d_{clamp}\right) \cdot \left(d_\gamma \cdot V_\gamma + d_\delta \cdot V_\delta\right) \quad (8)$$

It is fair to assume that the clamp capacitor voltage will charge at the highest peak line-to-line voltage level, which is further increased by the negative sequence, while the minimum average uncompensated dc-link voltage level is expected to decrease in correlation with the unbalance:

$$V_{clamp} = \left(1 + unbal\right) \cdot \sqrt{2} \cdot V_{line-D} \quad (9)$$

where *unbal* is the amplitude of the negative sequence present in the supply voltage relative to the positive sequence which has the amplitude $V_{\text{line-D}}$.

$$V_{PN-INV} = d_{clamp} \cdot V_{clamp} + \\ + \left(1 - d_{clamp}\right) \cdot \sqrt{3}/2 \cdot \left(1 - unbal\right) \cdot V_{line-pk} = \sqrt{3}/2 \cdot V_{line-pk} \quad (10)$$

This enables us to find the highest duty-cycle of the clamp capacitor voltage to fully compensate the supply unbalance:

$$d_{clamp-\max} = \frac{unbal}{\frac{\left(1+unbal\right)}{\sqrt{3}/2} - \left(1-unbal\right)} = \frac{1}{\frac{2}{\sqrt{3}} + 1 + \frac{\frac{2}{\sqrt{3}} - 1}{unbal}} \quad (11)$$

For example, in case of 10% unbalance, the clamp capacitor will be connected to the inverter terminals for not more than 27 % of the switching period, which is the maximum. In case we assume a triangular shape of d_{clamp}:

$$\Delta W_{clamp} = \int d_{clamp}(t) \cdot V_{clamp} \cdot I_{dc-avrg} \cdot dt = \\ = 0.5 \cdot d_{clamp-\max} \cdot V_{clamp} \cdot I_{dc-avrg} \cdot \Delta t \quad (12)$$

In case of 10 % unbalance, the duration for which the average dc-link voltage is below the target value is 2 ms, which results in a requirement to store 1.57 J for a 4 kW motor (4.5 kW power fed by the converter) with 485 V average dc-link voltage and 9.3 A average dc-link current.

We assumed that the voltage in the clamp circuit would remain constant. Normally, the ripple in the dc-link voltage will vary from (13) which means 625 V when the negative sequence points into the same direction as the direct sequence and the clamp capacitor is fully charged, to (14)

$$V_{clamp-\max} = \left(1 + unbal\right) \cdot \sqrt{2} \cdot V_{line-D} \quad (13)$$

$$V_{clamp-\min} = \left(1 - unbal\right) \cdot \sqrt{2} \cdot \sqrt{3}/2 \cdot V_{line-D} \quad (14)$$

which means 440 V, when the negative sequence points opposite to the direct sequence. If we assume that we can

allow a discharge of the clamp circuit with 50 V, it results a minimum value for the clamp capacitor, which is feasible:

$$C_{clamp} = \frac{\Delta W_{clamp}}{V_{clamp-av} \cdot \Delta V_{clamp}} = \frac{1.57}{600 \cdot 50} = 52.3\mu F \qquad (15)$$

It is necessary to evaluate the amount of distortion caused by the uncontrolled charging of the clamp capacitor, which is done by assuming similarity with a diode rectifier that selects the highest in magnitude line-to-line input voltage:

$$I_{clamp-\max} = C_{clamp} \cdot \frac{dv_{line-in}}{dt} =$$

$$= 100\pi \cdot C_{clamp} \cdot (1 + unbal) \cdot \sqrt{2} \cdot V_{line-D} \cdot \sin\left(\frac{\pi}{2} + \alpha_{chg}\right)$$

The worst-case condition takes place when the clamp capacitor is fully discharged to the level given by (14), which gives the corresponding angle for the clamp diode to enter conduction:

$$\alpha_{chg-\min} = \sin^{-1}\left(\frac{V_{clamp-\min}}{V_{clamp-\max}}\right) \qquad (17)$$

In case of 10 % voltage unbalance, it means that in the worst case condition $\alpha_{chg} = \sin^{-1}(440/625)=0.25\ \pi$, which in the case of having a 52.5 µF clamp capacitor gives a maximum current peak of 7.3 A. In the case considered in (15) which was used to size the clamp capacitor, the capacitor is discharged only by 50 V giving therefore a higher angle $\alpha_{chg} = \sin^{-1}(575/625)=0.37\ \pi$, which leads to a smaller charging current peak of only 4 A. This situation is reasonable compared with the input current drawn by the converter when operating at full load (approx 10 A_{pk}), which proves that this current peaks will not damage the converter, limiting also the input current distortion.

IV. Simulation Results

Operation of a DPC under unbalanced voltage supply has been previously investigated [15]-[16], but all the methods uses passive compensation which means that the available output voltage decreases as the unbalance increases. In order to prove the superiority of the proposed active compensation method, a simulation test is carried out where the DPC was required to supply the theoretical output voltage limit of 0.86 while the supply voltage has a 10 % unbalance.

Fig. 7 shows the situation when the 2-stage DPC operates under 10 % unbalanced voltage supply, while the output voltage demand is within the generation possibilities of the converter, the ratio between the output voltage demand divided to the direct sequence of the input voltage being $V_{out}/V_{in\text{-}D}$=0.77. The fact that the input voltage supply is unbalanced can be seen in the shape of the dc-link voltage shown in Fig. 7a. Fig. 7b shows the filtered output line-to-line voltages, obtained by applying the output PWM voltages to a RC low pass filter that removes only the switching ripple. The filtered output voltages as well as the load currents presented in Fig. 7c reveal that they are sinusoidal and balanced which proves that passive compensation provided by the feed-forward compensation

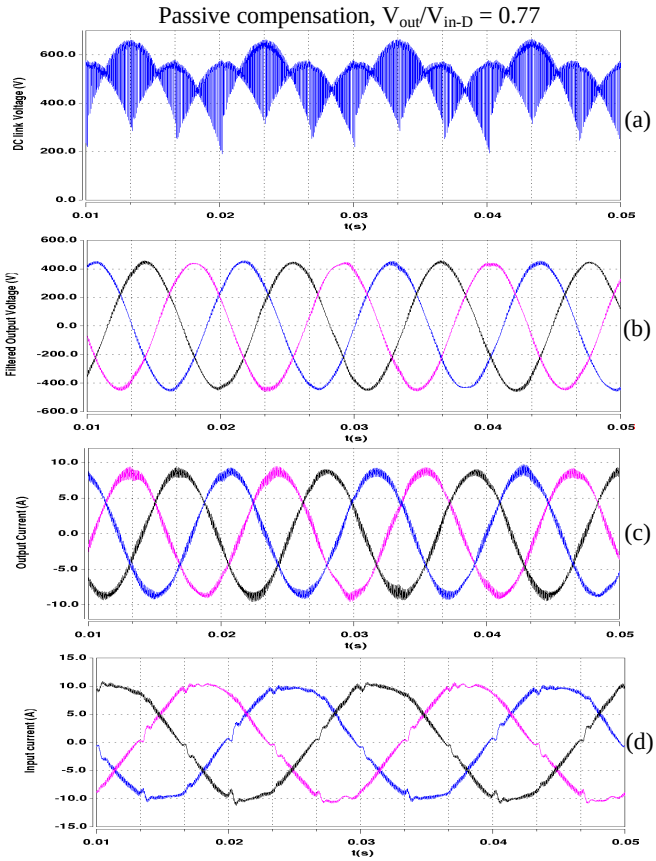

Fig. 7. Operation of a 2-stage DPC with 10 % voltage unbalance when the voltage transfer ratio relative to the direct sequence [$V_{out}/V_{in\text{-}D}$] is 0.77 using passive compensation. Waveforms: a) dc-link voltage; b) filtered output voltages; c) load currents; d) input currents.

of the average dc-link voltage variation works fine as long as the output voltage demand can be supported by the unbalanced supply voltage. The input currents have also an acceptable shape due to the fact that the angle of the input current reference vector is locked on the angle of the direct sequence. They are unbalanced though because this is a direct power converter with no energy storage which means that in order to supply constant ripple-free output power, the input currents have to be unbalanced: the smaller the input voltage is, the larger the line current will result.

Fig. 8 shows the same situation but when the output voltage demand reaches 0.86 the amplitude of the direct voltage sequence. Because in the moment the positive and the negative sequences point opposite there is not enough voltage available (Fig. 8a), the output voltage presents momentary distortion (Fig. 8b) which is reflected also on load current disturbance (Fig. 8c).

With active compensation, which uses the clamp voltage to boost the average dc-link voltage (Fig. 9a), it was possible to maintain the output voltages balanced, undistorted and at a similar high level as when the supply voltages were balanced as seen in Fig. 9b. The load currents are balanced and sinusoidal as well (Fig. 9c). The distortion of the input currents is higher than in the previous two cases, but is acceptable considering the circumstances.

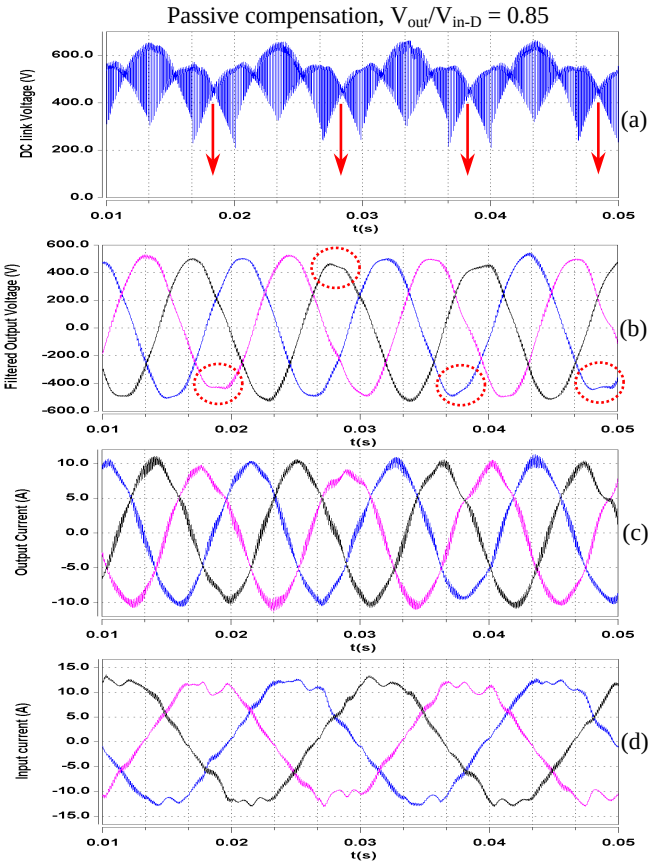

Fig. 8. Operation of a 2-stage DPC with 10 % voltage unbalance when the voltage transfer ratio relative to the direct sequence [V_{out}/V_{in-D}] is 0.85 using passive compensation. Waveforms: a) dc-link voltage; b) filtered output voltages; c) load currents; d) input currents.

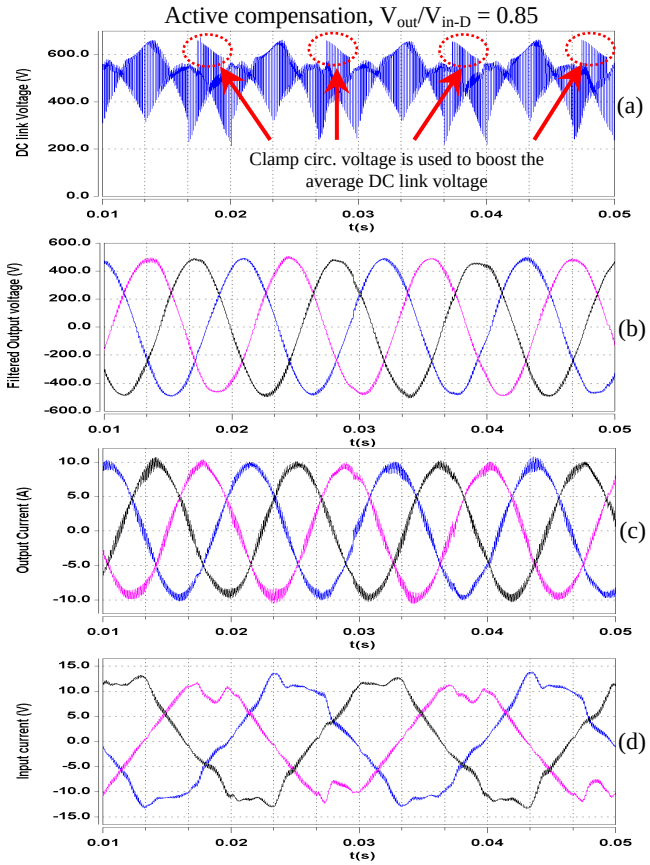

Fig. 9. Operation of a 2-stage DPC with 10 % voltage unbalance when the voltage transfer ratio relative to the direct sequence [V_{out}/V_{in-D}] is 0.85 using active compensation with C_{clamp}=52.5 µF. Waveforms: a) dc-link voltage; b) filtered output voltages; c) load currents; d) input currents.

Fig. 10 shows the locus of the input voltage vector that is unbalanced (locus is an ellipse) and the locus of the averaged output voltage vector which in the case of no compensation, is clearly distorted due to insufficient voltage, while in case the active compensation is performed, it maintains circular shape. The effect on the output current is not so clear because the passive load attenuates the voltage distortion. As expected, the input current is more unbalanced in the case of active compensation.

A prototype is currently under development to prove this solution but until the completion of this paper, only experimental results at reduced input voltage and light load were available and these are shown in Fig. 11. In the upper plot, the three unbalanced phase line-to-line voltages, having 56/75/81 V_{rms} are shown, having more than 20 % unbalance, while the middle shows the dc-link voltage and the interval where the clamp capacitor is activated is emphasized. The filtered output line-to line voltage and the load currents are also shown. The active compensation works, but is not that effective because the 15µF clamp capacitor retains too little energy and discharges near the end of its operating interval. The shape of the output voltage is sinusoidal with a peak of 75 V that would correspond to a balanced three-phase supply voltage of 61.4 V_{rms} line-to-line, slightly above the smallest line-to-line voltage (56 V).

V. Conclusion

A new method to perform active compensation of unbalanced supply voltage is proposed. It uses the clamp capacitor, which traditionally is used only for protection purpose and therefore, remains unused during normal operation, in order to store some energy needed to correct the voltage deficit. It is proven through simulations that it can successfully compensate voltage unbalance as high as 10 % without affecting the output voltage capability, which is the main concern when abnormal supply conditions occur. The price to be paid for improving the converter robustness against grid disturbances is a slightly oversized clamp capacitor, the need to introduce an extra IGBT in the clamp circuit and the degradation of input current quality due to uncontrolled capacitor charging.

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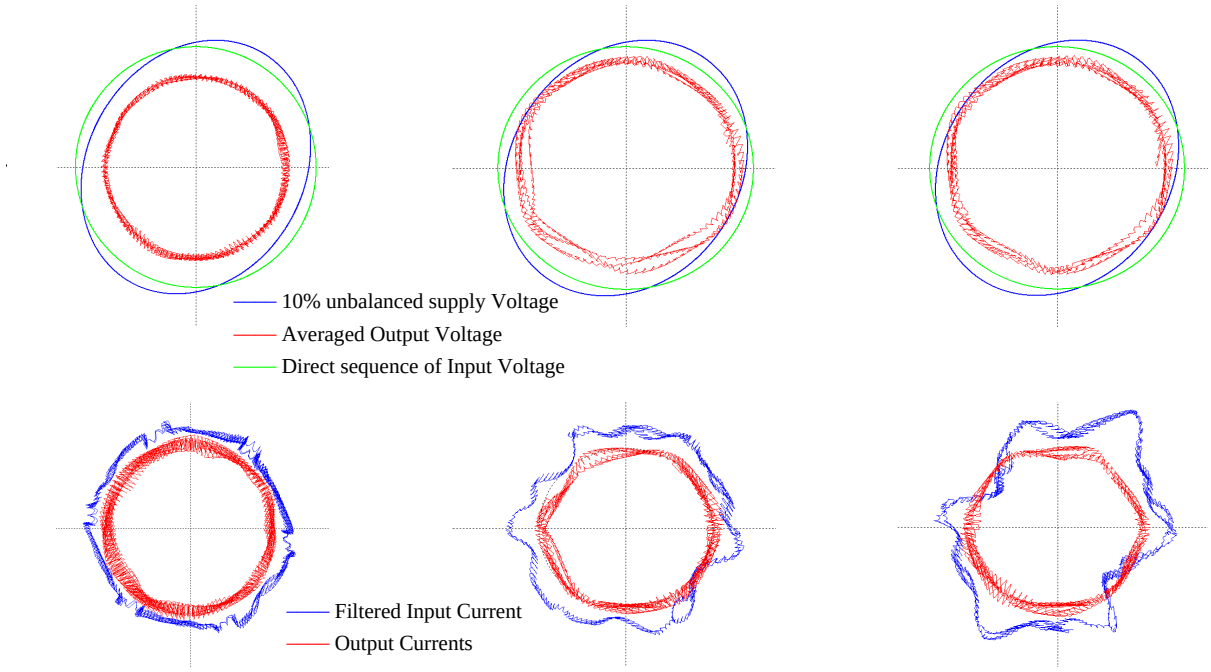

Fig. 10. Trajectory of the input phase voltage and filtered output voltage vectors (top) and of the input and output currents (bottom) in the case of passive compensation with [$V_{out}/V_{in\text{-}D}$] is 0.77 (left side), passive compensation with [$V_{out}/V_{in\text{-}D}$] is 0.85 (center) and active compensation with [$V_{out}/V_{in\text{-}D}$] is 0.85 using the clamp circuit (right side), when the supply voltage has 10% unbalance. C_{clamp}=52.5 µF

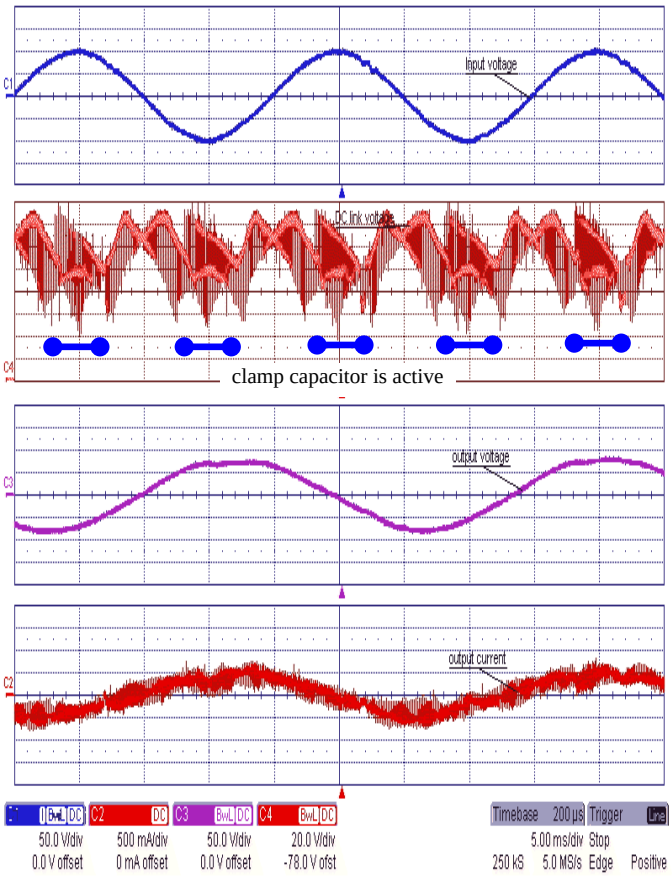

Fig. 11. Experimental result with reduced input line-to line voltage of 56/75/81 V_{rms} and light load connected to the output side: a) input line-to-line voltage; b) dc-link voltage with indication where the clamp capacitor is active; c) filtered output line-to-line voltage; d) load current. Parameters: V_{out}=50V_{rms}; C_{Clamp}=15µF, R_L=120 Ω, L_L=3.75mH, f_{sw}= 8 kHz

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