Implementation of a Hybrid AC/AC Direct Power Converter with Unity Voltage Transfer Ratio

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***Abstract*— A novel hybrid approach for Direct Power Conversion (DPC) based on two-stage Matrix Converter (2-stage MC) topology is proposed, which has practically proven advantages of improved voltage transfer ratio and higher robustness against supply voltage unbalances over the Conventional Matrix Converters (CMC). The hybrid approach also has inherent advantages of the CMC such as: controllable supply power factor, sinusoidal supply currents and no bulky energy storage elements which reduce the life time of the converter. The proposed converter can theoretically have more than unity voltage transfer ratios; even in the case the supply voltage is highly unbalanced. Important aspects of design and implementation of the new Hybrid Direct Power Converter (HDPC) will be presented with theoretical analysis and simulations. Experimental waveforms using a laboratory prototype is presented to confirm the viability of the proposed idea in practice.**

I. INTRODUCTION

Conventional three phase to three phase matrix converters [1]-[8] are capable of providing variable frequency variable voltage three phase output to a load whilst maintaining sinusoidal supply currents with controlled supply power factor irrespective of the type of the load. Matrix convert consists of 9-bidirectional switches (Fig. 1a) enabling bidirectional power flow while directly converting the power without using an energy storage device which may degrade the life span of the converter and reduce the power density. Alternative structures to obtain DPC have been investigated in [9]-[15], where it uses the same or fewer semiconductor devices whilst maintaining the same input/output performances as the CMC. One of such arrangements is presented in Fig. 1b which is known as the '2-stage matrix converter', 'indirect matrix converter' or 'sparse matrix converter in the literature. A 2-stage MC consists of a three phase to two phase matrix converter as the Current Source type Rectifier (CSR) connected to a conventional Voltage Source Inverter (VSI). The intermediate stage of the CSR and VSI acts as a variable voltage DC link due the absence of any energy storage device. Therefore, synchronization of pulses for CSR and the VSI is highly important to maintain power balance with sinusoidal supply currents. Furthermore, absence of any energy storage elements in these DPCs requires having a clamp circuit to protect the converter during sudden turn off of the load due to over current situation [6], [7]. In case of single stage CMC, twelve additional diodes and a clamp capacitor should be employed [6], while a 2-stage MC requires only one diode and a capacitor connected to the intermediate DC link [7].

In contrast to the standard ac/ac power converters, matrix converters are lack of their maximum undistorted load voltage capability and robustness to the supply voltage variations, where converters with bulky energy storage devices would overcome the situation. In the case of CMC the ratio of load voltage over the supply is known as Voltage Transfer Ratio (VTR) which is theoretically limited to 0.866. In practice this figure could further reduce due to a voltage drops in the semiconductor devices, pulse width limitation due to 4-step

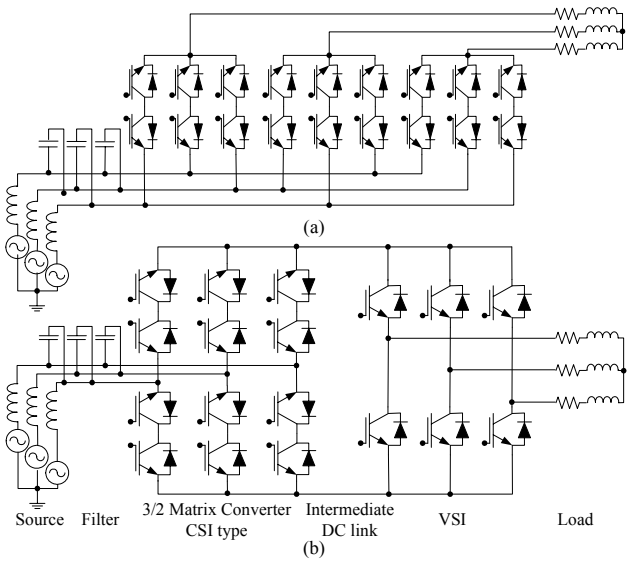

Fig.1. Matrix converter structures:
(a) single stage CMC, (b) 2-stage MC

commutation times or dead times and also due to voltage drops in the filter. Therefore, a feasible limit for the VTR would be around 80 % of the supply. In the case of supply voltage unbalances maximum undistorted load voltage capability is further reduced [15] where limited improvement in VTR can be obtained using active or passive compensation techniques. This limitation of VTR in CMC prevents the use of standard voltage motors in drives based on CMC whereas expensive customized motors will have to be utilized. This factor has been a key issue when commercializing a matrix converter based drive. Traditional boost type back to back voltage source inverters could solve these problems by employing a huge DC link capacitor bank to store energy required to compensate those effects and to have any load voltage demand. On the other hand dc link capacitors could degrade the lifespan of the converter and reduces the power density. Therefore, it is important to investigate a direct power converter which has higher load voltage transfer to have cost effective, compact industrial motor drives while maintaining the standard power quality regulations.

In this paper practical implementation of a HDPC topology solving the most important drawbacks of the 2-stage MC is presented. Analytical study, control technique, modulation scheme, simulation results and experimental results using a laboratory prototype are also presented.

II. HYBRID DIRECT POWER CONVERTER

A. Structure of HDPC

The proposed HDPC structure is based on combine an Auxiliary Voltage Source (AVS) in the intermediate dc link of the 2-stage MC, as presented in Fig.2. It is also required that this AVS should provide higher voltage magnitude than any line to line supply voltage. Therefore, when the converter demands a higher load voltage than the theoretical maximum, AVS could be used to provide the increased in dc link voltage demand. One of the possible arrangements for this AVS is shown in Fig. 2 (b) where a simple boost type converter is utilized with additional switches TR_3 and TR_4 to commutate

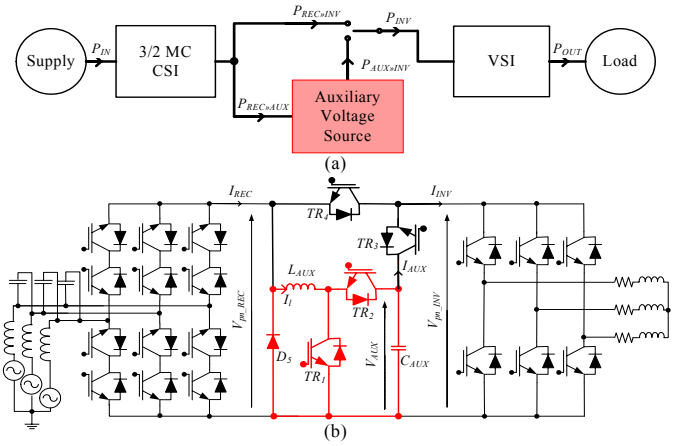

Fig.2. Proposed hybrid DPC: (a) Principal Model, (b) One of the promising arrangements with an auxiliary boost converter connected in the intermediate DC link of the 2stage MC

the currents to the VSI from both the AVS and the rectification stage as required. It can also be noticed that inductor (L_{AUX}) and capacitor (C_{AUX}) in the AVS store energy, as a result, could devalue the proposed idea which is supposed to be a DPC. Therefore, the value of the C_{AUX} and L_{AUX} has to be minimized whilst keeping the AVS voltage (V_{AUX}) constant by controlling the current through the boost inductor (I_l) so that an accurate balance of input and output power over a switching period is achieved. Furthermore, the C_{AUX} in the AVS can also act as a clamp capacitor to absorb the inductive energy when the inversion stage needs to be turned off due to over a current situation. Therefore, additional clamp circuitry for the HDPC is not required unlike in the case of CMC. In a regenerative situation, stored energy in the C_{AUX} could feed back to the rectification stage by operating TR_4 and TR_2, where the AVS acts as a buck type converter. Switch TR_3 will be utilized whenever the AVS is to be used to boost the dc link voltage seen by the VSI, where its switching will be determined by (6).

B. Modulation strategy

Implementation of Space Vector Modulation (SVM) for a 2-stage MC has been discussed in [13] – [15] where a similar approach as in [14] and [15] can be used for the HDPC. According to the SVM for 2-stage MC duty-cycle of the adjacent active input current vectors in a CSI type rectification stage (d_γ,d_δ)and adjacent active output voltage vectors in a VSI type inverter stage (d_α, d_β)can be expressed as:

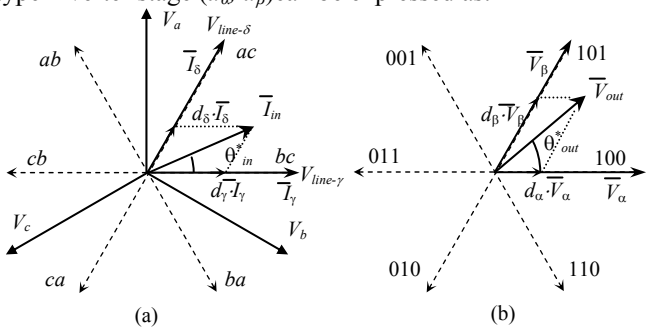

Fig.3. Generation of the reference vectors in a two-stage MC SVM: (a) rectification stage; (b) inversion stage.

$$d_\gamma = m_R \cdot \sin\left(\pi/3 - \theta^*_{in}\right) \qquad d_\delta = m_R \cdot \sin\theta^*_{in} \tag{1}$$

$$d_\alpha = m_I \cdot \sin\left(\pi/3 - \theta^*_{out}\right) \qquad d_\beta = m_I \cdot \sin\theta^*_{out} \tag{2}$$

where m_R and m_I are the rectification and inversion stage modulation indexes and θ^*_{in} and θ^*_{out} are the angles within their respective sectors of the input current and output voltage reference vectors. By eliminating the zero vectors in the rectification stage the modified duty cycles of the rectification stage (d^R_γ, d^R_δ) can be expressed as:

$$d^R_\gamma = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d^R_\delta = \frac{d_\delta}{d_\gamma + d_\delta} \tag{3}$$

Elimination of zero vectors from the rectification stage will produce a time varying dc link voltage output (V_{pn_REC}) which can be expressed as:

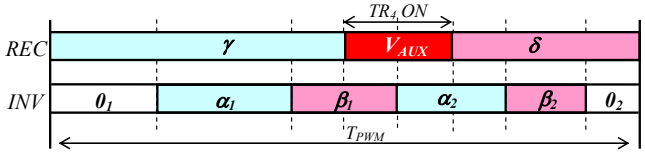

Fig.4. Combination of the switching state succession in hybrid direct power converter: γ, δ are the active vectors of the rectification stage and α, β are the active vectors in the inversion stage, 0 are the inversion-stage zero vectors

$$V_{pn\_REC} = d_{\gamma}^{R}.V_{line-\gamma} + d_{\delta}^{R}.V_{line-\delta} \quad (4)$$

If the duty-cycle of the AVS is d_{AUX}, the resultant dc link voltage seen by the inversion stage (V_{pn_INV}) becomes,

$$V_{pn\_INV} = (1-d_{AUX}).V_{pn\_REC} + d_{AUX}.V_{AUX} = \sqrt{2}.V_{OUT} \quad (5)$$

Therefore, duty cycle of the TR_4 can be obtained by (6) where, V_{OUT} is the output voltage demand and V_{AUX} is the magnitude of the voltage appears across the AVS capacitor.

$$d_{AUX} = \left(\frac{\sqrt{2}V_{OUT} - V_{pn\_REC}}{V_{AUX} - V_{pn\_REC}} \right) \quad (6)$$

The inverter stage use a double-sided asymmetric PWM switching sequence 0_1-α-β-α-0_2, as shown in Fig. 4. The modulation index of the inversion stage can now be expressed as:

$$m_I = \frac{\sqrt{2}V_{OUT}}{V_{pn-INV}} \quad (7)$$

C. *Analysis of Hybrid Direct Power Converter*

By analyzing the power flow through AVS will enable to design the size of the inductor and the capacitor in the AVS, while maintaining undistorted supply currents. For an ideal situation balance of power over one switching period (T_{PWM}) for HDPC is expressed in (8), where P_{INV} is the input power to the inversion stage, P_{AUX} is the power supplied by the AVS and $P_{REC\text{-}INV}$ is the power delivered to the inversion stage by the rectifier.

$$P_{INV} = P_{REC \rightarrow INV} + P_{AUX \rightarrow INV} \quad (8)$$

Equation (8) can be used to derive an expression for the current supplied by the AVS to the inversion stage (I_{AUX}) during T_{PWM} as:

$$I_{AUX} = \frac{d_{AUX}}{\{d_{AUX} + (1-k)\}} I_{INV} \quad (9)$$

Where, I_{INV} is the current drawn by the inverter and,

$$k = \frac{\sqrt{2}V_{OUT}}{V_{AUX}} \quad (10)$$

Energy storage in the AVS during T_{PWM} should be kept zero in order to maintain sinusoidal supply currents. Therefore, neglecting any losses;

$$P_{REC \rightarrow AUX} = P_{AUX \rightarrow INV} \quad (11)$$

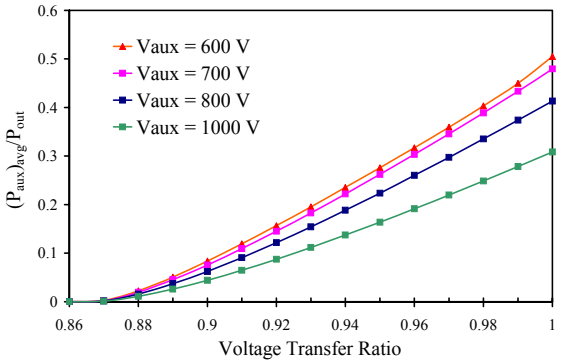

Fig.5. Variation of average power processed by the AVS in the intermediate dc link in the HDPC, as a fraction of the load power Vs the voltage transfer ratio at different level of auxiliary voltages.

where, $P_{REC\text{-}AUX}$ is the input power of the AVS. If the reference inductor current in order to satisfy (11) is $I_{l\text{-}shape}$ following expression can be obtained

$$I_{l\_shape} = \frac{I_{AUX}.V_{AUX}}{V_{pn\_REC}} \quad (12)$$

In an ideal case where inductor current I_l exactly follow the reference given in (12) will result in zero energy storage at C_{AUX}. Any error in tracking the I_l reference would result instantaneous energy storage in C_{AUX} which is the case of any type of practical controller. But properly tuned controller will maintain the zero average error therefore; average energy storage in AVS becomes zero while acting as quasi-direct power conversion.

It is also important to evaluate how much power is processed by the AVS compared to the total power of the converter as it will determine the size of the required AVS. Losses in the VSI are negligible compared to the load power P_{OUT} which is maintained at a constant value therefore;

$$P_{OUT} = P_{INV} \quad (13)$$

Using (8), (9) and (13) power processed by the AVS can be expressed as:

$$P_{AUX} = \frac{d_{AUX}}{k.\{(1-k) + d_{AUX}\}} P_{OUT} \quad (14)$$

Average power processed by the AVS for different Load voltage demands at different V_{AUX} has been simulated to estimate the power sharing of the HDPC which is shown in Fig. 5. It indicates that higher the V_{AUX} the smaller the average power delivered by the AVS thereby the smaller in size. But increasing V_{AUX} results in expensive high voltage devise in use for the AVS and potential to increase losses. Therefore, intermediate level of V_{AUX} = 800 V is chosen where at unitary load voltage demand about 41% of the load power is processed through the AVS.

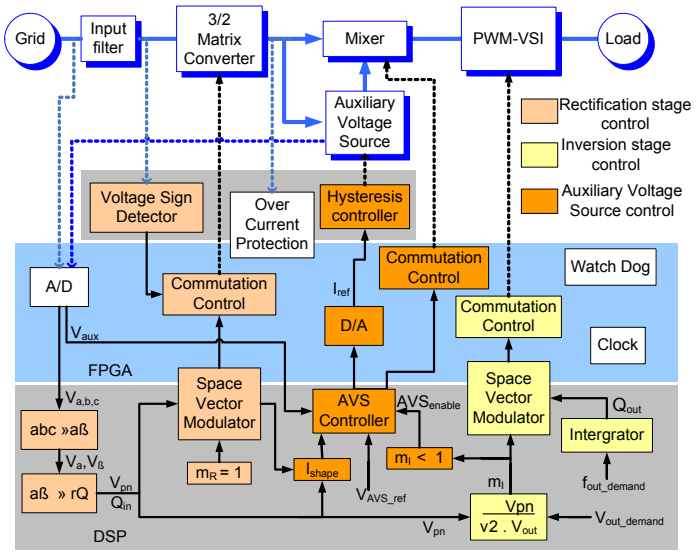

Fig.6. Control structure of the Hybrid Direct Power Converter

III. DESIGN AND CONTROL OF HYBRID DIRECT POWER CONVERTER

A. *Overall control structure*

It is a well known fact that matrix converter requires using high performance Digital Signal Processor (DSP) based control hardware to perform necessary calculations and bi-directional switch commutations as they are comparably more complex than other traditional power converter controls. Protection circuitry, A/D and D/A are also vital elements which could be incorporated must the control platform a compact solution. In addition to those essential elements, input voltage or output current zero crossing detectors will be used if the matrix converter switch commutation is based on input voltage or out put currents [4] respectively. As the basic control elements for HDPC are similar to matrix converter, control architecture designed and proposed in [4] for CMC and used in 2-stage MC [15] can be used. Four step input voltage based commutation control [7] is used for the rectification stage of HDPC. In addition HDPC requires having a hardware hysteresis controller to control the current through the AVS inductor (L_{AUX}) as in (12). The overall structure of the HDPC control is illustrated in Fig. 6. The details of 2-stage MC control are omitted in this paper as it has been discussed in [11] – [15] where only the control of the AVS will be explained in the following section.

B. *Implementation of hysteresis controller for Auxiliary Voltage Source*

According to I_{l_shape} in (12) a controller with a fast dynamics should be selected to force the I_l to follow the (12) which has shape gradients. Hysteresis controller can be used to obtain the desired inductor current shape as it inherently have fast dynamics while having the opportunity to minimize the size of the inductor. Control architecture of the AVS is shown in Fig.7 where a hysteresis controller for the current loop and a PI type relatively slow controller for the voltage loop have been utilized. I_{l_shape} in (12) is multiplied by the PI voltage controller output to generate the reference current (I_{ref}) for the current controller. External hardware for the hysteresis controller is necessary where the calculated I_{ref} will be fed though a D/A converter as illustrated in Fig. 6.

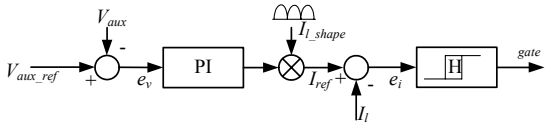

Fig.7. Hysteresis controller for the Auxiliary Voltage Source

In the case of a hysteresis controller care must be taken to limit the bandwidth to avoid high frequency switching of the TR_1 in the AVS. Considering the switching losses in the system increase in the f_{TR1} will directly affect the efficiency of the HDPC because it is subjected to hard switching conditions. Therefore, f_{TR1} can be reduced by introducing a thick hysteresis band (H) or by using an increased inductance for L_{AUX}.

Another factor to be considered is the inductance L_{AUX} which determines the size and cost of the AVS. Therefore, compromise between cost and performance will always be made when selecting the optimum L_{AUX} for each control method.

Structure of the HDPC also allows C_{AUX} to operate as a clamp capacitor. If the necessary clamp capacitance is C_{Clamp} the following (15) should also be satisfied. But the voltage rating of C_{AUX} must be higher than normal clamp capacitor due to increase V_{AUX} which could incur additional cost.

$$C_{AUX} \geq C_{Clamp} \qquad (15)$$

The value of C_{Clamp} can be found as presented in [7] considering the motor and circuit parameters. A typical value for the clamp capacitor is about 100 µf. with voltage of 850 V.

IV. RESULTS

A. *Simulation Results*

Operation of the HDPC was simulated using the Saber© simulation package in order to synthesize and compare the performances with the CMC.

Variations of switching frequency of the TR_1 (f_{TR1}) and step

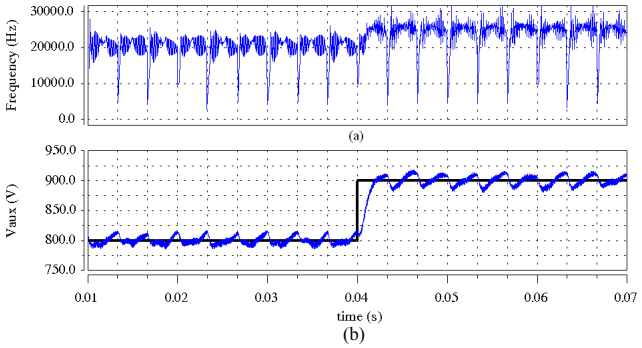

Fig.8. (a) Variation of the switching frequency and (b) step response of the V_{AUX} of the AVS when using a hysteresis current controller (L_{AUX} = 2 mH and hysteresis band = 4 A).

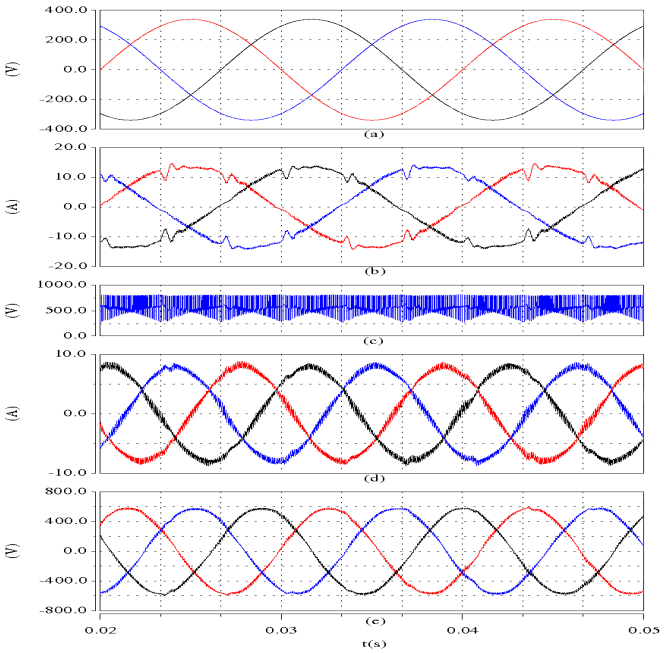

Fig.9. Simulation of HDPC operates at unitary voltage transfer when supply voltage is balanced (a) supply phase voltage, (b) supply currents, (c) dc link voltage seen by the inversion stage, (d) load currents and (e) filtered line to line load voltage (Appendix - I).

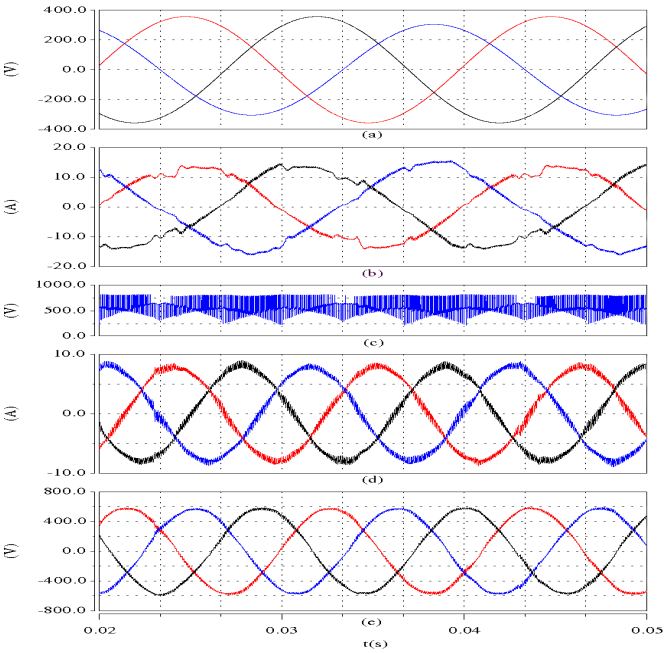

Fig.10. Simulation of HDPC operates at unitary voltage transfer when supply voltage is 10% unbalanced (a) supply phase voltage, (b) supply currents, (c) dc link voltage seen by the inversion stage, (d) load currents and (e) filtered line to line load voltage (Appendix - I).

response of the hysteresis controller are illustrated in Fig. 8. It can be noticed that ripple voltage of approximately 30 V is presented in V_{AUX} where sampling of instantaneous value of V_{AUX} in (11) can minimize the impact on the output performance. In a HDPC, AVS is only used in the situation where the load voltage demands more than 86 % of the supply. When the demanded load voltage becomes higher than 86% AVS processes a smaller amount of power (Fig.5.). At these instances the AVS is inactive for several milliseconds in which unstable behavior of the controller can be observed with this type of PI based voltage control. Alternatively a fuzzy controller may be used to replace the PI to avoid such situations.

Fig.9 shows the operation of HDPC at unitary voltage transfer having a balanced supply voltage. Passive load of R_L=42 Ω and L_L = 5 mH was used to simulate a balance load where the inductance is similar to the leakage inductance in a typical induction motor. According to the Fig. 9(a) and Fig. 9(b) zero displacement of the supply voltage and the current could be observed as expected from the space vector modulation for a CSI type rectification stage with unity power factor. Fig. 9(c) shows that the dc link voltage produce by the HDPC is pulsating due to the absence of any energy storage unlike in the case of a conventional VSI. The waveform in Fig. 9(e) represents the filtered line to line load voltage where only the high frequency switching ripples have been eliminated to clearly observe the VTR. The peak value of the filtered load voltage is about 590 V which represents a unitary voltage transfer as the supply is 415Vrms.

B. Simulation with unbalanced supply voltagesupply

The results shown in Fig.10 are for one of the extreme conditions where supply voltage is highly unbalanced. Fig. 10 shows how the supply/load current and voltage waveforms of a HDPC operating at 10% supply voltage unbalance condition where the converter feeds the same load as in the balance supply voltage situation shown in Fig. 9. The filtered load voltage waveforms shown in Fig. 10(e) have the peak value of 590V which is same as the magnitude of the direct sequence of the supply voltage. Thereby a unitary voltage transfer was confirmed using HDPC even at 10% supply voltage unbalance. Variation of the inductor current and its reference in the AVS and the capacitor voltage of the AVS in the case of supply voltage unbalance situation are shown in Fig. 11.

Fig. 12 shows the trajectory of the supply and the filtered load voltage vectors when the HDPC operates at the unitary load voltage demand. The Fig. 12 compares two situations

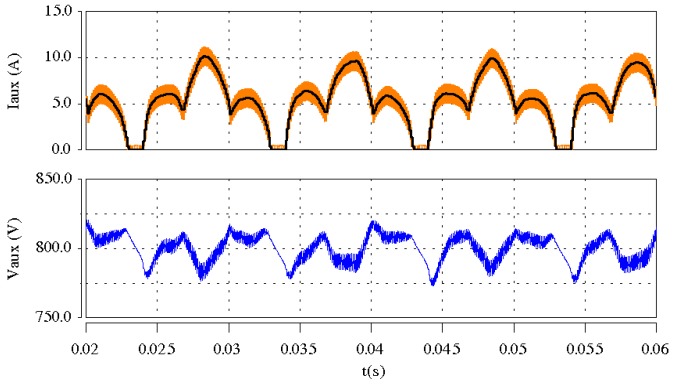

Fig.11. Simulated behavior of (a) current through the auxiliary inductor (I_{AUX}) and its reference I_{ref}, (b) resultant auxiliary voltage V_{AUX} produced by AVS at 10 % input voltage unbalance

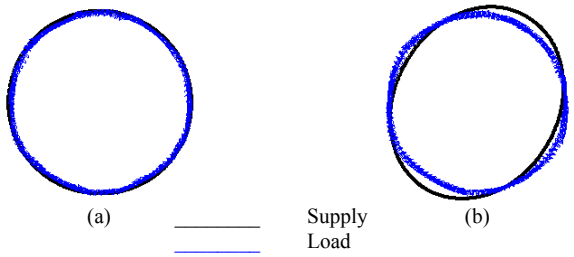

Fig.12. Trajectory of the Supply and load voltage vectors of the HDPC when demanding a unitary load voltage, (a) at supply voltage balanced and (b) at 10% supply voltage unbalance condition.

where the supply is balanced and its 10 % unbalanced. In both the situations circular trajectory of the load voltage indicates balanced three phase load voltage situation. At some points the amplitude of the load vector is more than the minimum amplitude of the supply which shows it is operating more than the maximum which could be obtained from a CMC. In the case of a CMC and 2-stage MC, producing a balance undistorted load voltage at supply voltage unbalance situation is limited even with the active compensation techniques [15]. But results of the HDPC indicate that the topology is capable of compensating supply unbalance disturbances without degrading the input-output performance of the system. Therefore, the HDPC has the potential to replace commercial drives in future where, factors such as; size, lifespan, supply power quality and. reliability are important.

C. *Experimental Results*

In order to validate the operation a laboratory prototype has been built for a 4 kW HDPC using a high voltage boost type converter as the auxiliary supply which is shown in Fig. 13. Texas Instruments© TMS320C6711 DSP and Actel© ProASIC A500K050 FPGA is utilized [4] for the control flat-form where all the A/D, D/A and the protection circuits as described in Fig. 5 were included in to the same board

Inductance value of 2 mH was selected for the L_{AUX}

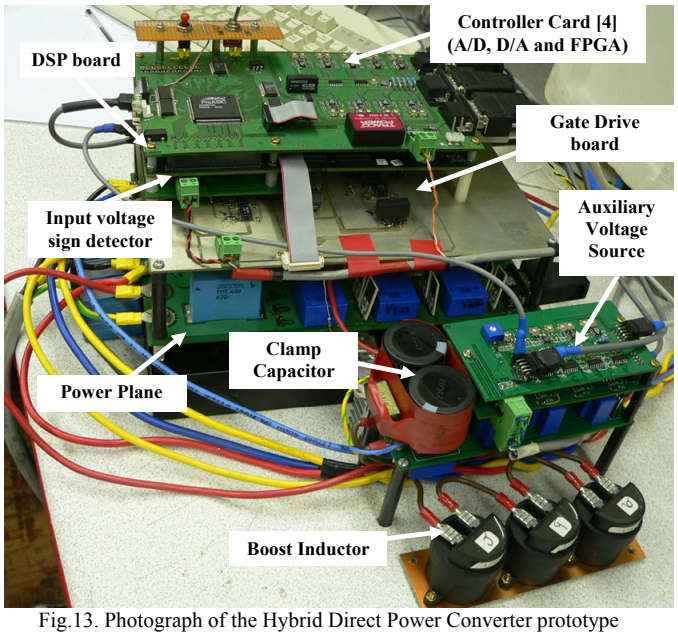

Fig.13. Photograph of the Hybrid Direct Power Converter prototype showing the essential components (Installed power 4kW).

according to the consideration described earlier. Calculated value for the C_{Clamp} as detailed in [6] and [7] for the laboratory prototype illustrated in Fig. 13, was about 19.5µF. Therefore, according to (15) capacitance of C_{AUX} is selected as 20 µF also to accommodate the energy in the L_{AUX}.

By the time of writing this paper experimental results at reduced supply voltage at low power are available at more than the unity VTR which is presented in Fig. 14. Filtered line to line load voltages are shown in Fig. 14 (a) which shows a 200 V peak value while line to line supply (Fig. 14b) voltage is 150 V peak. Therefore, results indicate a VTR of 1.33 with the use of an auxiliary voltage of 400 V. Mixing of the two line to line voltages V_γ and V_δ and the AVS (V_{aux}) over a switching period, in order to boost the average DC link voltage seen by the VSI is shown in Fig. 14 (e).

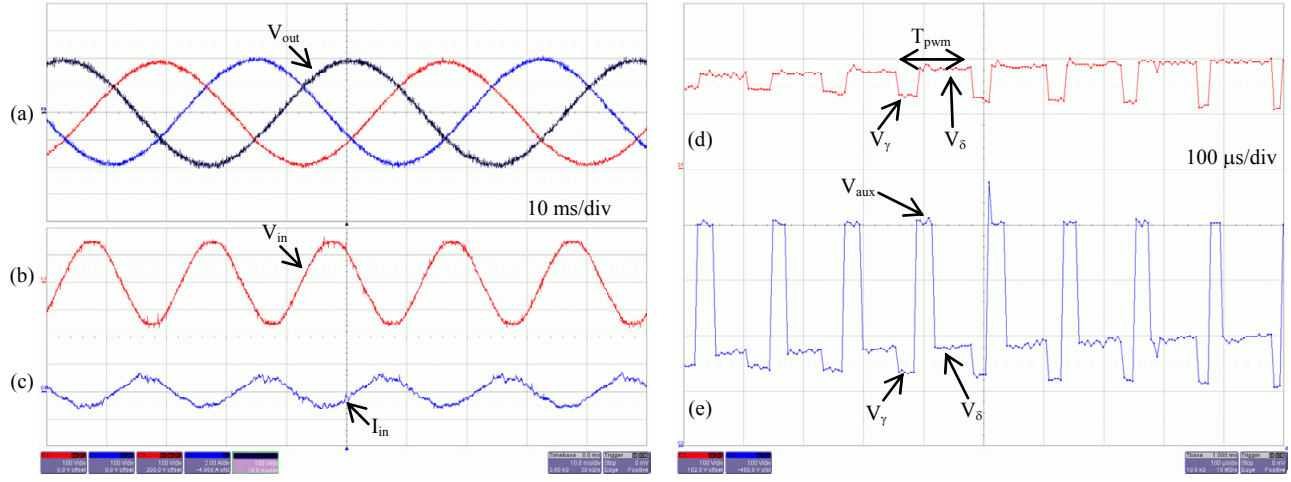

Fig.14. Experimental results of HDPC when operating with more than unitary VTR at low supply voltage; (a) filtered line to line load voltages, (b) supply line to line voltage, (c) supply current, (d) DC link voltage before mixing the 3rd AVS, (e) DC link voltage seen by the VSI after mixing AVS to boost the average Vertical Scale: 100 V/div, 2A/div (Appendix - II)

V. CONCLUSION

A novel hybrid approach for Direct Power Converters based on 2-stage MC which has advantages over other DPCs in improved Voltage Transfer Ratio and robustness to the supply voltage unbalances is proposed. An auxiliary voltage supply with a higher voltage is used to increase the average DC link voltage where the average energy storage during a switching period in the AVS is maintained zero by an appropriate control of the power flow. Thereby a quasi- direct power conversion is achieved. The HDPC requires no additional clamp circuit which is usually used in the CMC for protection thereby reduction of cost for the clamp circuitry. Simulation results and the experimental results with reduced voltage prove that the proposed method delivers the expected benefits.

APPENDIX – I. SIMULATION PARAMETERS

The parameters used for the simulation results presented in Fig. 9, Fig. 10 , Fig. 11 and Fig. 12 are: $V_{out\text{-}phase}$ (rms)= 240 V; f_{out} = 90 Hz; V_{AUX} =800 V; Supply Filter: L_{in}= 1 mH; C_{in} = 9.2 µF/phase; L_{AUX} = 2 mH; R_{load} =42; L_{load}= 5 mH/phase; hystersis band H=4 A, fsw =10 kHz.

In the case of Fig 9 and Fig 12(a) $V_{in\text{-}phase}$(rms) = 240V/240V/240, In Fig. 10, Fig. 11 and Fig 12(b) $V_{in\text{-}phase}$(rms) = 252.86V/216V/252.86V;

APPENDIX – II. EXPERIMENTAL PARAMETERS

The parameters for the experimental results presented in Fig. 14 are: $V_{in\text{-}phase}$ 61.5 V_{rms}; $V_{out\text{-}phase}$ = 82 V_{rms}; f_{out} = 21 Hz; V_c =400 V; L_{in}= 1 mH; C_{in} = 9.2 µF/phase; L_{boost} = 0.9 mH; R_{load} =120; L_{load}= 3 mH/phase; fsw = 10 kHz.

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