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Pei-Hsin Ho

Professional Experience

1998 - present Synopsys, Inc. Hillsboro, OR

Synopsys Fellow with the Implementation Group.

- Working on next-generation IC design automation software.
- Built and led an international team that developed an ultra low-power asynchronous design technology, designed and taped out a test chip of an asynchronous JPEG codec to validate the asynchronous design technology.
- Built and led an international team that produced technologies for implementing low-power ICs and productized 6 new capabilities in Synopsys flagship software product IC Compiler.
- Built and led a team that created and productized Magellan, Synopsys' hybrid RTL verification product that won the IEC Design Vision Award in 05 and was the #1 hybrid/formal RTL verification tool in 06 and 07 (John Cooley).

1995 - 1998 Intel Corporation Hillsboro, OR

Senior CAD Engineer with Strategic CAD Labs.

- Developed several formal property verification technologies for microprocessors.

1991 - 1995 Cornell University Ithaca, NY

Ph.D. student with Prof. Tom Henzinger on the formal verification of hybrid systems.

- Created formal verification technology HyTech for real-time embedded systems.

Education

1991 - 1995 Cornell University Ithaca, NY

Ph.D., Computer Science. Dissertation: Automatic Analysis of Hybrid Systems.

1987 - 1989 National Chiao-Tung University Hsinchu, Taiwan

Master of Science, Applied Mathematics.

1983 - 1987 Chung-Yuan Christian University Chungli, Taiwan

Bachelor of Science, Applied Mathematics.

Patents

- Method and apparatus for reducing power consumption in an integrated circuit
- Method and apparatus for partitioning an integrated circuit chip
- Abstraction refinement using controllability and cooperativeness analysis
- Method and apparatus for solving sequential constraints
- Simulation-based functional verification of microcircuit designs

Professional Activities

Technical Program Committee for DAC, ATVA and ASICON. Editorial Board for Formal Methods Letters. Referee for ICCAD, ICCD, CAV, IEEE TCAD and IEEE TSE.

Publications

- GPU friendly fast Poisson solver for structured power grid network analysis, in *Proceedings of DAC2009* (**Best Paper Candidate**). Co-authored with J.Shi, Y.Cai, W.Hou, L.Ma, S. X.-D. Tan and X.Wang.
- On improving optimization effectiveness in interconnect-driven physical synthesis, in *Proceedings of ISPD2009.* Co-authored with P. Saxena, V. Khandelwal, C. Qiao, J.-C. Lin and M. Iyer.
- Automatic Register Banking for Low-Power Clock Trees, in *Proceedings of ISQED 2009.* Co-authored with W. Hou.
- Techniques for effective distributed physical synthesis, in *Proceedings of DAC2007*. Co-authored with F. Mang and W. Hou.
- Intelligent random vector generator based on probability analysis of circuit structure, in *Proceedings of ISQED2007*. Co-authored with Y. Kuo, C. Lin, C. Wang and S. Chang.
- Power-aware placement, in *Proceedings of DAC2005*. Co-authored with Y. Cheon, A.B. Kahng, S. Reda and Q. Wang.
- Supporting sequential assumptions in hybrid verification, in *Proceedings of ASPDAC2005.* Co-authored with E. Cerny, A. Dsouza, K. Harer and T. Ma.
- Abstraction refinement by controllability and cooperativeness analysis, in *Proceedings of DAC2004.* Co-authored with F. Mang.
- Formal property verification by abstraction refinement with formal, simulation and hybrid engines, in *Proceedings of DAC2001*. Co-authored with D. Wang, J. Long, J. Kukula, Y. Zhu, T. Ma and R. Damiano.
- Smart Simulation using collaborative formal and simulation engines, in *Proceedings of ICCAD2000*. Co-authored with T. Shiple, K. Harer, J. Kukula, R. Damiano, V. Bertacco, J. Taylor and J. Long.
- Coverage estimation for symbolic model checking, in *Proceedings of DAC1999* (**Best Paper Award**), pp. 300-305. Co-authored with Y. Hoskote, T. Kam and X. Zhao.
- Formal verification of pipeline control using token semantics and data abstraction, in *Proceedings of ICCAD1998,* pp. 529-536. Co-authored with A. Isles and T. Kam.
- Verification of a complete floating-point unit using word-level model checking, in *Proceedings of FMCAD1996,* Lecture Notes in Computer Science 1166, Springer-Verlag, 1996, pp. 19-33. Co-authored with Y-A. Chen, E. Clarke, Y. Hoskote, T. Kam, M. Khaira, J. O'Leary and X. Zhao.

- HyTech, A Model Checker for Hybrid Systems, in *Software Tools for Technology Transfer*, Vol.1, No.1, pp.110-122, 1998. Co-authored with T.A. Henzinger and H. Wong-Toi.

- Algorithmic Analysis of Nonlinear Hybrid Systems, in *IEEE Transactions on Automatic Control*, Vol.43, No.4, pp.540-554, 1998. Co-authored with T.A. Henzinger and H. Wong-Toi.

- The Algorithmic Analysis of Hybrid Systems, in Theoretical Computer Science, Vol. 138, 1995, pp 3--34. Co-authored with R. Alur, C. Courcoubetis, T.A. Henzinger, X. Nicollin, A. Olivero, J. Sifakis and S. Yovine.

- Automatic Symbolic Verification of Embedded Systems, in *IEEE Transactions on Software Engineering*, Vol. 22, No.3, 1996, pp 181--201. Co-authored with R. Alur and T.A. Henzinger.

- Automated analysis of an audio control protocol, in *Proceedings of CAV95*, Lecture Notes in Computer Science (LNCS) 939, Springer-Verlag, 1995, pp. 381-394. Co-authored with H. Wong-Toi.

- HyTech: The next generation, in *Proceedings of IEEE RTSS95*. Co-authored with T.A. Henzinger and H. Wong-Toi.

- A note on abstract-interpretation strategies for hybrid automata, in *Proceedings of the Hybrid System Workshop*, LNCS 999, Springer-Verlag, 1995. Co-authored with T.A. Henzinger.

- HyTech: the Cornell HYbrid TECHnology tool, in *Proceedings of the Hybrid System Workshop*, LNCS 999, Springer-Verlag, 1995. Co-authored with T.A. Henzinger.

- Hybrid automata: an algorithmic approach to the specification and verification of hybrid systems, in *Proceedings of Hybrid Systems Workshop*, LNCS 736, Springer-Verlag, 1993, pp. 209--229. Co-authored with R. Alur, C. Courcoubetis and T.A. Henzinger.

- The β – Assignment Problems, in *European Journal of Operation Research*, Vol. 104, No.3, pp 593-600, 1998. Co-authored with G.J. Chang.

- The β – Assignment Problem in General Graphs, in *Computers and Operation Research*, Vol. 24, No. 8, pp.757-765, 1997. Co-authored with G.J. Chang.

- The Domatic Problems on Interval Graphs, in *SIAM Journal of Discrete Mathematics*, 3(4). pp.531--536, 1990. Co-authored with T.-L. Lu and G.J. Chang.