

## SDRAM Module Serial Presence Detect Definitions

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### Overview

This application note fully describes the Serial Presence Detect assignments for SPD revision 2 used on Synchronous DRAM Modules.

The table on the following page summarizes the byte assignments. The rest of this document gives the details of each of these bytes. Included are serial PD tables for 168 pin Unbuffered and Registered/Buffered SDRAM and 144 pin SDRAM SO DIMMs which have been JEDEC approved. This information may be changed based on further JEDEC activities. Please refer to product datasheets for the most current information.

For most serial PD 'bytes', a line number has been included which will allow related documents to reference specific table entries in a convenient manner. For example, Byte 3, line 11 defines 11 Row Addresses (0Bh). Even though many of the PDs seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries. Unused entries will be coded as 00h except where noted.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes written during module production	1
1	Total number of Bytes in Serial PD device	2
2	Fundamental Memory Type (FPM, EDO, SDRAM ...)	
3	Number of Row Addresses on this assembly	3
4	Number of Column Addresses on this assembly	
5	Number of DIMM Banks	
6-7	Data Width of this assembly	
8	Voltage Interface Level of this assembly	
9	SDRAM Cycle time at Maximum Supported $\overline{\text{CAS}}$ Latency (CL), CL=X	4
10	SDRAM Access from Clock	
11	DIMM configuration type (Non-parity, Parity or ECC)	
12	Refresh Rate/Type	4, 5
13	Primary SDRAM Width	
14	Error Checking SDRAM Width	
15	SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back Random Column Access	
16	SDRAM Device Attributes: Burst Lengths Supported	
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	4
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency	4
19	SDRAM Device Attributes: $\overline{\text{CS}}$ Latency	4
20	SDRAM Device Attributes: Write Latency	4
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	4
23	Minimum Clock Cycle at CLX-1	4
24	Maximum Data Access Time ( $t_{AC}$ ) from Clock at CLX-1	4
25	Minimum Clock Cycle at CLX-2	4
26	Maximum Data Access Time ( $t_{AC}$ ) from Clock at CLX-2	4
27	Minimum Row Precharge Time ( $t_{RP}$ )	4
28	Minimum Row Active to Row Active delay ( $t_{RRD}$ )	4
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay ( $t_{RCD}$ )	4
30	Minimum $\overline{\text{RAS}}$ Pulse width ( $t_{RAS}$ )	4
31	Module Bank Density	
32	Address and Command Setup Time Before Clock	6
33	Address and Command Hold Time After Clock	6
34	Data Input Setup Time Before Clock	6
35	Data Input Hold Time After Clock	6
36-61	Superset Information (may be used in future)	
62	SPD Revision	
63	Checksum for Bytes 0-62	
64-71	Manufacturer's JEDEC ID Code	7
72	Module Manufacturing Location	7
73-90	Module Part Number	7
91-92	Module Revision Code	7
93-94	Module Manufacturing Date	7
95-98	Module Serial Number	7
99-125	Manufacturer's Specific Data	7

1. This will typically be programmed as 128 Bytes.
2. This will typically be programmed as 256 Bytes.
3. High order bit defines if assembly requires "redundant" addressing (if set to "1", redundant addressing is required).
4. From Datasheet.
5. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh.
6. The JEDEC spec specifies that these bytes are optional for 66MHz applications. If they are not included, then the SPD revision level (byte 62) is set at revision 1 (01h).
7. These are optional, in accordance with the JEDEC spec.



Byte Number	Function Described	Notes
126-127	Reserved	
128-255	Open for customer use	

1. This will typically be programmed as 128 Bytes.
2. This will typically be programmed as 256 Bytes.
3. High order bit defines if assembly requires "redundant" addressing (if set to "1", redundant addressing is required).
4. From Datasheet.
5. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh.
6. The JEDEC spec specifies that these bytes are optional for 66MHz applications. If they are not included, then the SPD revision level (byte 62) is set at revision 1 (01h).
7. These are optional, in accordance with the JEDEC spec.



## Byte 0: Number of Bytes Utilized by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Line #	Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

## Byte 1: Total Number of Bytes in Serial PD Device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor.

Line #	Serial Memory	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	2 Bytes	0	0	0	0	0	0	0	1	01
2	4 Bytes	0	0	0	0	0	0	1	0	02
3	8 Bytes	0	0	0	0	0	0	1	1	03
4	16 Bytes	0	0	0	0	0	1	0	0	04
5	32 Bytes	0	0	0	0	0	1	0	1	05
6	64 Bytes	0	0	0	0	0	1	1	0	06
7	128 Bytes	0	0	0	0	0	1	1	1	07
8	256 Bytes	0	0	0	0	1	0	0	0	08
9	512 Bytes	0	0	0	0	1	0	0	1	09
10	1024 Bytes	0	0	0	0	1	0	1	0	0A
11	2048 Bytes	0	0	0	0	1	0	1	1	0B
12	4096 Bytes	0	0	0	0	1	1	0	0	0C
13	8192 Bytes	0	0	0	0	1	1	0	1	0D
14	16384 Bytes	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	-	1	1	1	1	1	1	1	0	FE
255	-	1	1	1	1	1	1	1	1	FF

## Byte 2: Memory Type

This byte describes the fundamental memory type (or technology) implemented on the module.

Line #	Fundamental Memory Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	TBD	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
253	TBD	1	1	1	1	1	1	0	1	FD
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF



### Byte 3: Number of Row Addresses

This field describes the Row addressing on the module. If there is one physical bank on the module **or** if there are two physical banks of the same size and organization, then bits 0-3 are used to represent the number of row addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0-3 represent the number of row addresses for physical bank 1 and bits 4-7 represent the number of row addresses for physical bank 2 (bank 2 device is 2x bank 1 device width). Note that these do not include the Bank Address pin since physical bank selection of DIMM modules is asserted on dedicated BA (Bank Address) pins. Also note that if the module employs redundant addressing, then it is denoted in Byte 21, bit 6.

Examples of Byte 3 implementation include:

Number of Banks	Number of Row Addresses for Bank 1	Number of Row Addresses for Bank 2	Module Organization	Device Used	Byte 3 Contents
1	11, RA0-RA10	N/A	2M x 64	2M x 8	0000 1011
2	11, RA0-RA10	11, RA0-RA10	2 x 2M x 64	2M x 8	0000 1011
2	11, RA0-RA10	11, RA0-RA10	2M x 64 & 1M x 64	2M x 8 & 1M x 16	1011 1011

**Byte 3, Subfield A: Number of Row Addresses on Bank 1, OR  
Number of Row Addresses on Bank 1 and 2 if both banks have the same depth (Bits 0-3)**

Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	
0A	Undefined	See Subfield B				0	0	0	0	_0	
1A	1/16						0	0	0	1	_1
2A	2/17						0	0	1	0	_2
:	:						:	:	:	:	:
7A	7						0	1	1	1	_7
8A	8						1	0	0	0	_8
9A	9						1	0	0	1	_9
10A	10						1	0	1	0	_A
11A	11						1	0	1	1	_B
12A	12						1	1	0	0	_C
13A	13						1	1	0	1	_D
14A	14						1	1	1	0	_E
15A	15						1	1	1	1	_F



Byte 3, Subfield B: Number of Row Addresses on Bank 2 if banks have different depths (Bits 4-7)										
Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	No 2nd Asymmetric Bank	0	0	0	0					0_
1B	1/16	0	0	0	1					1_
2B	2/17	0	0	1	0					2_
:	:	:	:	:	:					:
7B	7	0	1	1	1					7_
8B	8	1	0	0	0					8_
9B	9	1	0	0	1					9_
10B	10	1	0	1	0					A_
11B	11	1	0	1	1					B_
12B	12	1	1	0	0					C_
13B	13	1	1	0	1					D_
14B	14	1	1	1	0					E_
15B	15	1	1	1	1					F_



### Byte 4: Number of Column Addresses

This field describes the Column addressing on the module. If there is one physical bank on the module **or** if there are two physical banks of the same size, then bits 0-3 are used to represent the number of column addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0-3 represent the number of column addresses for physical bank 1 and bits 4-7 represent the number of column addresses for physical bank 2 (bank 2 device is 2x bank 1 device width). For example:

Number of Banks	Number of Column Addresses for Bank 1	Number of Column Addresses for Bank 2	Module Organization	Device Used	Byte 4 Contents
1	9, CA0-CA8	N/A	2M x 64	2M x 8	0000 1001
2	9, CA0-CA8	9, CA0-CA8	2 x 2M x 64	2M x 8	0000 1001
2	9, CA0-CA8	8, CA0-CA7	2M x 64 & 1M x 64	2M x 8 & 1M x 16	1000 1001

Byte 4, Subfield A: Number of Column Addresses on Bank 1, OR Number of Column Addresses on Bank 1 and 2 if both banks have the same depth (Bits 0-3)											
Line Number	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	
0A	Undefined	See Subfield B				0	0	0	0	0	_0
1A	1/16					0	0	0	1	_1	
2A	2/17					0	0	1	0	_2	
:	:					:	:	:	:	:	
7A	7					0	1	1	1	_7	
8A	8					1	0	0	0	_8	
9A	9					1	0	0	1	_9	
10A	10					1	0	1	0	_A	
11A	11					1	0	1	1	_B	
12A	12					1	1	0	0	_C	
13A	13					1	1	0	1	_D	
14A	14					1	1	1	0	_E	
15A	15					1	1	1	1	_F	

Byte 4, Subfield B: Number of Column Addresses on Bank 2 if banks have different depths (Bits 4-7)										
Line Number	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	No 2nd Asymmetric Bank	0	0	0	0	See Subfield A				0_
1B	1/16	0	0	0	1					1_
2B	2/17	0	0	1	0					2_
:	:	:	:	:	:					:
7B	7	0	1	1	1					7_
8B	8	1	0	0	0					8_
9B	9	1	0	0	1					9_
10B	10	1	0	1	0					A_
11B	11	1	0	1	1					B_
12B	12	1	1	0	0					C_
13B	13	1	1	0	1					D_
14B	14	1	1	1	0					E_
15B	15	1	1	1	1					F_



## Byte 5: Number of DIMM Banks

This field describes the number of physical banks on the SDRAM module. The number of logical banks for the SDRAM device is defined in Byte 17.

Line #	Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

## Bytes 6 and 7: Module Data Width

Bytes 6 and 7 are used to designate the module's data width. The data width is presented as a 16-bit word: bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit 7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 256 bits, byte 7 will be 00h. If the data width is 256 bits or more, byte 7 is used in conjunction with byte 6 to designate the total module width. For example:

If the module's Data Width is:	then Byte 7 is:	and Byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
576	0000 0010	0100 0000

## Byte 6: Module Data Width

Line #	Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	0	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
32	32	0	0	1	0	0	0	0	0	20
33	33	0	0	1	0	0	0	0	1	21
-	-	-	-	-	-	-	-	-	-	-
36	36	0	0	1	0	0	1	0	0	24
-	-	-	-	-	-	-	-	-	-	-
64	64	0	1	0	0	0	0	0	0	40
-	-	-	-	-	-	-	-	-	-	-
72	72	0	1	0	0	1	0	0	0	48
-	-	-	-	-	-	-	-	-	-	-
80	80	0	1	0	1	0	0	0	0	50
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
144	144	1	0	0	1	0	0	0	0	90
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

## Byte 7: Module Data Width Continuation

This byte will be left at 00h if the module data width is less than 256 bits wide. If the width is 256 or greater, then this byte will be used in conjunction with byte 6.

Line #	Data Width (cont'd)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Hex
0	0 (+)	0	0	0	0	0	0	0	0	00
1	256 (+)	0	0	0	0	0	0	0	1	01
2	512 (+)	0	0	0	0	0	0	1	X	02-03
3	1024 (+)	0	0	0	0	0	1	X	X	04-07
4	2048 (+)	0	0	0	0	1	X	X	X	08-15

X = 0 or 1.



## Byte 8: Voltage Interface Level of this assembly

This field describes the module's voltage interface.

Line #	Interface Levels	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	TTL/5V tolerant	0	0	0	0	0	0	0	0	00
1	LVTTL (not 5V tolerant)	0	0	0	0	0	0	0	1	01
2	HSTL 1.5V	0	0	0	0	0	0	1	0	02
3	SSTL 3.3V	0	0	0	0	0	0	1	1	03
4	SSTL 2.5V	0	0	0	0	0	1	0	0	04
5	TBD	0	0	0	0	0	1	0	1	05
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-



### Byte 9: SDRAM Cycle Time ( $t_{CYC}$ )

This byte defines the minimum cycle time for the SDRAM module at the highest  $\overline{CAS}$  Latency,  $\overline{CAS}$  Latency = X, defined in byte 18. If other  $\overline{CAS}$  latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. Byte 9, Cycle time for CAS Latency=X, is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example:

If bits 7:4 are	and bits 3:0 are	then the cycle time is:
1010	0101	
(10ns)	+ (0.5ns)	= 10.5ns

Byte 9, SDRAM Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)

Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1	F_				
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 9, SDRAM Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)

Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield Table B				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	RFU	1	0	1	0	_A				
-	-	-	-	-	-	-	-	-	-	
-	Undefined	1	1	1	1	1	1	1	1	FF

## Byte 10: SDRAM Access from Clock ( $t_{AC}$ )

This byte defines the maximum clock to data out for the SDRAM module. This is the Clock to data out specification at the highest given  $\overline{CAS}$  Latency specified in byte 18 of this SPD specification. If other  $\overline{CAS}$  latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of 1/10ns and is added to the value designated by the higher nibble. For example:

<b>if bits 7:4 are</b>	<b>and bits 3:0 are</b>	<b>then the access time is:</b>
1010	0101	
(10ns)	+ (0.5ns)	= 10.5ns

Byte 10: SDRAM Access from Clock, Subfield A: Whole Nanoseconds (Bits 4-7)											
Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	
0A	Undefined	0	0	0	0	See Subfield B				0_	
1A	1ns	0	0	0	1						1_
2A	2ns	0	0	1	0						2_
3A	3ns	0	0	1	1						3_
4A	4ns	0	1	0	0						4_
5A	5ns	0	1	0	1						5_
6A	6ns	0	1	1	0						6_
7A	7ns	0	1	1	1						7_
8A	8ns	1	0	0	0						8_
9A	9ns	1	0	0	1						9_
10A	10ns	1	0	1	0						A_
11A	11ns	1	0	1	1						B_
12A	12ns	1	1	0	0						C_
13A	13ns	1	1	0	1						D_
14A	14ns	1	1	1	0						E_
15A	15ns	1	1	1	1					F_	
-	Undefined	1	1	1	1	1	1	1	1	FF	

Byte 10: SDRAM Access from Clock Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+1ns					0	0	0	1	_1
2B	+2ns					0	0	1	0	_2
3B	+3ns					0	0	1	1	_3
4B	+4ns					0	1	0	0	_4
5B	+5ns					0	1	0	1	_5
6B	+6ns					0	1	1	0	_6
7B	+7ns					0	1	1	1	_7
8B	+8ns					1	0	0	0	_8
9B	+9ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF



## Byte 11: DIMM Configuration Type

This byte describes the module's error detection and/or correction scheme.

Line #	Error Detection/Correction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	None	0	0	0	0	0	0	0	0	00
1	Parity	0	0	0	0	0	0	0	1	01
2	ECC	0	0	0	0	0	0	1	0	02
3	TBD	0	0	0	0	0	0	1	1	03
4	TBD	0	0	0	0	0	1	0	0	04
5	TBD	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-

## Byte 12: Refresh Rate/Type

This byte describes the module's refresh rate and type.

Line #	Refresh Period	Bit 7 (Self Refresh Flag)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Normal (15.625 us)	0	0	0	0	0	0	0	0	00
1	Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1	01
2	Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0	02
3	Extended (2x)...31.3us	0	0	0	0	0	0	1	1	03
4	Extended (4x)...62.5us	0	0	0	0	0	1	0	0	04
5	Extended (8x)...125us	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
7	TBD	0	0	0	0	0	1	1	1	07
-	-	-	-	-	-	-	-	-	-	-
Self Refresh Entries										
128	Normal (15.625 us)	1	0	0	0	0	0	0	0	80
129	Reduced (.25x)...3.9us	1	0	0	0	0	0	0	1	81
130	Reduced (.5x)...7.8us	1	0	0	0	0	0	1	0	82
131	Extended (2x)...31.3us	1	0	0	0	0	0	1	1	83
132	Extended (4x)...62.5us	1	0	0	0	0	1	0	0	84
133	Extended (8x)...125us	1	0	0	0	0	1	0	1	85
134	TBD	1	0	0	0	0	1	1	0	86
135	TBD	1	0	0	0	0	1	1	1	87
-	-	-	-	-	-	-	-	-	-	-

### Byte 13: Primary SDRAM Width

Bits 0-6 of this byte indicate the width of the primary data SDRAM. Bit 7 is a flag which is set to “1” when there is a second physical bank on the module which is of different size from the first physical bank (the second physical bank’s data RAMs are 2X the width of those on the first physical bank). If there is a second physical bank of the same size and configuration as the first, then bit 7 remains as “0” and primary SDRAM width for both banks is expressed using bits 0-6. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, and x32. Note that if the module is made with SDRAMs which provide for data and error checking, e.g. x9, x18, and x36, then it is also designated in this field.

This table contains examples of SDRAM DIMM using 1 and 2 banks of symmetrical and asymmetrical size.

Module Width	Physical Bank 1 Primary SDRAM Width	Physical Bank 2 Primary SDRAM Width	Physical Bank 1 Error Checking SDRAM Width	Physical Bank 2 Error Checking SDRAM Width	Possible (16Mb based) Module Density	Byte 13 Contents
x72	x9	N/A	—	N/A	16MB	0000 1001
x72	x8	N/A	x8	N/A	16MB	0000 1000
x72	x16	N/A	x4	N/A	8MB	0001 0000
x72	x8	x8	x8	x8	32MB	0000 1000
x64	x8	x16	N/A	N/A	24MB	1000 1000

Byte 13, Subfield A: Data SDRAM Width								
Data SDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	See Subfield B	0	0	0	0	0	0	0
1		0	0	0	0	0	0	1
:		:	:	:	:	:	:	:
4		0	0	0	0	1	0	0
:		:	:	:	:	:	:	:
8		0	0	0	1	0	0	0
9		0	0	0	1	0	0	1
:		:	:	:	:	:	:	:
15		0	0	0	1	1	1	1
16		0	0	1	0	0	0	0
17		0	0	1	0	0	0	1
:		:	:	:	:	:	:	:
32		0	1	0	0	0	0	0
:		:	:	:	:	:	:	:
36		0	1	0	0	1	0	0
:		:	:	:	:	:	:	:
127	1	1	1	1	1	1	1	

Byte 13, Subfield B: Bank 2 Data SDRAM Width Multiplier								
Bank 2 Data SDRAM Width Multiple	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
No Bank 2 or Bank 2 uses same width SDRAM as Bank 1	0	See Subfield A						
Bank 2 SDRAM is 2X the width of Bank 1 SDRAM	1							

### Byte 14: Error Checking SDRAM Width

If the module incorporates error checking and if the primary data SDRAM does not include these bits — i.e. there are separate error checking SDRAMs — then the error checking SDRAM’s width is expressed in this



byte. Bits 0-6 of this byte relate the error checking SDRAM's width. Bit 7 is a flag set to "1" when the module has a second physical bank that is a different size than the first physical bank. Bit 7 set to "1" indicates that Bank 2's error checking RAMs are 2X the width of those on the first physical bank. If there is a second physical bank of the same size and configuration as the first, then bit 7 remains as "0" and error checking SDRAM width for both physical banks is expressed using bits 0-6.

The following table contains examples of error checking SDRAM widths using 1 and 2 banks of symmetrical and asymmetrical size.

Module Width	Physical Bank 1 Primary SDRAM Width	Physical Bank 2 Primary SDRAM Width	Physical Bank 1 Error Checking SDRAM Width	Physical Bank 2 Error Checking SDRAM Width	Possible (16Mb based) Module Density	Byte 14 Contents
x72	x9	N/A	—	N/A	16MB	0000 0000
x72	x8	N/A	x8	N/A	16MB	0000 1000
x72	x16	N/A	x4	N/A	8MB	0000 0100
x72	x8	x8	x8	x8	32MB	0000 1000
x72	x8	x16	x8	x16	24MB	1000 1000
x80	x8	x16	x8	x16	24MB	1000 1000

Byte 14, Subfield A: Error Checking SDRAM Width								
Error Checking SDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	See Subfield B	0	0	0	0	0	0	0
1		0	0	0	0	0	0	1
:		:	:	:	:	:	:	:
4		0	0	0	0	1	0	0
:		:	:	:	:	:	:	:
8		0	0	0	1	0	0	0
9		0	0	0	1	0	0	1
:		:	:	:	:	:	:	:
15		0	0	0	1	1	1	1
16		0	0	1	0	0	0	0
17		0	0	1	0	0	0	1
:		:	:	:	:	:	:	:
32		0	1	0	0	0	0	0
:		:	:	:	:	:	:	:
36		0	1	0	0	1	0	0
:	:	:	:	:	:	:	:	
63	1	1	1	1	1	1	1	

Byte 14, Subfield B: Bank 2 Error Checking SDRAM Width Multiplier								
Bank 2 Error Checking SDRAM Width Multiple	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
No Bank 2 or Bank 2 uses same width SDRAM as Bank 1	0	See Subfield A						
Bank 2 SDRAM is 2X the width of Bank 1 SDRAM	1							

**Byte 15: SDRAM Device Attributes – Minimum Clock Delay, Back-to-Back Random Column Access**

This byte describes the minimum Clock Delay for back-to-back random column accesses. Note that SDRAM architecture can be gained with this parameter. A latency of 1 for random writes denotes Pipelined SDRAM and a latency of 2 for random writes denotes Prefetch DRAMs.

Line #	Number of Clocks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

### Byte 16: SDRAM Device Attributes – Burst Lengths Supported

This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is “1”, then that Burst Length is supported on the module; if the bit is “0”, then that Burst Length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly, 0 = Not supported on this assembly.

### Byte 17: SDRAM Device Attributes – Number of Banks on SDRAM Device

This byte details how many banks are on each SDRAM installed onto the module.

Line #	Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF



### Byte 18: SDRAM Device Attributes – $\overline{\text{CAS}}$ Latency

This byte describes which of the programmable  $\overline{\text{CAS}}$  latencies are acceptable for the module. If the bit is “1”, then that  $\overline{\text{CAS}}$  latency is supported on the module; if the bit is “0”, then that  $\overline{\text{CAS}}$  latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	$\overline{\text{CAS}}$ Latency = 7	$\overline{\text{CAS}}$ Latency = 6	$\overline{\text{CAS}}$ Latency = 5	$\overline{\text{CAS}}$ Latency = 4	$\overline{\text{CAS}}$ Latency = 3	$\overline{\text{CAS}}$ Latency = 2	$\overline{\text{CAS}}$ Latency = 1
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly; 0 = Not supported on this assembly.

### Byte 19: SDRAM Device Attributes – $\overline{\text{CS}}$ Latency

This byte describes which of the programmable  $\overline{\text{CS}}$  latencies are acceptable for the module. If the bit is “1”, then that  $\overline{\text{CS}}$  latency is supported on the module; if the bit is “0”, then that  $\overline{\text{CS}}$  latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	$\overline{\text{CS}}$ Latency = 6	$\overline{\text{CS}}$ Latency = 5	$\overline{\text{CS}}$ Latency = 4	$\overline{\text{CS}}$ Latency = 3	$\overline{\text{CS}}$ Latency = 2	$\overline{\text{CS}}$ Latency = 1	$\overline{\text{CS}}$ Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly; 0 = Not supported on this assembly.

### Byte 20: SDRAM Device Attributes – $\overline{\text{WE}}$ Latency

This byte describes which of the programmable  $\overline{\text{WE}}$  latencies are acceptable for the module. If the bit is “1”, then that  $\overline{\text{WE}}$  latency is supported on the module; if the bit is “0”, then that  $\overline{\text{WE}}$  latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	$\overline{\text{WE}}$ Latency = 6	$\overline{\text{WE}}$ Latency = 5	$\overline{\text{WE}}$ Latency = 4	$\overline{\text{WE}}$ Latency = 3	$\overline{\text{WE}}$ Latency = 2	$\overline{\text{WE}}$ Latency = 1	$\overline{\text{WE}}$ Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly; 0 = Not supported on this assembly.

### Byte 21: SDRAM Modules Attributes

This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	* Redundant Addressing	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On-Card PLL (Clock)	** Registered Address and Control Inputs	** Buffered Address and Control Inputs
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Included on this assembly; 0 = Not included on this assembly.

\* Redundant addressing implies the use of SDRAMs having the same address depth (e.g. 4M x 4 mixed with 4M x 16) in the same 8 byte quad word, but having different  $\overline{RAS}/\overline{CAS}$  addressing and/or different numbers of device banks. Actual implementation is not yet determined.

\*\* Address,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{CKE}$ ,  $\overline{CS}$

### Byte 22: SDRAM Device Attributes – General

This byte depicts various aspects of the SDRAMs on the module. It details various unrelated but critical elements pertinent to the SDRAMs. A given SDRAM characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is "1". Conversely, if the aspect is FALSE, the designated bit is "0".

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	*Upper $V_{CC}$ tolerance: 0=10% 1=5%	*Lower $V_{CC}$ tolerance: 0=10% 1=5%	Supports Write1/Read Burst	Supports Precharge All	Supports Auto-Precharge	Supports Early $\overline{RAS}$ Precharge
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

1 = Included on this assembly; 0 = Not included on this assembly.

\* Tolerance refers to the voltage range under which the SDRAMs operate to the timings specified in the SPD bytes 9, 10, 23-30.



### Byte 23: Minimum Clock Cycle Time at Reduced $\overline{\text{CAS}}$ Latency, X-1

The highest  $\overline{\text{CAS}}$  latency identified in byte 18 is X and the timing values associated with  $\overline{\text{CAS}}$  latency 'X' are found at byte locations 9 and 10. Byte 23 denotes the minimum cycle time at  $\overline{\text{CAS}}$  latency X-1.

For example, if byte 18 denotes  $\overline{\text{CAS}}$  latencies of 1-3, then X is 3 and X-1 is 2. Byte 23 then denotes the minimum cycle time at  $\overline{\text{CAS}}$  latency 2.

Byte 23 is broken into two nibbles: the higher order nibble (bits 4-7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the cycle time is
1001	0101	
(9ns)	+ (0.5ns)	= 9.5ns

Byte 23, SDRAM Minimum Cycle Time @ CL X-1, Subfield A: Whole Nanoseconds (Bits 4-7)

Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	
0A	Undefined	0	0	0	0	See Subfield B				0_	
1A	1ns/16ns	0	0	0	1						1_
2A	2ns/17ns	0	0	1	0						2_
3A	3ns	0	0	1	1						3_
4A	4ns	0	1	0	0						4_
5A	5ns	0	1	0	1						5_
6A	6ns	0	1	1	0						6_
7A	7ns	0	1	1	1						7_
8A	8ns	1	0	0	0						8_
9A	9ns	1	0	0	1						9_
10A	10ns	1	0	1	0						A_
11A	11ns	1	0	1	1						B_
12A	12ns	1	1	0	0						C_
13A	13ns	1	1	0	1						D_
14A	14ns	1	1	1	0						E_
15A	15ns	1	1	1	1					F_	

Byte 23, SDRAM Minimum Cycle Time @ CL X-1, Subfield B: Tenths of Nanoseconds (Bits 0-3)

Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+1ns					0	0	0	1	_1
2B	+2ns					0	0	1	0	_2
3B	+3ns					0	0	1	1	_3
4B	+4ns					0	1	0	0	_4
5B	+5ns					0	1	0	1	_5
6B	+6ns					0	1	1	0	_6
7B	+7ns					0	1	1	1	_7
8B	+8ns					1	0	0	0	_8
9B	+9ns					1	0	0	1	_9
10B	RFU				1	0	1	0	_A	
-	.	.	.	.	.	.	.	.	.	.
-	Undefined	1	1	1	1	1	1	1	1	FF

## Byte 24: Maximum Data Access Time ( $t_{AC}$ ) from Clock at CLX-1

The highest  $\overline{CAS}$  latency identified in byte 18 is X. Byte 23 denotes the maximum access time from Clock at  $\overline{CAS}$  latency X-1.

For example, if byte 18 denotes supported  $\overline{CAS}$  latencies of 1-3, then X is 3 and X-1 is 2. Byte 24 then denotes the maximum clock access time from CLK at  $\overline{CAS}$  latency 2.

Byte 24 is broken into two nibbles: the higher order nibble (bits 4-7) designates the access time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of 1/10ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the cycle time is
1001	0101	
(9ns)	+ (0.5ns)	= 9.5ns

Byte 24, SDRAM Access Time from Clock @ CL X-1, Subfield A: Whole Nanoseconds (Bits 4-7)											
Line #	Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	
0A	Undefined	0	0	0	0	See Subfield B				0_	
1A	1ns/16ns	0	0	0	1						1_
2A	2ns/17ns	0	0	1	0						2_
3A	3ns/18ns	0	0	1	1						3_
4A	4ns	0	1	0	0						4_
5A	5ns	0	1	0	1						5_
6A	6ns	0	1	1	0						6_
7A	7ns	0	1	1	1						7_
8A	8ns	1	0	0	0						8_
9A	9ns	1	0	0	1						9_
10A	10ns	1	0	1	0						A_
11A	11ns	1	0	1	1						B_
12A	12ns	1	1	0	0						C_
13A	13ns	1	1	0	1						D_
14A	14ns	1	1	1	0						E_
15A	15ns	1	1	1	1					F_	

Byte 24, SDRAM Access Time from Clock @ CL X-1, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	RFU				1	0	1	0	_A	
-	.	.	.	.	.	.	.	.	.	.
	Undefined	1	1	1	1	1	1	1	1	.



## Byte 25: Minimum Clock Cycle Time at CLX-2

The highest  $\overline{\text{CAS}}$  latency identified in byte 18 is X. Byte 25 denotes the minimum cycle time at  $\overline{\text{CAS}}$  latency X-2.

For example, if byte 18 denotes  $\overline{\text{CAS}}$  latencies of 1-3, then X is 3 and X-2 is 1. Byte 25 then denotes the minimum cycle time at  $\overline{\text{CAS}}$  latency 1.

Byte 25 is broken into two pieces: the higher order bits (bits 2-7) designate the cycle time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of 1/4ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the cycle time is
011001 (25ns)	00 +(0.0ns)	=25.0ns
100001 (33ns)	11 +(.75)	=33.75ns

Byte 25, SDRAM Minimum Cycle Time @ CL = X-2, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 25, SDRAM Minimum Cycle Time @ CL = X-2, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+0ns	See Subfield A						0	0
+.25ns							0	1
+50ns							1	0
+75ns							1	1

## Byte 26: Maximum Data Access Time ( $t_{AC}$ ) from Clock at CL X-2

The highest  $\overline{CAS}$  latency identified in byte 18 is X. Byte 26 denotes the maximum access time from Clock at  $\overline{CAS}$  latency X-2.

For example, if byte 18 denotes supported  $\overline{CAS}$  latencies of 1-3, then X is 3 and X-2 is 1. Byte 26 then denotes the maximum data access time from CLK at  $\overline{CAS}$  latency 1.

Byte 25 is broken into two pieces: the higher order bits (bits 2-7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-1) has a granularity of 1/4ns and is added to the value designated by the higher nibble. For example:

if bits 7:2 are	and bits 1:0 are	then the cycle time is
001001 (9ns)	01 +(0.25ns)	=9.250ns

Byte 26, SDRAM Access Time from Clock @ CL = X-2, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 26, SDRAM Access Time from Clock @ CL = X-2, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1



## Byte 27: Minimum Row Precharge Time (tRP)

Byte 27 is used to designate the module's minimum Row Precharge time.

Minimum Row Precharge Time (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

### Byte 28: Minimum Row Active to Row Active Delay ( $t_{RRD}$ )

This field describes the minimum required delay between different row activations.

Minimum Row Active to Row Active Delay (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
19	0	0	0	1	0	0	1	1	13
20	0	0	0	1	0	1	0	0	14
21	0	0	0	1	0	1	0	1	15
22	0	0	0	1	0	1	1	0	16
23	0	0	0	1	0	1	1	1	17
24	0	0	0	1	1	0	0	0	18
25	0	0	0	1	1	0	0	1	19
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF



## Byte 29: Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay ( $t_{\text{RCD}}$ )

This byte describes the minimum delay required between assertions of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ .

Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF



### Byte 30: Minimum $\overline{\text{RAS}}$ Pulse Width ( $t_{\text{RAS}}$ )

This byte identifies the minimum  $\overline{\text{RAS}}$  pulse width.

Minimum $\overline{\text{RAS}}$ Pulse Width (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF



### Byte 31: Module Bank Density

This byte describes the density of each physical bank on the SRAM DIMM. This byte will have at least one bit set to “1” to represent at least one bank’s density. If there are more than one bank on the module (as represented in byte #5), and they have the same density, then only one bit is set in this field. If the module has more than one bank of different sizes, then more than one bit will be set; each bit set for each density represented. For example:

Number of Banks	Density of Bank 1	Density of Bank 2	Byte 3 Contents
1	32MB	N/A	0000 1000
2	32MB	32MB	0000 1000
2	32MB	16MB	0000 1100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512MB	256MB	128MB	64MB	32MB	16MB	8MB	4MB
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

1 = Supported on this assembly; 0 = Not supported on this assembly.

## Byte 32: Address and Command Setup Time Before Clock

This field describes the input setup time before the rising edge of the clock. Since this value can be either negative or positive, provisions have been made to accommodate both. If the byte starts with a zero in bit 7, then the input setup time is positive. If the byte starts with a one in bit 7, then the value is negative. For example:

If bits 7:4 are	and bits 3:0 are	then the cycle time is:
0010 (+2ns)	0101 (0.5ns)	= +2.5ns
1010 (-2ns)	0101 (0.5ns)	= -2.5ns

Byte 32, Input Setup Time Before Clock, Subfield A: Units of Nanoseconds (Bits 4-7)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	>0, <1ns	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	>-1, <0ns	1	0	0	0					8_
9A	-1ns	1	0	0	1					9_
10A	-2ns	1	0	1	0					A_
11A	-3ns	1	0	1	1					B_
12A	-4ns	1	1	0	0					C_
13A	-5ns	1	1	0	1					D_
14A	-6ns	1	1	1	0					E_
15A	-7ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 32, Input Setup Time Before Clock, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	±0ns	See Subfield Table A				0	0	0	0	_0
1B	±0.1ns					0	0	0	1	_1
2B	±0.2ns					0	0	1	0	_2
3B	±0.3ns					0	0	1	1	_3
4B	±0.4ns					0	1	0	0	_4
5B	±0.5ns					0	1	0	1	_5
6B	±0.6ns					0	1	1	0	_6
7B	±0.7ns					0	1	1	1	_7
8B	±0.8ns					1	0	0	0	_8
9B	±0.9ns					1	0	0	1	_9
10B	RFU	1	0	1	0	_A				
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF



### Byte 33: Address and Command Hold Time After Clock

This field describes the input hold times after the rising edge of the clock. Since this value can be either negative or positive, provisions have been made to accommodate both. If the byte starts with a zero in bit 7, then the input hold time is positive. If the byte starts with a one in bit 7, then the value is negative. For example:

If bits 7:4 are	and bits 3:0 are	then the cycle time is:
0010 (+2ns)	0101 (0.5ns)	= +2.5ns
1010 (-2ns)	0101 (0.5ns)	= -2.5ns

Byte 32, Input Hold Time After Clock, Subfield A: Units of Nanoseconds (Bits 4-7)

Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	>0, <1ns	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	>-1, <0ns	1	0	0	0					8_
9A	-1ns	1	0	0	1					9_
10A	-2ns	1	0	1	0					A_
11A	-3ns	1	0	1	1					B_
12A	-4ns	1	1	0	0					C_
13A	-5ns	1	1	0	1					D_
14A	-6ns	1	1	1	0					E_
15A	-7ns	1	1	1	1	F_				
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 32, Input Hold Time After Clock, Subfield B: Tenths of Nanoseconds (Bits 0-3)

Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	±0ns	See Subfield Table A				0	0	0	0	_0
1B	±0.1ns					0	0	0	1	_1
2B	±0.2ns					0	0	1	0	_2
3B	±0.3ns					0	0	1	1	_3
4B	±0.4ns					0	1	0	0	_4
5B	±0.5ns					0	1	0	1	_5
6B	±0.6ns					0	1	1	0	_6
7B	±0.7ns					0	1	1	1	_7
8B	±0.8ns					1	0	0	0	_8
9B	±0.9ns					1	0	0	1	_9
10B	RFU	1	0	1	0	_A				
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

### Byte 34: Data Input Setup Time Before Clock

This field describes the input setup time before the rising edge of the clock. Since this value can be either negative or positive, provisions have been made to accommodate both. If the byte starts with a zero in bit 7, then the input setup time is positive. If the byte starts with a one in bit 7, then the value is negative. For example:

If bits 7:4 are	and bits 3:0 are	then the cycle time is:
0010 ( $\tau_{\text{CIIS}}$ )	0101 (0.5ns)	= +2.5ns
1010 (-2ns)	0101 (0.5ns)	= -2.5ns

Byte 32, Input Setup Time Before Clock, Subfield A: Units of Nanoseconds (Bits 4-7)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	>0, <1ns	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	>-1, <0ns	1	0	0	0					8_
9A	-1ns	1	0	0	1					9_
10A	-2ns	1	0	1	0					A_
11A	-3ns	1	0	1	1					B_
12A	-4ns	1	1	0	0					C_
13A	-5ns	1	1	0	1					D_
14A	-6ns	1	1	1	0					E_
15A	-7ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 32, Input Setup Time Before Clock, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	$\pm 0$ ns	See Subfield Table A				0	0	0	0	_0
1B	$\pm 0.1$ ns					0	0	0	1	_1
2B	$\pm 0.2$ ns					0	0	1	0	_2
3B	$\pm 0.3$ ns					0	0	1	1	_3
4B	$\pm 0.4$ ns					0	1	0	0	_4
5B	$\pm 0.5$ ns					0	1	0	1	_5
6B	$\pm 0.6$ ns					0	1	1	0	_6
7B	$\pm 0.7$ ns					0	1	1	1	_7
8B	$\pm 0.8$ ns					1	0	0	0	_8
9B	$\pm 0.9$ ns					1	0	0	1	_9
10B	RFU	1	0	1	0	_A				
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

## Byte 35: Data Input Hold Time After Clock

This field describes the input hold times after the rising edge of the clock. Since this value can be either negative or positive, provisions have been made to accommodate both. If the byte starts with a zero in bit 7, then the input hold time is positive. If the byte starts with a one in bit 7, then the value is negative. For example:

If bits 7:4 are	and bits 3:0 are	then the cycle time is:
0010 (+2ns)	0101 (0.5ns)	= +2.5ns
1010 (-2ns)	0101 (0.5ns)	= -2.5ns

**Byte 32, Input Hold Time After Clock, Subfield A: Units of Nanoseconds (Bits 4-7)**

Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex																																																								
0A	>0, <1ns	0	0	0	0	See Subfield Table B				0_																																																								
1A	1ns	0	0	0	1									1_																																																				
2A	2ns	0	0	1	0													2_																																																
3A	3ns	0	0	1	1																	3_																																												
4A	4ns	0	1	0	0																					4_																																								
5A	5ns	0	1	0	1																									5_																																				
6A	6ns	0	1	1	0																													6_																																
7A	7ns	0	1	1	1																																	7_																												
8A	>-1, <0ns	1	0	0	0																																					8_																								
9A	-1ns	1	0	0	1																																									9_																				
10A	-2ns	1	0	1	0																																													A_																
11A	-3ns	1	0	1	1																																																	B_												
12A	-4ns	1	1	0	0																																																					C_								
13A	-5ns	1	1	0	1																																																									D_				
14A	-6ns	1	1	1	0																																																													E_
15A	-7ns	1	1	1	1																																																													
-	Undefined	1	1	1	1	1	1	1	1																																																									

**Byte 32, Input Hold Time After Clock, Subfield B: Tenths of Nanoseconds (Bits 0-3)**

Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex																																
0B	±0ns	See Subfield Table A				0	0	0	0	_0																																
1B	±0.1ns									0	0	0	1	_1																												
2B	±0.2ns													0	0	1	0	_2																								
3B	±0.3ns																	0	0	1	1	_3																				
4B	±0.4ns																					0	1	0	0	_4																
5B	±0.5ns																									0	1	0	1	_5												
6B	±0.6ns																													0	1	1	0	_6								
7B	±0.7ns																																	0	1	1	1	_7				
8B	±0.8ns																																					1	0	0	0	_8
9B	±0.9ns																																									1
10B	RFU																																									1
-	-					-	-	-	-																																	-
-	Undefined					1	1	1	1	1	1	1	1																													FF

## Bytes 36-61: Superset Information

If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in these bytes.

## Byte 62: SPD Revision

This byte defines the revision level of the SPD JEDEC standard definition, which is currently 02h. After the SPD definition is updated, it will be necessary to specify which version of SPD is depicted.

SPD Revision	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Initial Release	0	0	0	0	0	0	0	0	00
Revision 1	0	0	0	0	0	0	0	1	01
Revision 2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.

## Byte 63: Checksum for Bytes 0-62

This field designates the checksum for checking data integrity (similar to parity) for bytes 0 - 62. It is written during module production and can be used by the customer to verify the data integrity for these bytes.

### Process for Calculating the Checksum

1. Convert binary information, in byte locations 0 - 62, to decimal.
2. Add together (sum) all decimal values for addresses 0 - 62.
3. Divide sum by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in address 63 as "Checksum."

Note: The same result can be obtained by adding the binary values in addresses 0 - 62 and eliminating all but the low order byte. The low order byte is the "Checksum."

### Example of a Checksum Calculation

SPD Byte Address	Serial PD		Convert to Decimal
0	0010 0100	→	36
1	1111 1110	→	+254
2	0000 0000	→	+ 0
3	0000 0000	→	+ 0
↓	↓	→	+ 0
		→	+ 0
60	0000 0000	→	+ 0
61	0000 0000	→	+ 0
62	0000 0000	→	+ 0
Decimal Total	-	-	290
Divide by 256	-	-	1
Remainder	-	-	34
Convert to binary	0010 0010	←	34
63 (Checksum)	0010 0010	-	-

## Bytes 64-71: Module Manufacturer's JEDEC ID Code

Manufacturers of a given module may include their identifier according to JEDEC spec JEP106. The first byte is utilized, the second byte is filling. The information coded in these bytes for IBM is "A4000000 00000000."

## Byte 72: Module Manufacturing Location

Manufacturers may include an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

**Bytes 73-90: Module Part Number**

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (20h).

**Bytes 91-92: Module Revision Code**

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

**Bytes 93-94: Module Manufacturing Date**

The module manufacturer may include a date code for the module. The JEDEC definitions of bytes 93 and 94 are year and week, respectively. However, since these bytes are optional, IBM products had implemented byte 93 as week and byte 94 as year, prior to the year 1998. These bytes are coded in binary. For example, week 19 in 1997 would be coded as: 13h (byte 93) and 61h (byte 94) and week 19 in 1998 would be coded as 62h (byte 93) and 13h (byte 94).

**Bytes 95-98: Module Serial Number**

The supplier may include a serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

**Bytes 99-125: Manufacturer's Specific Data**

The module manufacturer may include any additional information desired into the module within these locations.

**Bytes 126-127: Reserved**

These bytes are reserved and cannot be allocated at any time.

**Bytes 128-255: Open for Customer Use**

These bytes are unused by the manufacturer and are open for customer use.

## Example:

This is an example of the SPD data for the single bank 8M x 64 (IBM13N8644HC-10T) and 8M x 72 (IBM13N8734HC-10T) 168 pin Unbuffered SDRAM DIMMs using 8M x 8 SDRAM devices with 12/9/2 addressing.

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	9	09	
5	Number of DIMM Banks	1	01	
6 - 7	Data Width of Assembly	8M x 64	x64	4000
		8M x 72	x72	4800
8	Voltage Interface Level of this Assembly	LVTTTL	01	
9	SDRAM Device Cycle Time at CL=3	10.0ns	A0	
10	SDRAM Device Access Time from Clock at CL=3	8.0ns	80	
11	DIMM Configuration Type	8M x 64	Non-Parity	00
		8M x 72	ECC	02
12	Refresh Rate/Type	SR/1x(15.625us)	80	
13	Primary SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	8M x 64	N/A	00
		8M x 72	x8	08
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	2, 3	06	
19	SDRAM Device Attributes: $\overline{\text{CS}}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{\text{WE}}$ Latency	0	01	
21	SDRAM Module Attributes	Unbuffered	00	
22	SDRAM Device Attributes: General	Wr-1/Rd Burst, Precharge All, Auto-Precharge, $V_{DD} \pm 10\%$	0E	
23	Minimum Clock Cycle at CL=2	15.0ns	F0	
24	Maximum Data Access Time ( $t_{AC}$ ) from Clock at CL=2	9.0ns	90	
25	Minimum Clock Cycle Time at CL=1	N/A	00	
26	Maximum Data Access Time ( $t_{AC}$ ) from Clock at CL=1	N/A	00	
27	Minimum Row Precharge Time ( $t_{RP}$ )	30ns	1E	
28	Minimum Row Active to Row Active delay ( $t_{RRD}$ )	20ns	14	
29	Minimum RAS to CAS delay ( $t_{RCD}$ )	30ns	1E	
1. cc = Checksum Data byte, 00-FF (Hex) 2. "R" = Alphanumeric revision code, A-Z, 0-9 3. rr = ASCII coded revision code byte "R" 4. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex) 5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex) 6. ss = Serial number data byte, 00-FF (Hex)				



**SDRAM Module Serial Presence Detect Definitions**

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
30	Minimum $\bar{R}AS$ Pulse width ( $t_{RAS}$ )	60ns	3C	
31	Module Bank Density	64MB	10	
32	Address and Command Setup Time Before Clock	3.0ns	30	
33	Address and Command Hold Time After Clock	1.0ns	10	
34	Data Input Setup Time Before Clock	3.0ns	30	
35	Data Input Hold Time After Clock	1.0ns	10	
36 - 61	Reserved	Undefined	00	
62	SPD Revision	2	02	
63	Checksum for bytes 0 - 62	Checksum Data	cc	1
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Module Part Number	8Mx64 ASCII'13N8644HC"R"-10T'	31334E383634344843rr 2D31305420202020	2,3
		8Mx72 ASCII'13N8734HC"R"-10T'	31334E38373334484rr 2D31305420202020	2, 3
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	4, 5
95 - 98	Module Serial Number	Serial Number	ssssssss	6
99 - 125	Reserved	Undefined	00	
126	Module Supports this Clock Frequency	66 MHz	66	
127	Attributes for Clock Frequency defined in byte 126	CL3, CL2	06	
128 - 255	Open for Customer Use	Undefined	00	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)



## ASCII Decode Matrix for SPDs

The following table is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

First Hex Digit in Pair	Second Hex Digit in Pair															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	Blank Space							(	)					- Dash		
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

**Examples:**

20h=Blank Space

34h=4

41h=A

SPD Bytes 73-90	
Manufacturer's PN	Coded in ASCII
13M32734BCD-260Y	31334D33323733344243442D323630592020