Low-Voltage Differential Signaling

Definition

Low-voltage differential signaling (LVDS) uses high-speed analog circuit techniques to provide multigigabit data transfers on copper interconnects and is a generic interface standard for high-speed data transmission. The American National Standards Institute (ANSI)/Telecommunications Industry Association (TIA)/Electronic Industries Alliance (EIA)–644-1995 standard specifies the physical layer as an electronic interface. This standard defines driver and receiver electrical characteristics only. It does not define protocol, interconnect, or connector details because these details are application-specific. The LVDS Standard's Working Group chose to define only the electrical characteristics to ensure that LVDS becomes a multipurpose interface standard. Therefore, each application that uses LVDS should also reference the appropriate protocol and interconnect standard.

Overview

This tutorial discusses the technological advantages that LVDS brings to highspeed digital data transfer (100 Mbps and higher) applications.

Topics

Glossary

1. Introduction

As a result of the Internet's tremendous growth, data transfers are increasing dramatically in all areas of communications. In addition, data streams for digital video, high-definition television (HDTV), and color graphics are requiring higher and higher bandwidth. The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards, and systems. The data may be digital, but it is LVDS that designers are choosing to drive these high-speed transmission lines. LVDS's proven speed, low power, noise control, and cost advantages are popular in point-to-point applications for telecommunications, data communications, and displays.

Wherever you need high-speed data transfer (100 Mbps and higher), LVDS offers a solution. There are many applications in many market segments that use LVDS for data transmission. These include the following:

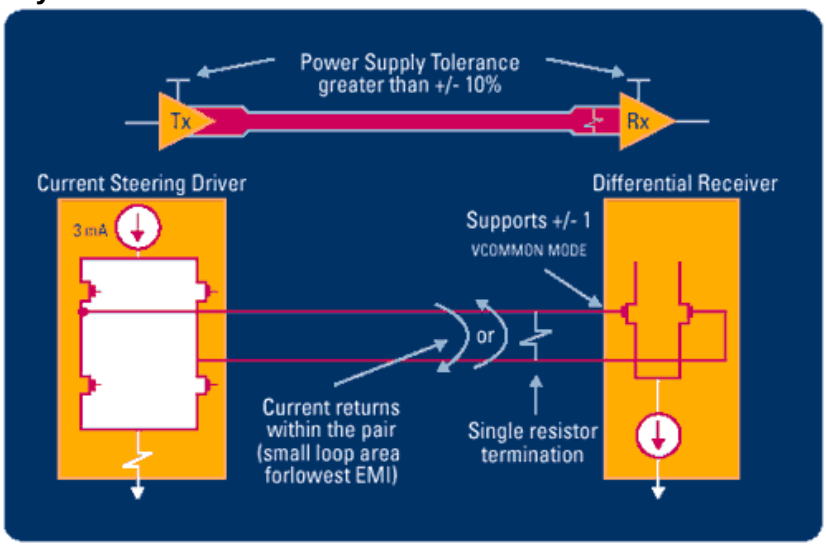
- stackable hubs for data communications
- wireless base stations and asynchronous transfer mode (ATM) switches in telecommunications
- flat-panel displays and servers in the computer market
- peripherals like printers and digital copy machines
- high-resolution displays in industrial applications
- flat-panel displays in the automotive market

In these applications, high-speed data moves within and between systems. Moving data within a system (intrasystem data transfer) is the main use for LVDS solutions today. Moving information between systems (intersystem data transfer) requires standard communications protocols such as Institute of Electrical and Electronic Engineers (IEEE) 1394, Fibre Channel, and Gigabit Ethernet. As the hardware and software overhead for intersystem protocols is too expensive to use for intrasystem data transfers, a simple and low-cost LVDS link is an attractive alternative. Thus, LVDS solutions move information on a board; between boards, modules, shelves, and racks; or box to box. The transmission media can be copper cables or printed circuit board (PCB) traces. In the future, LVDS will also carry protocols for intersystem communication.

2. LVDS Physical Layer

The equivalent circuit structure of the LVDS physical layer is shown in *Figure 1*. In the driver, a current source limits output to about 3 mA, and a switch box steers the current through the termination resistor. This differential driver produces odd-mode transmission: equal and opposite currents flow in the transmission lines. The current returns within the wire pair, so the current loop area is small and therefore generates the lowest amount of electromagnetic interference (EMI). The current source limits any spike current that could occur during transitions. Because there are no spike currents, data rates as high as 1.5 Gbps are possible without a substantial increase in power dissipation. In addition, the constant current driver output can tolerate transmission lines shorted together or to ground without creating thermal problems.

Figure 1. The Equivalent Circuit Structure of the LVDS Physical Layer



The differential receiver is a high-impedance device that detects differential signals as low as 20 mV and then amplifies them into standard logic levels. The signal has a typical driver offset of 1.2 V, and the receiver accepts an input range of ground to 2.4 V. This allows rejection of common-mode noise picked up along the interconnect of up to ± 1 V.

In addition, hot plugging of LVDS drivers and receivers is possible because the constant current drive eliminates damage potential. Another feature is the receiver's failsafe function, which prevents output oscillations when the input pins are floating.

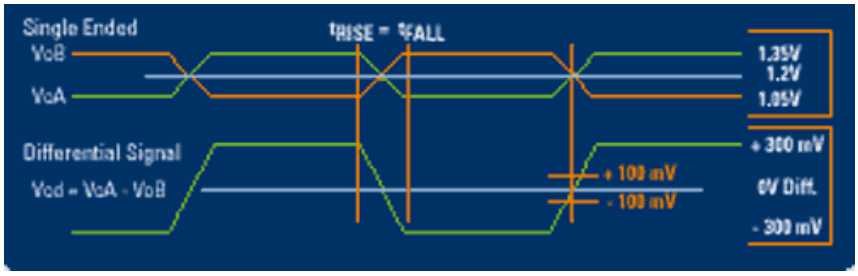
3. Multiple Technologies and Supply Voltages

When choosing the signal-level voltages for drivers and receivers, the standards committee considered LVDS implementation in technologies such as bipolar, complementary metal oxide semiconductor (BiCMOS), and even GaAs. In addition, the working group targeted a wide range of power supplies (such as 5 V, 3.3 V, and 2.5 V) for implementing LVDS to ensure that LVDS would be the interface of choice for future generations of products.

Low-voltage signals have many advantages, including fast bit rates, lower power, and better noise performance. Design engineers have previously used full-swing CMOS and low-voltage, transistor-transistor logic (LVTTL), but as bit rates increase, these solutions become unattractive. More recently, designers have turned to reduced-swing technologies such as stub series terminated logic (SSTL) and gunning transceiver logic (GTL) to gain speed, save power, and reduce noise. LVDS increases these advantages by lowering voltage swings to about 300 mV. To increase noise immunity and noise margins even further, LVDS uses differential data transmission. Differential signals are immune to common-mode noise, the primary source of system noise. Because its voltage change between logic states is only 300 mV, LVDS can change states very fast. An LVDS signal also changes voltage levels without a fast slew rate. Slowing the transition rate decreases the radiated field strength. Slower transitions reduce the problem of reflections from transmission-path impedance discontinuities, decreasing emissions and crosstalk problems. Low-voltage swing reduces power consumption because it lowers the voltage across the termination resistors and lowers the overall power dissipation.

Figure 2 emphasizes the advantage of a low-voltage swing for higher performance. For example, when the signal level changes 300 mV in 333 ps, the slew rate is only 0.9 V/ns, which is less than the 1 V/ns benchmark slew rate commonly acceptable for minimizing signal distortion and crosstalk. If you use the old benchmark that rise and fall times should be no more than two-thirds of the bit width, then signals with 333-ps transitions can operate as high as 1 Gbps with plenty of margin.

Figure 2. The Lowered Voltage Swing Maintains High Speed without Excessive Slew Rate



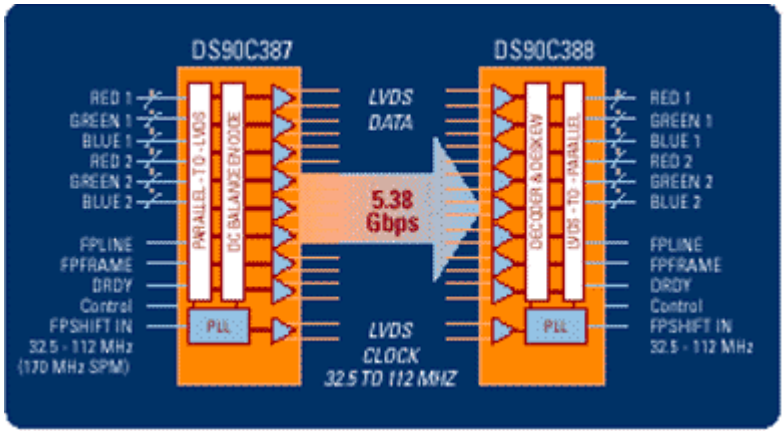
4. Gigabits at Milliwatts

The simple phrase “Gigabits at milliwatts” conveniently describes the benefits of an LVDS system. These benefits are high-speed data throughput, power-miser operation, noise control, low cost, and higher integration.

LVDS system features, such as serializing data, encoding the clock, and low skew, all work together for higher performance. Skew is a big problem for sending parallel data and its clock across cables or PCB traces. The problem is that the phase relation of the data and clock can be lost as a result of different travel times through the link. However, the ability to serialize parallel data into a high-speed signal with embedded clock eliminates the skew problem. The problem disappears because the clock travels with the data over the same differential pair of wires. The receiver uses clock and data recovery to extract the embedded clock, which is phase-aligned to the data.

An example of LVDS’s high performance is the open LVDS display interface (OpenLDI) chipset that supports 24-bit color and provides throughput of over 5 Gbps using only eight data pairs and a clock pair (see *Figure 3*). The chipset serializes a 48-bit TTL interface down to the eight pairs and then deserializes it at the receiver. The chipset supports TTL clock rates of up to 112 MHz. To do this, each LVDS data channel serializes six TTL lines, plus a direct current (DC) balance bit, into a single high-speed LVDS pair. That pair operates at 784 Mbps with a data throughput of 672 Mbps. The OpenLDI chipset can also operate at TTL bit rates as low as 33 Mbps.

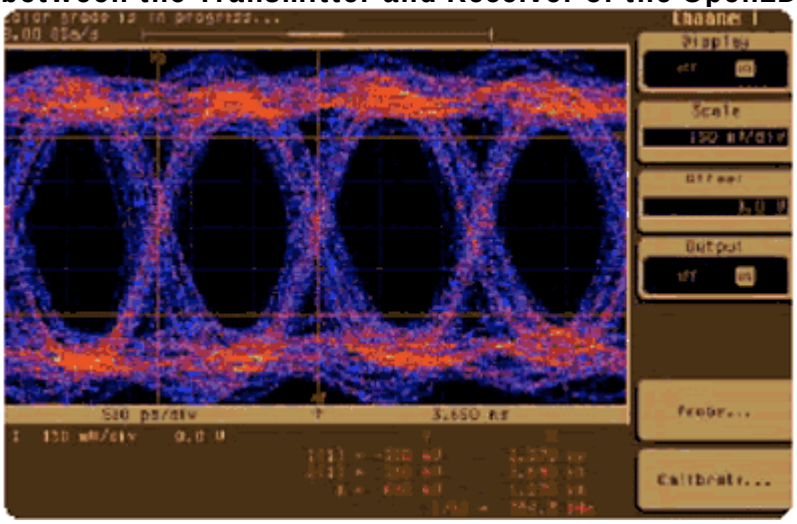
Figure 3. The OpenLDI Chipset Is an Example of LVDS’s High Performance



Besides giving tremendous throughput, the chipset reduces the interconnect width and provides other system benefits. The cable and connector are smaller and cost less; the cable is more flexible, and the connector has fewer pins. The beautiful eye pattern in *Figure 4* is taken at the end of a 5-meter cable between the transmitter and receiver of the OpenLDI chipset. The transmitter drives a

pseudo random bit sequence (PRBS) through the cable, and the receiver recovers the signal. The markers show the bit width to be 1.275 ns, indicating a data rate of 784 Mbps. Each of the 8 pairs carries this raw data rate, resulting in an aggregate bandwidth of almost 6.3 Gbps. This data rate includes overhead for DC balance, so the actual payload bandwidth is 5.38 Gbps.

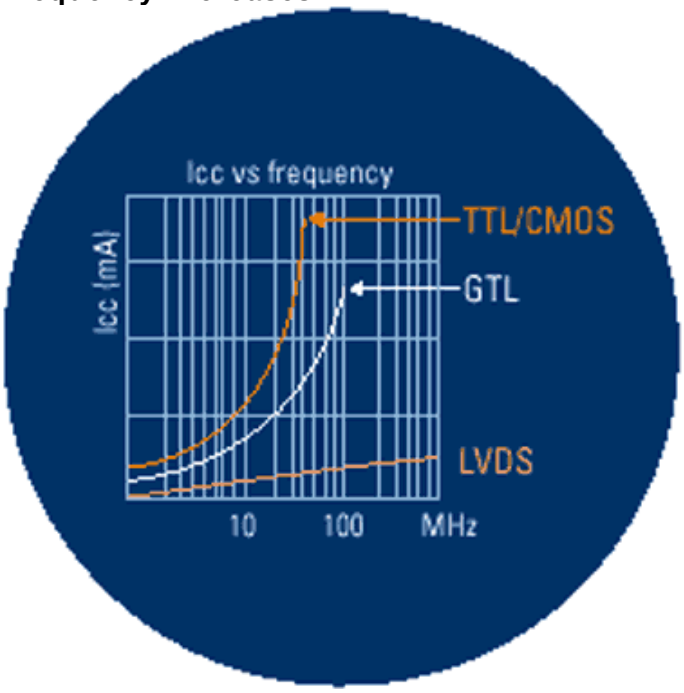
Figure 4. Eye Pattern Measured at the End of a 5-Meter Cable between the Transmitter and Receiver of the OpenLDI Chipset



5. Flat Supply Current versus Operating Frequency

A significant advantage of LVDS technology is the lower power requirement. *Figure 5* shows LVDS's supply current remaining flat as the operating frequency increases, whereas the supply current for CMOS and GTL technology increases exponentially as frequency increases. LVDS benefits because it uses a constant-current line driver rather than a voltage-mode driver. The load power calculation (3.3 mA times the 330-mV drop across the 100-W termination resistor) means LVDS has only 1.1–mW load power consumption. By comparison, GTL consumes 40 mA of load current through a 1-V drop across the load resistor, which is a whopping 40–mW load power dissipation. LVDS also has low-power requirements compared to pseudo emitter coupled logic (PECL). The DS90C031 is an LVDS pin-compatible replacement part for the PECL 41L quad differential line driver. The LVDS part consumes 16 times less supply current than the PECL part (3 mA compared to 50 mA). Furthermore, the low power consumption inherent in LVDS technology eliminates the need for either heat sinks or special packaging. This benefit also reduces the system cost of Gigabit data transfers.

Figure 5. LVDS's Supply Current Remains Flat as the Operating Frequency Increases



Another advantage of LVDS is its low electromagnetic-interference generation. The reasons LVDS generates low emissions are its low voltage swing, slow edge rates, the odd-mode differential signals, and the minimal I_{cc} spikes from constant current drivers. High-frequency signal transitions flowing through a transmission path create electromagnetic fields that radiate emissions. The field's strength is proportional to the energy carried by the signal. By reducing the voltage swing and the current energy, LVDS minimizes these fields. However, even the reduced electromagnetic fields can cause radiation problems.

6. Low Electromagnetic Interference

Differential signal paths reduce the harmful effects of these fields to minimize these radiation problems further. Balanced differential lines have equal but opposite currents, called odd-mode signals. When the fields created by these odd-mode signals are closely coupled, they tend to tie each other up and thus cannot escape to cause harm. Therefore, it is important to maintain a balanced and closely coupled differential transmission path to reduce the emission of electromagnetic interference. Differential signals also have the advantage of tolerating interference from outside sources such as inductive radiation from electric motors or crosstalk from neighboring transmission lines. When the differential transmission lines are closely coupled, the induced signal is common-mode noise that appears as a common-mode voltage at the receiver input. The differential receiver responds only to the difference between the plus and the minus inputs, so when the noise appears commonly to both inputs, the input

differential signal amplitude is undisturbed. This common-mode noise rejection also applies to noise sources such as power supply variations, substrate noise, and ground bounce.

The LVDS flat panel display (FPD) link standard shown in *Figure 6* demonstrates the low noise-generation characteristics for LVDS while targeting LCD applications for notebook and subnotebook computers. The FPD link moves large amounts of display data from the notebook personal computer (PC) to the display panel. The system designers had to solve the problem of twisted-pair cables or flex circuit carrying high-speed data through the panel hinge without creating EMI problems. They chose to use LVDS technology because it has better EMI performance than all other interface technologies.

7. Cost Benefits

All of the LVDS advantages discussed so far also benefit system cost. There are even more system cost savings from using LVDS. The first is LVDS's ability to tolerate minor impedance mismatches in transmission paths. As long as the differential signal passes through balanced discontinuities in closely coupled transmission paths, the signal can maintain integrity. The effect of nonimpedance-controlled connectors, PCB vias, and chip packaging is not as detrimental to differential signals as it is to single-ended signals. In addition, it is possible to use fewer circuit board layers because of the relative immunity to crosstalk that is inherent in differential signals.

LVDS requires only a simple termination resistor, which can be integrated onto the chip. This costs much less than using multiple resistor and capacitor components for each transmission line. In addition, LVDS requires no termination or V_{ddq} voltage supply, a big cost savings over technologies such as GTL, LVTTL, and stub series terminated logic (SSTL).

Because LVDS is capable of handling the high-speed data that results from serializing many parallel bits into a single data stream, LVDS chips commonly integrate serializers and deserializers. This saves about 50 percent of the cabling, connector, and PCB costs when compared to a parallel interconnect. The FPD–link chipset demonstrates this system cost savings. The chipset takes the 18- or 24-bit-wide red/green/blue (RGB) bus, and the VSYNC, HSYNC, and data enable control lines and multiplexes them down to only four or five pairs. This low-cost four- or five-pair link passes data through the hinge to the panel where it is demultiplexed. Typical interconnects range from about 8 cm to 40 cm in length and use low-cost flex circuit or twisted-pair cabling.

The final LVDS system benefit is its integration capability. Because it is possible to implement high-speed LVDS in a standard CMOS process, integrating complex

digital functions with LVDS's analog circuits is very beneficial. Integrating serializers and deserializers is only the beginning to mixed-signal LVDS chips.

8. Many Channels per Chip

LVDS's low power consumption enables integrating many channels per chip. For example, it is possible to serialize a 128-bit, on-chip parallel bus down to eight differential channels. This narrower link dramatically reduces pin count and total link cost. Integration also benefits from differential signals. These signals tolerate high levels of switching noise, so they can be reliably integrated with large-scale digital circuits. In addition, LVDS generates very little noise as a result of the constant-current nature of the output structures. Therefore, complete interface systems-on-a-chip are feasible. Digital blocks for integration include DC balance, clock embedding, clock recovery, encoders and decoders, and de-skew blocks. Higher-level digital functions such as hardware protocol assist, management and statistics counters, and routing decision logic are also using LVDS–on-chip as the interface of choice. Further integration of the blocks shown in the FPD–link chipset (see *Figure 6*) is already happening. Obvious candidates for integration are the LVDS transmitter with the VGA controller and the LVDS receiver with the timing controller.

Figure 6. The LVDS FPD Link Moves Large Amounts of Data from the Notebook PC to the Display Panel

The OpenLDI chipset supports cable lengths up to 10 meters by integrating special functions. These functions are transmitter pre-emphasis, DC balance coding, and cable deskew. They all work to extend the reach and bandwidth of OpenLDI interconnects to flat-panel-monitor applications that may require longer cables.

9. DC Balance for Longer Cables

The OpenLDI chipset implements a simple DC balancing scheme that reduces intersymbol interference (ISI). This demonstrates integrating digital functions onto the same chip as the LVDS interface. Without DC balance, a long cable can result in ISI for a single-bit transition and cause a bit error. This happens because a single-bit transition, after a long string of no transitions, may not contain the energy necessary to change the stored charge through the entire cable. The term *disparity* describes the stored charge on the cable. If the disparity magnitude is large, then the single-bit transition cannot overcome the intersymbol interference at the end of the cable.

The OpenLDI part provides DC balance on a frame-by-frame basis. During the frame, the transmitter monitors the input signal for transitions. If no transitions occur, the transmitter inverts the next frame to maintain balanced cable charge, thus keeping the disparity between plus 10 and minus 9. The seventh LVDS data bit indicates whether the data in the payload is true or inverted.

This simple DC balance scheme keeps the signal eye diagram wide open at the receiver end. In addition, it provides enough DC balance to satisfy fiber-optical interconnect requirements, allowing the OpenLDI chipset to interface with standard parallel fiber-optical products.

Another integrated enhancement to the OpenLDI chipset is the transmitter pre-emphasis feature. Without pre-emphasis, the signal coming out of a cable loses the sharp transition edges due to the cable's high-frequency filter effect. With pre-emphasis, the driver accentuates the transitions to compensate for the filter effect at the end of the cable.

The pre-emphasis feature is user-selectable. When pre-emphasis is selected, the transmitter has two current drive levels. It delivers additional dynamic current during transitions to overcome the cable's filtering and supplies a lower drive current after the transition. It opens the signal eye diagram by overcoming cable distortion of the signal.

LVDS is now spawning follow-on technologies that expand its applications. The first follow-on is Bus LVDS, which allows the low-voltage differential signals to work in bidirectional and multidrop configurations. Another LVDS derivative, ground-referenced LVDS (GLVDS), is progressing through the standardization process. GLVDS moves the differential signal's common-mode voltage close to ground, which allows chips operating from very low supply voltages to communicate over a high-speed standard interface.

Self-Test

1. Even though data is digital, designers are choosing analog LVDS to drive transmission lines.

    a. true

    b. false

2. Moving information between systems is the main use for LVDS solutions today.

    a. true

    b. false

3. An LVDS signal is immune to common-mode noise.

    a. true

    b. false

4. Which of the following does not accurately describe LVDS?

    a. high-speed data throughput

    b. high cost

    c. higher integration

    d. power-miser operation

5. LVDS has _____ power requirements compared to PECL and GTL.

    a. lower

    b. higher

6. The input differential signal amplitude is undisturbed when noise appears _____.

    a. more at the minus input

    b. more at the plus input

    c. commonly to both inputs

7. LVDS technology has better EMI performance than all other interface technologies.

    a. true

    b. false

8. Even with LVDS, it is not possible to integrate multiple channels per chip.

    a. true

    b. false

9. The single-bit transition cannot overcome the intersymbol interference at the end of the cable when _____.

    a. the disparity magnitude is small

    b. the disparity magnitude is large

10. The _____ LVDS data bit indicates whether the data in the payload is true or inverted.

    a. fifth

    b. sixth

    c. seventh

    d. eighth

Correct Answers

1. Even though data is digital, designers are choosing analog LVDS to drive transmission lines.

    a. true

    b. false

    See Topic 1.

2. Moving information between systems is the main use for LVDS solutions today.

    a. true

    b. false

    See Topic 1.

3. An LVDS signal is immune to common-mode noise.

    a. true

    b. false

    See Topic 3.

4. Which of the following does not accurately describe LVDS?

    a. high-speed data throughput

    b. high cost

    c. higher integration

    d. power-miser operation

    See Topic 4.

5. LVDS has _____ power requirements compared to PECL and GTL.

    a. lower

    b. higher

    See Topic 5.

6. The input differential signal amplitude is undisturbed when noise appears _____.

    a. more at the minus input

    b. more at the plus input

    c. commonly to both inputs

    See Topic 6.

7. LVDS technology has better EMI performance than all other interface technologies.

    a. true

    b. false

    See Topic 6.

8. Even with LVDS, it is not possible to integrate multiple channels per chip.

    a. true

    b. false

    See Topic 8.

9. The single-bit transition cannot overcome the intersymbol interference at the end of the cable when _____.

    a. the disparity magnitude is small

    b. the disparity magnitude is large

    See Topic 9.

10. The _____ LVDS data bit indicates whether the data in the payload is true or inverted.

    a. fifth

    b. sixth

    c. seventh

    d. eighth

    See Topic 9.

Glossary

ANSI
American National Standards Institute

ATM
asynchronous transfer mode

CMOS
complementary metal oxide semiconductor

DC
direct current

EIA
Electronic Industries Alliance

EMI
electromagnetic interference

FPD
flat panel display

GLVDS
ground-referenced LVDS

GTL
gunning transceiver logic

HDTV
high-definition television

IEEE
Institute of Electrical and Electronic Engineers

ISI
intersymbol interference

LVDS
low-voltage differential signaling

LVTTL
low-voltage transistor-transistor logic

OpenLDI
open LVDS display interface

PCB
printed circuit board

PECL
pseudo emitter coupled logic

RGB
red/green/blue

SSTL
stub series terminated logic

TIA
Telecommunications Industry Association