Design Considerations for Gigabit Backplane Systems

Definition

Engineers continually access new technologies when making architectural decisions for their new products. The consumer demand for more system bandwidth is common, as is the need to balance high system speed with the reality of establishing cost/performance/risk tradeoffs for electronic equipment. The designer may have constraints that dictate certain design parameters; others remain open for selection. In the design of a backplane interconnect system, a myriad of options is available for printed circuit (PC) board materials, trace topologies, and connectors. Launches from the connector to the board and trace lengths must also be considered to reach system performance goals as designers optimize the system. Part of this optimization includes achieving the electrical integrity necessary to pass such signals while maintaining mechanical attributes and cost tradeoffs.

Overview

This tutorial explores high-speed backplane-interconnect system tradeoffs related to the effects on increases in bandwidth on the signal path from driver to receiver through printed circuit boards (PCBs).

Topics

Glossary

1. Introduction

System attributes evaluated in this study include line length, trace width, trace topologies (single-ended, broadside differential, and edge-coupled differential), material losses (for FR–4 and more exotic, lower-loss materials), conductor losses, plated-through hole (PTH) launches, routing considerations, and board-to-board interconnects. The effects of the aforementioned components or subsystems for backplane systems are quantified to present possibilities for a viable system based on fast data rates. 2.5 Gbps was chosen as the data rate for sample system comparison. These trends would also be useful in understanding design parameters for other data rates.

Analysis of individual components will verify the 2.5–Gbps data stream in order to create a complete system. Once the test system is analyzed, correlation between the system measurements and a mathematical combination of individual components will use all data for additional system descriptions. Time and frequency domain analyses are in the form of reflection data (time domain reflection [TDR], S11) and transmitted data (time domain transmission [TDT], S21, eye pattern). Test equipment includes a 3–Gbps HP (70841B) pulse pattern generator, a Tektronix 11801B TDR, and an HP 8722D 40 GHz vector network analyzer (VNA).

As signal speeds increase, system performance is limited by long lengths, impedance mismatches, and various noise in the system. Long lengths relate to material losses, conductive losses, and greater distances for noise interjection. Because the system is more sensitive to these factors, engineers implement different techniques designed to combat the aforementioned nuisances. Different material laminates may alleviate dielectric losses and dispersive effects. From a table of different high-performance laminates, nine laminates were chosen for board studies and highlighted in *Table 1*.

Table 1. High-Performance Printed Wire Board (PWB) Materials

Material	Type	Availability	Er	Df	Tg (degrees C)
Nelco	N4000–13	all types	3.95 @ 10 Ghz	0.01 @ 1 Ghz	210
	N6000	all types	3.3 @ 1 Ghz	0.005 @ 1 Ghz	210
Arlon	25N	0.006” increm.	3.25 @ 10 Ghz	0.0024 @ 10 GHz	> 225
Megtron	R57 15	all types	3.5–4.2 @ 1 Mhz	0.010-0.015 @ 1 MHz	180

Allied Signal	FR 408	all types	< 3.6 50 Mhz–1 Ghz	< 0.009 50 Mhz–1 Ghz	180
Gore	Speedboard C	prepreg only	2.2.–2.6 @ 1 Mhz	0.003 @ 1 Mhz	190
Rogers	4000 series	0.0033” increm. core	3.38 @ 10 Ghz	0.004 @ 10 Ghz	> 280
		0.0040” increm. fill			
Polyclad	PCL–LD–621	all types	3.5 @ 1 Ghz	0.006 @ 10 Ghz	190
GIL	GML 1000	0.020”, 0.030”, 0.060”	3.05 @ 10 Ghz	0.003 @ 10 Ghz	135
	MC 5	cores/prepregs	3.26 1–15 Ghz	0.0015 @ 10 Ghz	145
G.E.	GETEK	all types	3.6–4.2 @ 1 Mhz	0.010–.015 @ 1 Mhz	175–185
ISOLA	GIGAVER	all types	3.5–4.0 @ 1 Mhz	0.003 @ 1 Mhz	210
Taconic	RF 35	0.0035” increm.	3.5 @ 2 Ghz	0.0018 @ 2 Ghz	315
		cores only			

To combat noise interjection, device manufacturers are implementing differential pairs.

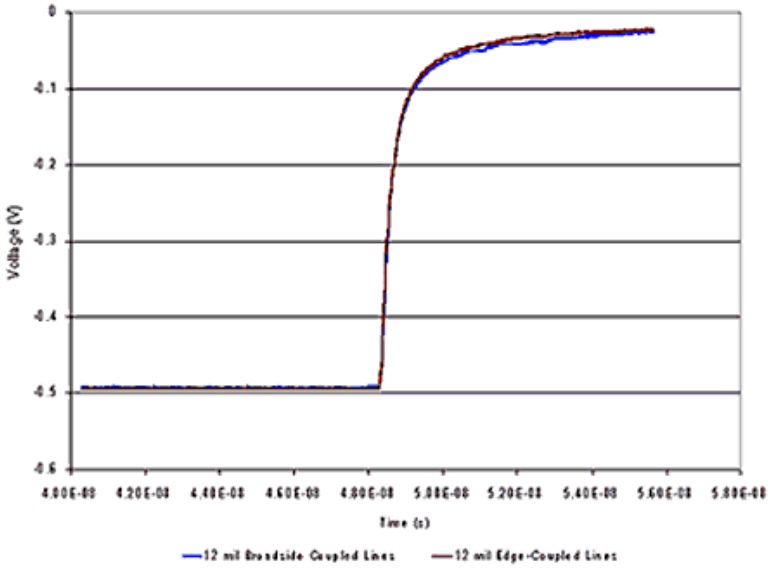
2. Broadside versus Edge-Coupled Differential Pairs

Preliminary findings derived from simulation and precursory measurements and presented at DesignCon 1999 in Signal Integrity Characterization of Printed Circuit Board Parameters proved to be false after a more detailed study.[1] Original results indicated a considerable improvement in broadside-coupled over edge-coupled lines, even in as narrow as 8-mil lines. New test boards and additional TDT and VNA measurements, however, show that there is no marked improvement between the two topologies. In the TDT plot shown in *Figure 1*, both cases have the same linewidth, spacings, and dielectric thicknesses to yield

[1] Patel, Gautam and Katie Rothstein. "Signal Integrity Characterization of Printed Circuit Board Parameters." 1999 High-Performance System Design Conference, DesignCon 1999, page 1.

100-Ohm nominal impedance. *Figure 1* merely demonstrates the insufficient difference between the two topologies. Comparable transmitted data plots in both different materials and different line widths show similar results.

Figure 1. Comparison of Broadside versus Edge-Coupled TDT for FR–4, 8-mil, 100-Ohm, 1-m Traces



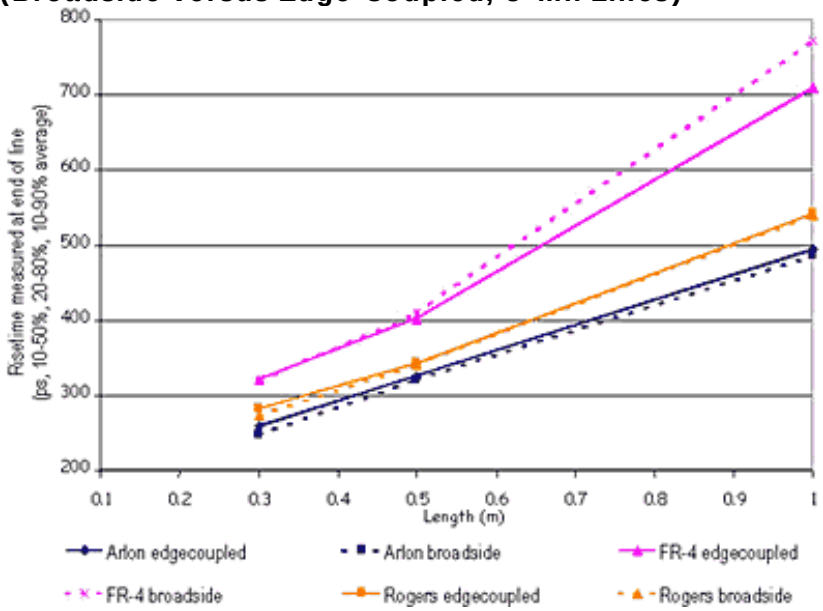
Layering multiple waveforms yields graphs that are difficult to read. Instead of plotting transmitted data against the time axis, the rise times of the transmitted pulses are plotted as individual data points. Risetime specifications of 10 to 50 percent, 20 to 80 percent, and 10 to 90 percent each seem to favor or ignore certain aspects of the losses. Ten- to fifty-percent risetimes are a better indicator of conductive losses, as the dispersive losses from the material are more readily seen in the top portion of the risetime waveform. Similarly, 10- to 90-percent waveforms are a better indicator of dispersive losses, which, on a TDT measurement, mask conductive losses. Risetimes specified from 20 to 80 percent tend to neglect some reflection seen on the transmitted pulse. For this reason, the three risetime results were averaged for each data point. The risetime data can then be plotted against other factors, such as trace length or trace width.

The output of the TDR's transmitted pulse at the test board was approximately a 35-ps edge (10- to 90-percent risetime). By plotting a very lossy (FR–4), a less lossy (Rogers 4000 series), and a low-lossy (Arlon 25N) material for both broadside-coupled and edge-coupled differential lines against trace length, a comparison between the two topologies can be made.

As expected, more lossy materials show lower performance from broadside lines than do less lossy materials. For example, FR–4 in the broadside configuration shows more loss than does the edge-coupled configuration seen in *Figure 2*. For Arlon, the broadside lines experience slightly less loss than do the edge-coupled.

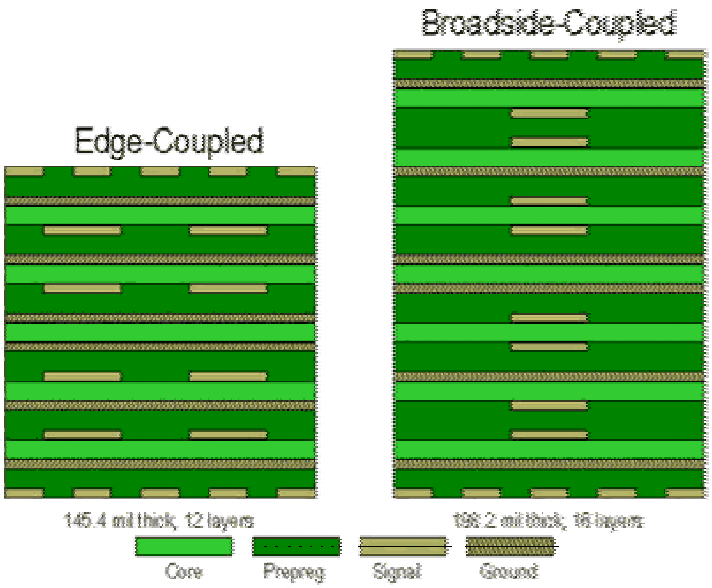
The Rogers material shows equal losses for broadside-coupled and edge-coupled lines. In all cases, the difference was not significant in the usable line width range.

Figure 2. Comparison of Different Materials at Different Lengths (Broadside versus Edge-Coupled, 8-mil Lines)



In some instances, broadside lines may have some routing advantages over edge-coupled lines. For the most part, however, broadside lines may become a manufacturing and electrical bane. To prove this point, two mock layups with four signal layers were constructed (see *Figure 3*).

Figure 3. Mock Layup for Differential Comparison



This translated into eight routing layers for broadside-coupled lines. The layups were based on common backplane linewidths and dielectrics and yielded the following results:

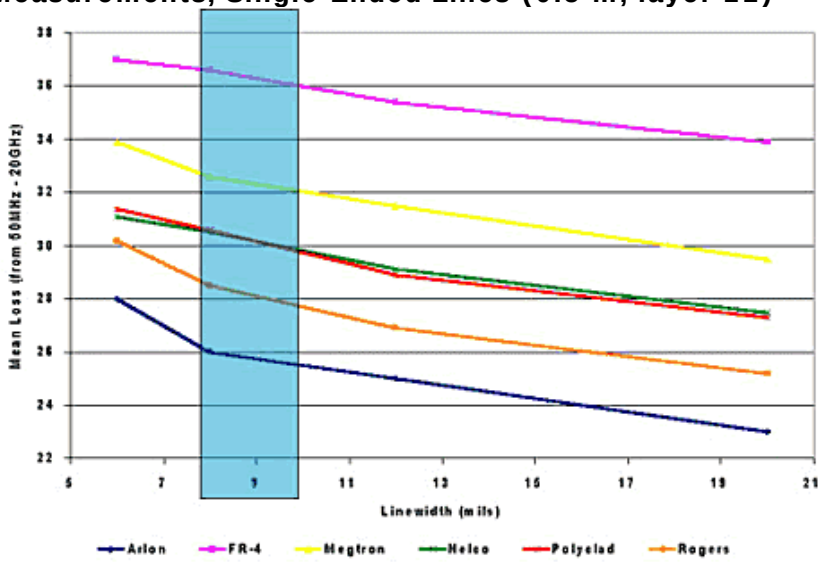
- A typical layup for 8-mil lines (12 mil fills both cases) will increase in thickness and therefore aspect ratio by 27 percent.
- Both factors translate into increased cost and decreased manufacturability.
- As more signal layers are added, the effects are compounded.

In addition to manufacturability implications, this increase in board thickness with broadside-coupled lines increases the capacitance of the PTH and increases the length of the stub, both of which have negative electrical effects.

3. Point of Diminishing Returns: Line Width Increases

Material losses amalgamate with copper losses, giving the designer several choices in distributing losses throughout the system. For cost motives, changes in dielectric materials may be one of the last changes made to the system. Line widths are often one of the first changes to be made. Intuitively, 20-mil lines give less conductive loss than 6-mil lines. What is the quantitative difference, however, between different line widths? Using single-ended lines and VNA through measurements (S21), different materials were analyzed over a spectrum of four different line widths (6, 8, 12, and 20 mil). As different materials experience peaks and notches at different frequencies, and some materials were more broadband than others, a mean loss value was found for each test case by sweeping from 50 MHz to 20 GHz (see *Figure 4*).

Figure 4. Comparison of Mean Loss Values for S21 Measurements, Single-Ended Lines (0.5 m, layer 11)



This type of result gives a more easily analyzable result than overlaid test cases. Actual waveforms are included in the Appendix.

Moving from a 6-mil to an 8-mil line yields 1.3-dB improvement, which is 4.4 percent. Likewise, going from an 8-mil line to a 12-mil trace width yields 1.3-dB improvement, or 4.4 percent. Because 8-mil lines seem to be about at the point of diminishing returns from an electrical, manufacturable, and routable standpoint, 8- and 10-mil lines were selected for system simulations. A 6-mil to a 20-mil increase in line width yields an average of 4.2-dB improvement over all materials (14 percent). This is roughly the same improvement (as averaged over line width) seen by moving from FR–4 to Megtron material (3.95 dB or 13.2 percent). So, at some point in time, a slight change in material may yield more significant results than major changes in line widths. The article entitled “On the Dielectric Material Properties for Thin Film Integrated RF and Microwave Applications” points out that, at high frequencies, broad line widths may contribute to additional parasitic effects such as radiation and capacitive coupling.[2]

Some criticism for not impedance-matching all test cases materialized with the above S21 graph (see *figure 4*). The number of test boards was limited to control cost and lead-time. In addition, keeping the boards at a reasonable thickness limited the number of layers per board. One line width was chosen to be impedance-matched for each trace topology. The 8-mil differential lines were matched to 100 Ohms, and the 12-mil, single-ended lines were matched to 50

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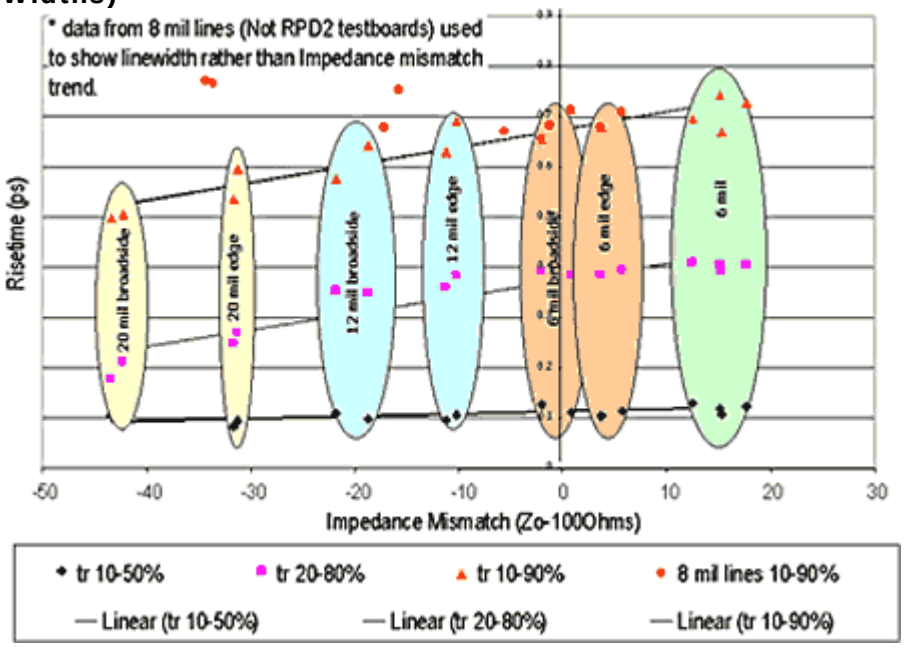
[2] Pieters, P., S. Brebels, G. Carchon, K. Vaesen, W. DeRaedt, E. Beyne, and R.P. Mertens. "On the Dielectric Material Properties for Thin Film Integrated RF and Microwave Applications." *Advancing Microelectronics*, volume 26, number 5, page 22.

Ohms. To achieve all the desired measurements, multiple line widths needed to reside on the same layer, causing impedance mismatches in many of the line widths.

Additional data was analyzed to ascertain the impedance mismatch's effect on measured loss. The analysis plotted risetime degradation against impedance mismatch. The impedance mismatch was calculated by subtracting 100-Ohms (all are differential cases) from the measured impedance of the line. Theoretically, if the impedance mismatch outweighed the line width effect on the TDT's risetime, the trend lines would form a *V* around the "0" impedance mismatch point. The trend lines clearly increase in risetime with respect to line width increases—not impedance mismatch. To prove this point further, 8-mil lines with varying degrees of impedance mismatch were plotted on the same graph. The risetime (10 to 90 percent) for all of these 8-mil lines remains approximately the same (see *Figure 5*).

Figure 5. Risetime Plotted against Impedance Mismatch (for FR–4; all layers; 0.5-m differential; 6-, 8-, 12-, 20-mil Line Widths)



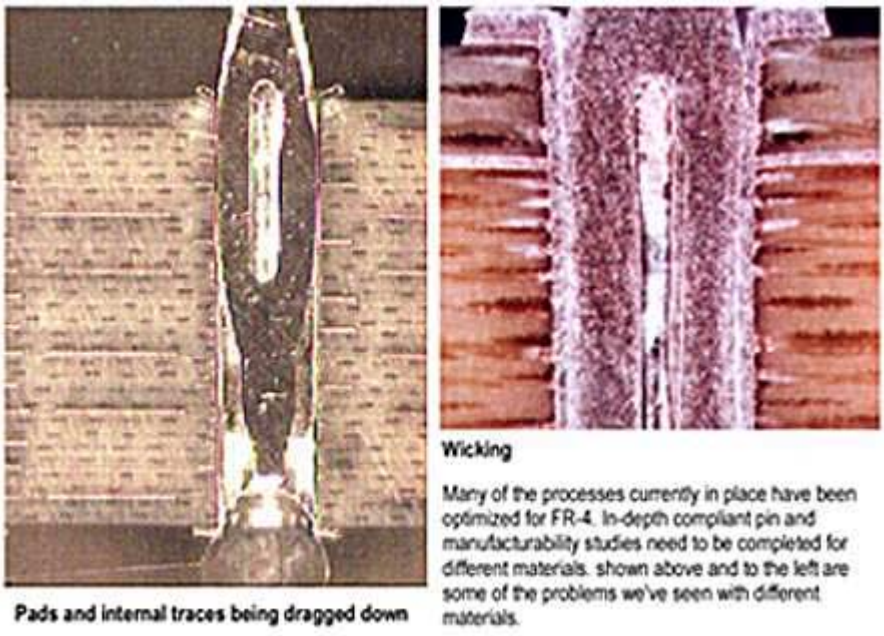
Based on the impedance mismatch data, the demonstrated improvements on the S21 graph shown in *Figure 5* are due primarily to material parameters. Moving from FR–4 to a Nelco 6000/Polyclad LD621 material represents a 20.5-percent improvement. Moving from FR–4 to Rogers 4000 series is a 26.8-percent improvement, and going from FR–4 to Arlon is a 34.1-percent improvement. Although electrical improvement makes obvious decisions for material selection, cost, manufacturability, and mechanical properties of the material enter into a decision matrix for material selection.

4. Mechanical Materials Properties

The PWB fabrication experiments will include a process parameter study of drilling, adhesion, stability, and press guidelines. Additionally, sheet size, core/prepreg, and thickness availability will affect the system usability, as these may limit the application of the performance laminates.

At the final system level, compatibility with connector and device termination must be considered. For daughtercards and active motherboards, the PCBs will be subjected to reflow temperatures. A reliability study must be completed on the new laminates. Hybrid boards where new materials will be mixed with FR–4 layers will need to be checked for delamination and barrel cracking due to the difference in temperature coefficients of expansion (TCEs). Currently, the predominant backplane connector is a press-fit compliant pin termination, as a result of difficulty in uniformly soldering the large thermal mass of today's backplanes and the proven reliability of this interface. Additionally, it is preferred because of the ability to repair a single damaged pin on a large, populated board. Experiments show that, due to the differences in adhesion and laminate modulus, the compliant pin/board interface must be altered from the FR–4 recipe for some advanced laminates (see *Figure 6*). A full test sequence has been developed to ensure the long-term reliability of the gastight pin/barrel joint.

Figure 6. Future Work



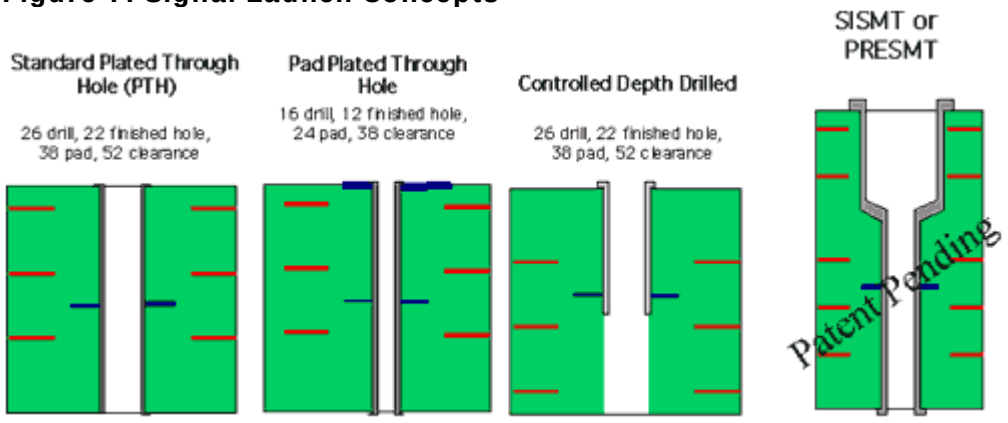
5. Launch Issues

After transmission through the PCB, launches were isolated as another effect on data transmission. In addition to stubbing effects, the parasitic parameters of the PTH cause electrical degradation. The goal was to optimize the inductance and capacitance of the PTH so that the launch behaved as an ideal transmission line. As backplane systems have large barrels and long PTHs as result of board thickness, lumped capacitance was used as a good first cut.

Capacitive launches act as a low-pass filter. The effect of this filter is to prohibit the transmission of high frequencies.

Using a different type of plated hole, such as micro-vias, can minimize many of these effects. Traditionally these have induced a cost penalty. Blind vias takes care of the electrical capacitance and stubbing problems; however, launching into the board onto any layer becomes a problem. To correct this, buried vias could be used to distribute the signal into deeper layers. Implementing blind and buried vias requires multiple lamination and processing steps yielding higher costs. Four different launches were explored for electrical gain (*Figure 7*).

Figure 7. Signal Launch Concepts



The standard PTH shown in the picture is a 0.022-inch finished hole. This is the specified hole size for Teradyne's press-fit VHDM family of connectors used in the system simulations and in the connector individual section of the report. The second type of PTH shown is a pad-type via. This type of hole would be used with a pressure-mount or a surface mount solder-attach-type of connector. The third PTH is a standard PTH that has been sent through drilling again, adding a secondary drilling operation after plating. This removes the unused portion of the via below the layer where the signals are routed out. The fourth type of hole is a semi-intrusive surface-mount technology (SISMT); a press-fit version of this hole (PRESMT) is also on the drawing board.

The standard PTH is a baseline measurement. The pad-type via shows electrical promise for reducing capacitance theoretically. The board thickness will determine the minimum drilled-through-via diameter due to plating aspect ratios. For example, a 0.250-inch board and a 12:1 aspect ratio yields a 0.021-inch drill and a 0.017-inch finished hole size. The pad itself has additional capacitance, so much of what is picked up in the smaller PTH is lost again on the pad. Based on the simple capacitance comparison, the only way to realize an electrical advantage from the padded system is to use it in conjunction with a blind and buried via or micro-via. Because of line widths needed in backplane systems and thick dielectric layers, the 1:1 or 1:2 aspect ratio needed for micro-vias is not always possible. As stated before, blind, buried, and micro-vias limit the depth to which signals can be launched into the board.

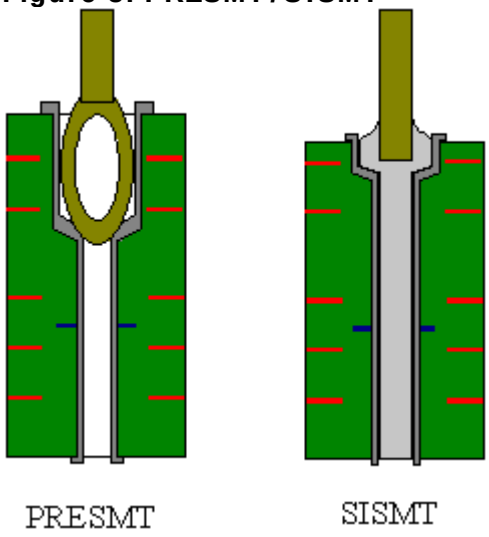
The counter-bored PTH has several advantages. Because part of the plating is drilled out, the capacitance and the stub are both reduced. Routing is not as efficient as micro or blind vias; the intent of this method, however, is to provide an electrically equivalent blind via at a lower cost. A press-fit-type connection requires approximately 100 mils of plated barrel length. On a very thick board, this type of launch could be used with press-fit pins. *Table 2* shows measured data for different amounts of plating removed from a standard VHDM 0.022-inch plated hole. From the data, it is apparent that this technique can drastically reduce the capacitance of the launch.

Table 2. Signal Launch Measured Capacitance, Standard VHDM Hole versus a Counter-Bored VHDM Hole (.250-inch-thick PCB with various secondary drill depths)

Test #	Measured Cap (pF) Standard Hole	Counter Bore Depth (mils)	Measured Cap w/CB (pF)
1	2.37	50	1.95
2	2.38	75	1.77
3	2.39	100	1.52
4	2.40	125	1.27
5	2.38	150	1.03

Finally, the SISMT/PRESMT–type of PTH allows routing to all layers and reduces capacitance but does not take care of stubbing effects. This graduated hole allows for smaller drills in the lower section of the hole, and if the top section is long enough, a press-fit-type connection can be used (PRESMT in *Figure 8*). Otherwise a stubby pin solder termination to the large diameter barrel can be used (SISMT in *Figure 8*).

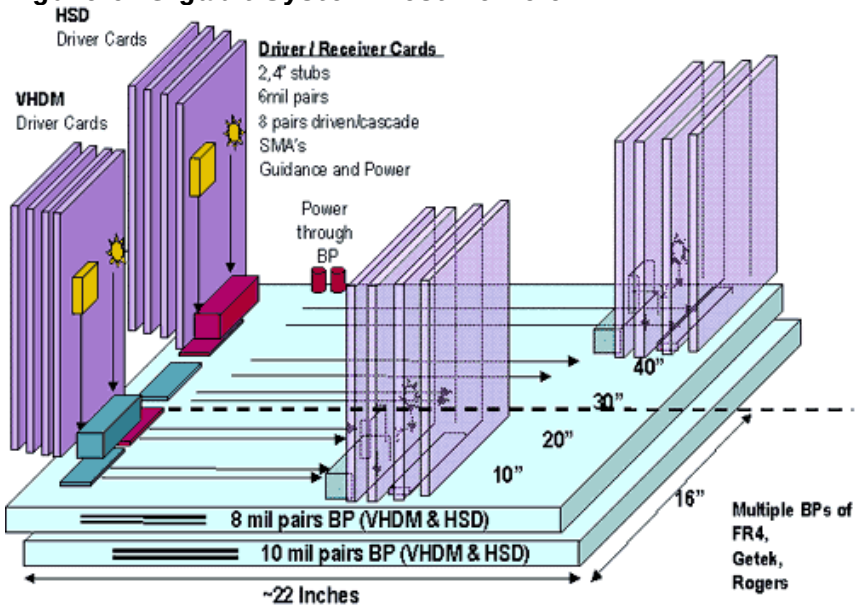
Figure 8. PRESMT/SISMT



6. System Measurements

Evaluating individual components of a backplane system is helpful in determining whether or not the components being measured meet a particular performance criterion. However, when the individual components are integrated, the overall performance may behave differently than the sum of the individual components. Measurements are needed to confirm a correlation. If a correlation is established, extrapolation of specific system components can be achieved. The backplane/daughtercard connector, PTH, and board laminate will be analyzed in an integrated fashion. A schematic of the test vehicle is shown in *Figure 9*.

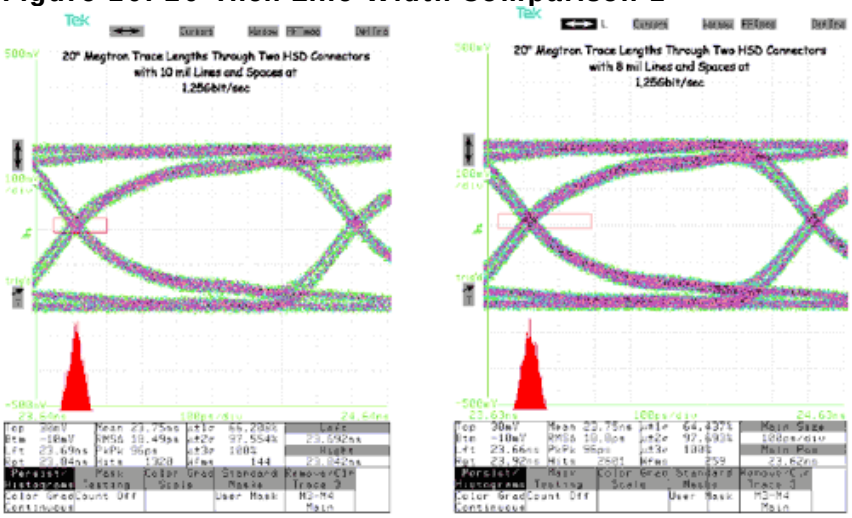
Figure 9. Gigabit System Test Vehicle



The goal of the analysis was to vary the individual components to determine the overall system performance. Board materials used in the system were Rogers 4000 series, Megtron (a Getek equivalent), and FR–4. Trace geometries were 8- and 10-mil line widths with lengths of 10, 20, 30, and 40 inches. The overall thicknesses of the backplanes were 0.250 of an inch. All the backplane and daughtercard traces have nominal 100-Ohm differential impedance. The daughtercards used to launch and receive the signals were 0.125-inch thick with 5-mil line widths/spaces and 2-inch/4-inch stubs. The measurements were taken at 1.25 Gbps, 2.5 Gbps, and 3.3 Gbps. Eye patterns were used as the measure of merit, and a pseudo-random bit pattern was used in the eye-pattern measurements.

The results show that at very long line lengths and fast data rates, there is very little improvement in going from an 8-mil line width to a 10-mil line width (see *Figures 10* to *12*).

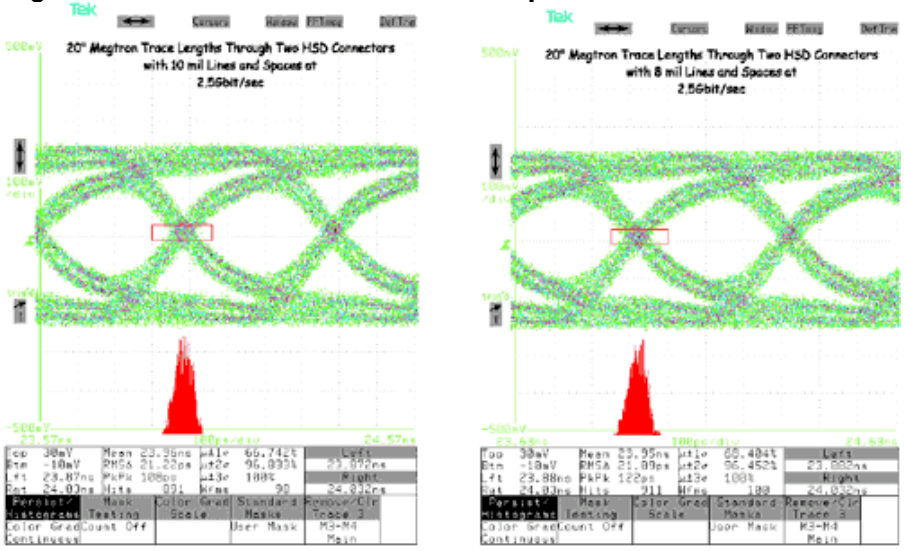
Figure 10. 20-Inch Line Width Comparison 1



Left: 20” Megtron trace lengths through two HSD connectors with 10-mil lines and spaces at 1.25 Gbps

Right: 20” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 1.25 Gbps

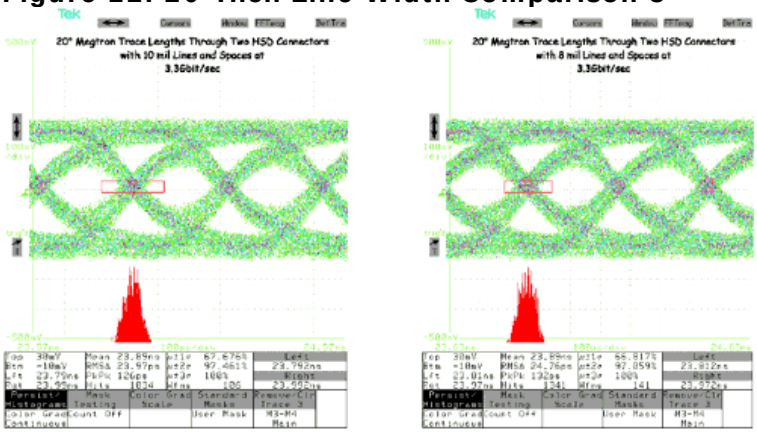
Figure 11. 20-Inch Line Width Comparison 2



Left: 20" Megtron trace lengths through two HSD connectors with 10-mil lines and spaces at 2.5 Gbps

Right: 20" Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 2.5 Gbps

Figure 12. 20-Inch Line Width Comparison 3

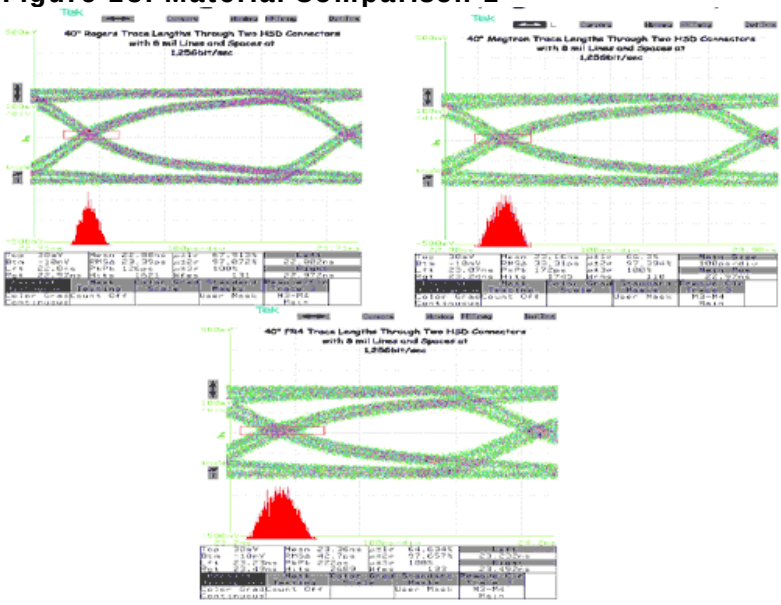


Left: 20" Megtron trace lengths through two HSD connectors with 10-mil lines and spaces at 3.3 Gbps

Right: 20" Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps

For a 40-inch track width at 2.5 Gbps in Megtron/Getek using 10-mil lines, the eye-opening was ~225 ps and the amplitude was ~90 mV. The same test done with an 8-mil line width shows an eye-opening of ~225 ps with an amplitude of ~90 mV. For 40-inch track lengths, the Rogers material shows an improvement over the FR–4 and Megtron materials (see *Figures 13* to *15*).

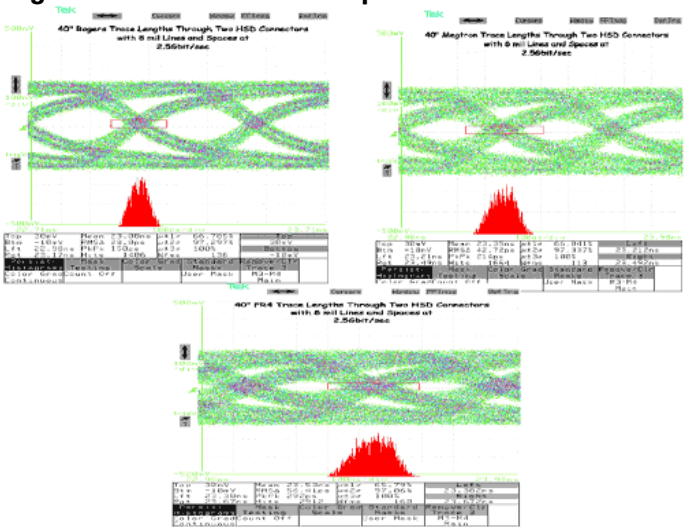
Figure 13. Material Comparison 1



Left: 40” Rogers trace lengths through two HSD connectors with 8-mil lines and spaces at 1.25 Gbps

Right: 40” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 1.25 Gbps

Figure 14. Material Comparison 2

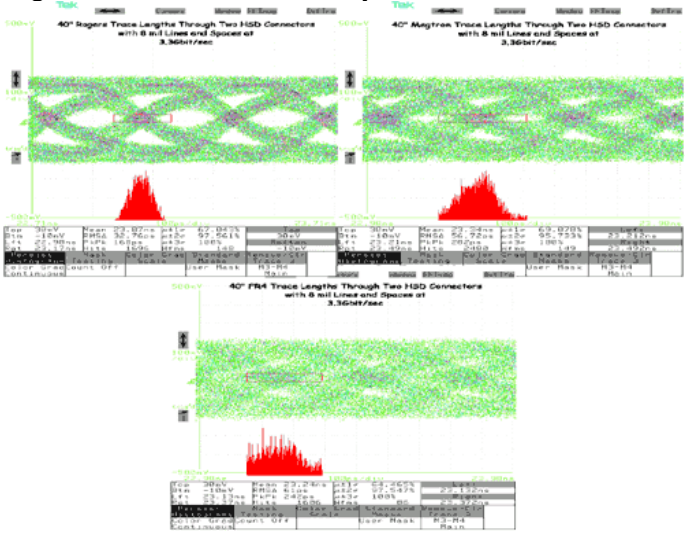


Left: 40” Rogers trace lengths through two HSD connectors with 8-mil lines and spaces at 2.5 Gbps

Right: 40” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 2.5 Gbps

Bottom: 40” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 2.5 Gbps

Figure 15. Material Comparison 3



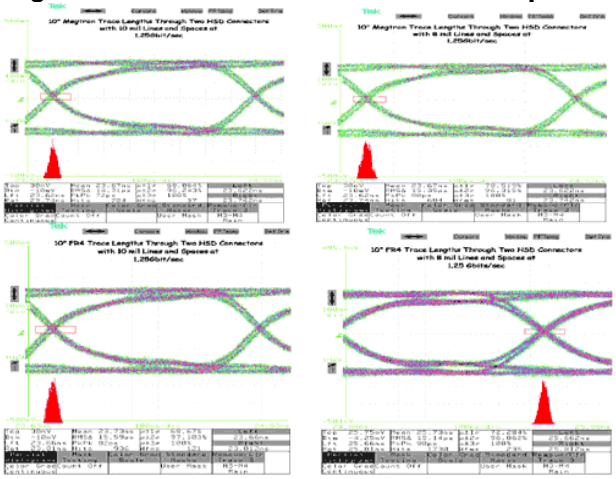
Left: 40” Rogers trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps

Right: 40” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps

Bottom: 40” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps

With a 40-inch track length and 8-mil line widths, the eye-opening in FR–4 at 2.5 Gbps was ~175 ps/50 mV. Using the same test scenario but changing the material to Megtron the eye opens up to ~225 ps/90 mV. Again, the same test was performed using the Rogers material and the eye-opening was ~300 ps/160 mV. The material performance is more evident at 3.3 Gbps with the eye-opening for FR–4 essentially closed, Megtron at ~100 ps/30 mV and Rogers ~175 ps/90 mV. At 1.25 Gbps with 40-inch track lengths, the three different materials perform essentially the same, thereby verifying that the dielectric loss plays a large role at the very fast data rates (high frequencies), but conductor loss will dominate at the lower frequencies. For shorter backplane track lengths such as 10-inch, line widths and dielectric loss still have a measurable effect in the signal performance. For a 10-inch track length in FR–4, 8-mil line widths, and 3.3 Gbps data rate, the eye opening is ~200 ps/110 mV. The same scenario with 10-mil line widths yields an eye opening of ~225 ps/170 mV. At 2.5 Gbps, 10-inch track length, 8-mil line width, in FR–4 yields an eye opening of ~320 ps/220 mV. With the same data rate, track length, and material and 10-mil line width, the eye opened up to ~350 ps/250 mV. In a Megtron backplane with 10-inch track length, 3.3 Gbps, and 8-mil lines, the eye opening was ~240 ps/180 V. Repeating the test with 10-mil line widths yields an eye opening of ~230 ps/190 mV. When the data rate was slowed to 2.5 Gbps, the eye opening with Megtron for the 8-mil line width was ~340 ps/250 mV, and with a 10-mil line width the eye opening was ~340 ps/260 mV. This shows that increasing the line width from 8 mil to 10 mil yields a slight improvement in performance but may not offset the penalty of increased board thickness to maintain the impedance (see *Figures 16* to *18*).

Figure 16. 10-Inch Line Width Comparison 1



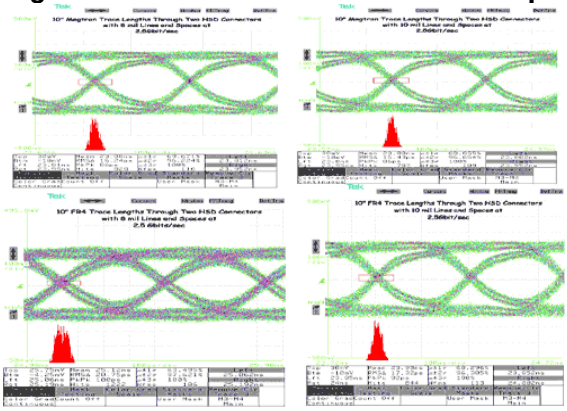
Top Left: 10” Megtron trace lengths through two HSD connectors with 10-mil lines and spaces at 1.25 Gbps

Top Right: 10” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 1.25 Gbps

Bottom Left: 10” FR–4 trace lengths through two HSD connectors with 10-mil lines and spaces at 1.25 Gbps

Bottom Right: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 1.25 Gbps

Figure 17. 10-Inch Line Width Comparison 2



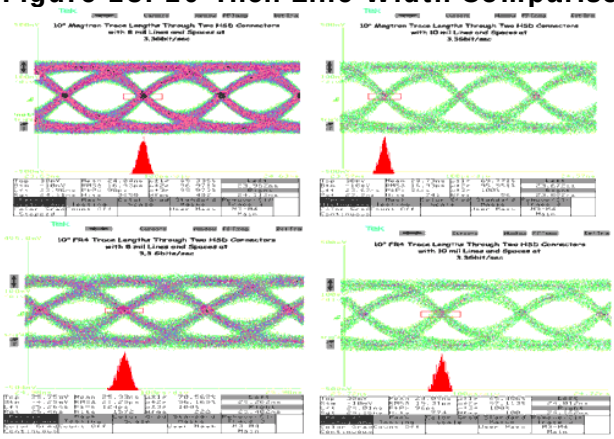
Top Left: 10” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 2.5 Gbps

Top Right: 10” Megtron trace lengths through two HSD connectors with 10-mil lines and spaces at 2.5 Gbps

Bottom Left: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 2.5 Gbps

Bottom Right: 10” FR–4 trace lengths through two HSD connectors with 10-mil lines and spaces at 2.5 Gbps

Figure 18. 10-Inch Line Width Comparison 3



Top Left: 10” Megtron trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps

Top Right: 10” Megtron trace lengths through two HSD connectors with 10-mil lines and spaces at 3.3 Gbps

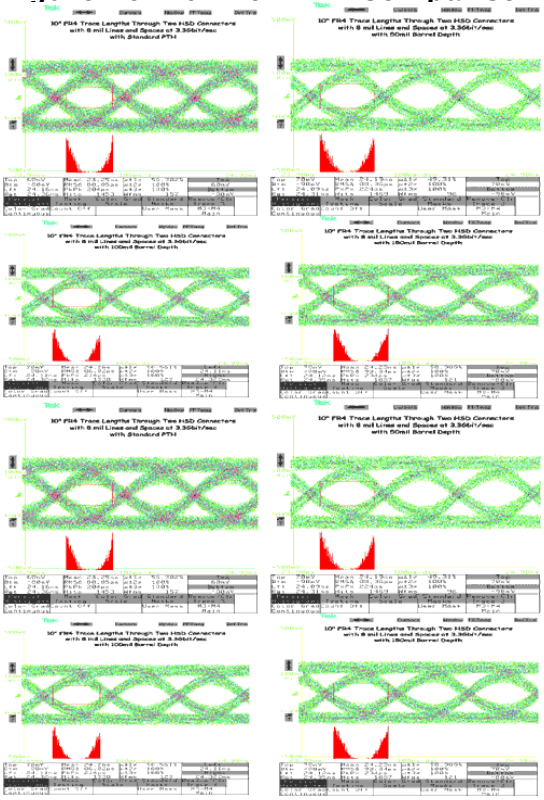
Bottom Left: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps

Bottom Right: 10” FR–4 trace lengths through two HSD connectors with 10-mil lines and spaces at 3.3 Gbps

A test was devised to evaluate the system effects of varying the launch capacitance. For conventional backplane connectors, a PTH launch is used and can give capacitance values up to 3 pF, depending on the thickness of the backplane. An experiment was done where a 10- and 20-inch backplane was

measured with a PTH capacitance of 2.5 pF. To see the effect of the launch capacitance on the system eye-pattern, the launches were counter-bored to leave barrel depths of 50 mils, 100 mils, and 150 mils. The eye patterns were compared at 3.3 Gbps over track lengths of 10 and 20 inches. For the 10-inch track lengths, the trace capacitance with a standard PTH was measured to be 39 pF. The measured trace capacitance with a 50-mil PTH was 36.7 pF; 100-mil PTH was 38.2 pF, and 150-mil PTH was 38.7 pF. The resulting eye patterns shown in *Figure 19* show that there is very little improvement in the eye opening, even with a 10 percent reduction in the overall trace capacitance.

Figure 19. 10-Inch PTH Comparison



Top Left: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with standard PTH

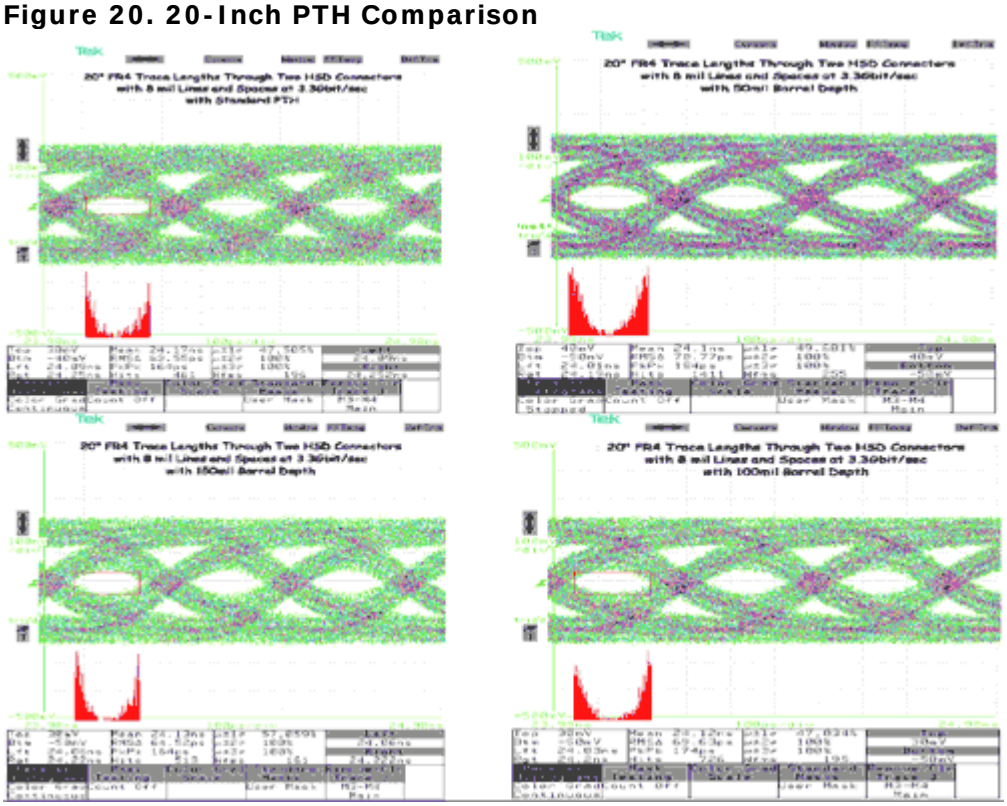
Top Right: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with 50-mil barrel depth

Bottom Left: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with 100-mil barrel depth

Bottom Right: 10” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with 150-mil barrel depth

Intuitively, it is expected that a reduced launch capacitance will be more effective for the shorter track lengths than the longer track lengths. *Figure 20* shows the resulting eye pattern at 3.3 Gbps in FR–4 over a 20-inch track and various PTH barrel depths. It is clear from the plots that there is very little improvement from the standard PTH barrel to one that was reduced to only a 50-mil PTH barrel.

Figure 20. 20-Inch PTH Comparison



Top Left: 20” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with standard PTH

Top Right: 20” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with 50-mil barrel depth

Bottom Left: 20” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with 150-mil barrel depth

Bottom Right: 20” FR–4 trace lengths through two HSD connectors with 8-mil lines and spaces at 3.3 Gbps with 100-mil barrel depth

7. Conclusion

Ongoing work will substitute device daughtercards into the system test vehicle. The aforementioned work with the processing constraints involved with building and loading backplanes made from high-performance materials is also ongoing. A more detailed study must be done on what technology will be needed to increase data rates up to 10-Gbps data streams over a conventional copper backplane system.

8. Appendix

Figures 21 and 22

Figure 21. S21 of 0.5-m Single-Ended Lines, 8 mil

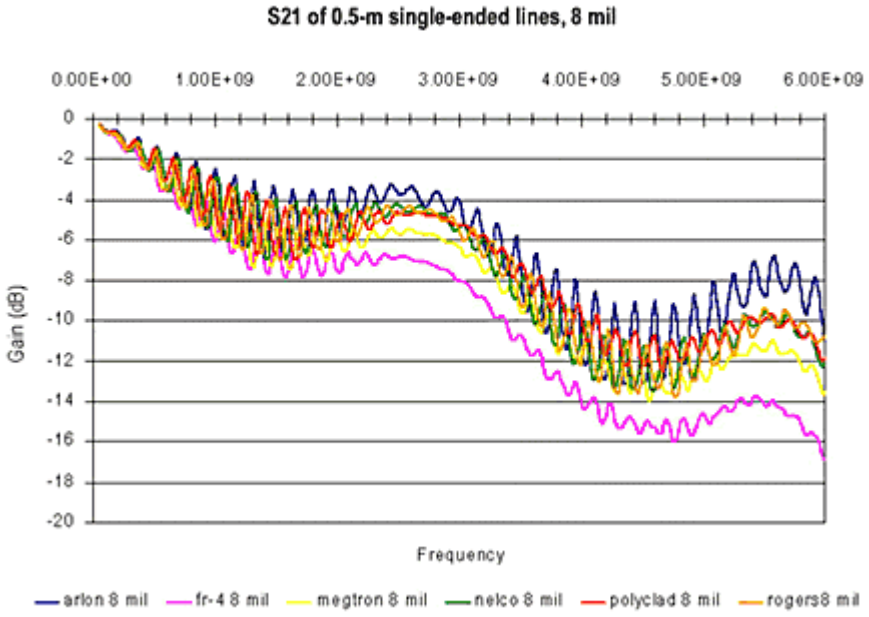
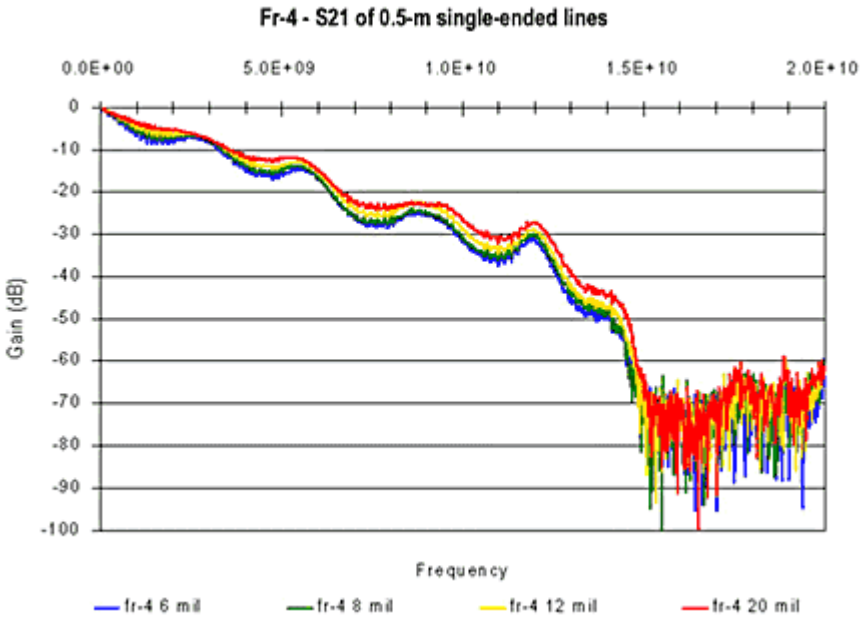
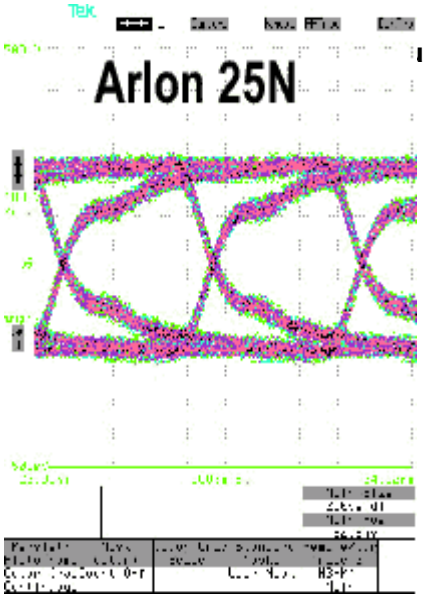


Figure 22. FR–4—S21 of 0.5-m Single-Ended Lines



Figures 23-28: Comparison of Eye Patterns for Different Materials (8-mil lines, edge-coupled, 1 m, 1.25 Gbps)

At slower speeds, the virtues of a less lossy material are not fully realized. Measurements are approximate.



ıde=66.7% Open

Figure 24. Rogers 4000 Series
Time=93.7% Open; Amplitude=63.3% Open

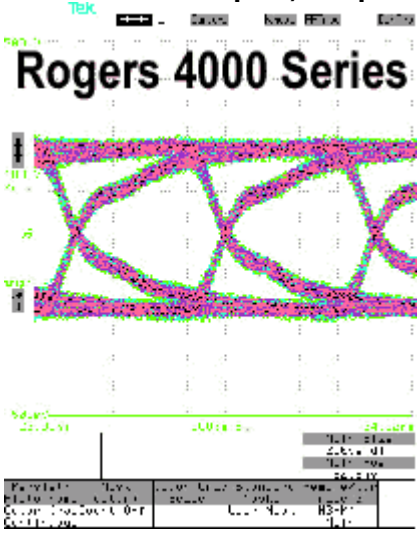


Figure 25. Polyclad LD621
Time=93.7% Open; Amplitude=66.7% Open

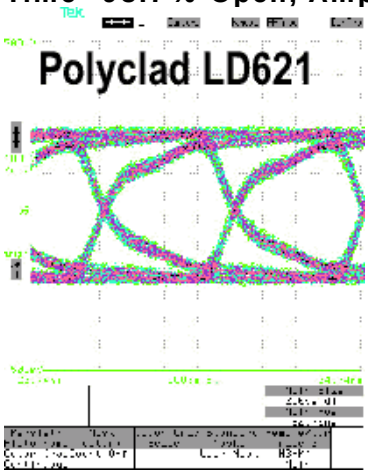


Figure 26. Nelco 6000 Series
Time=93.7% Open; Amplitude=66.7% Open

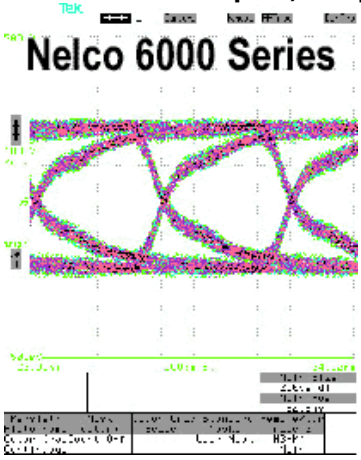


Figure 27. Megtron
Time=91.7% Open; Amplitude=60% Open

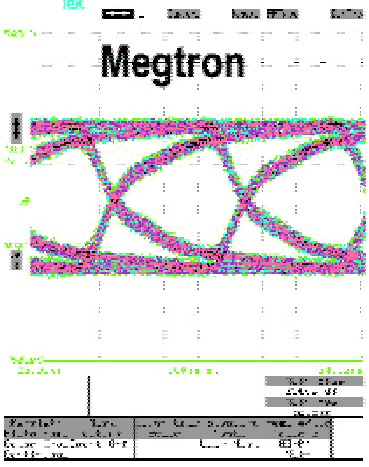
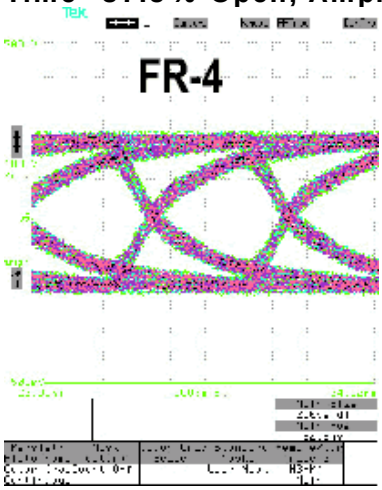
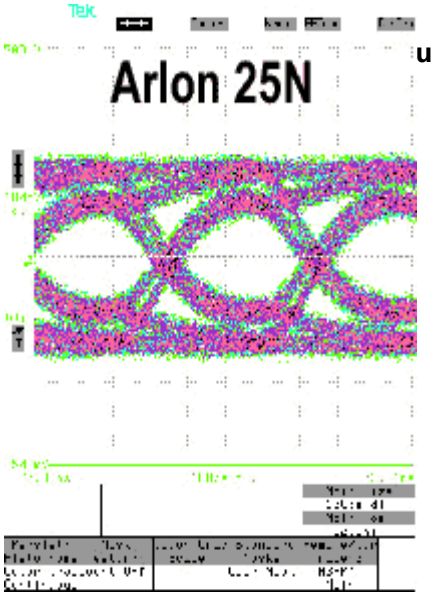


Figure 28. FR–4
Time=87.5% Open; Amplitude=53.3% Open



Figures 29-34: Comparison of Eye Patterns for Different Materials (8-mil lines, edge-coupled, 1 m, 2.5 Gbps)

At higher speeds, the need for a less lossy material becomes more apparent. Measurements are approximate.



ude=36.6% Open

Figure 30. Rogers 4000 Series
Time=72.9% Open; Amplitude=30% Open

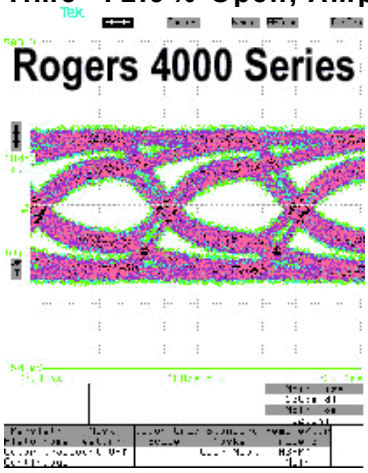


Figure 31. Polyclad LD621
Time=70.8% Open; Amplitude=33.3% Open

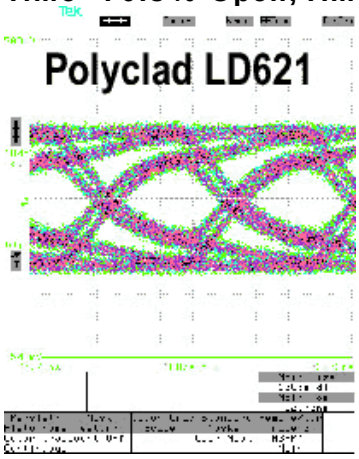


Figure 32. Nelco 6000 Series
Time=70.8% Open; Amplitude=33.3% Open

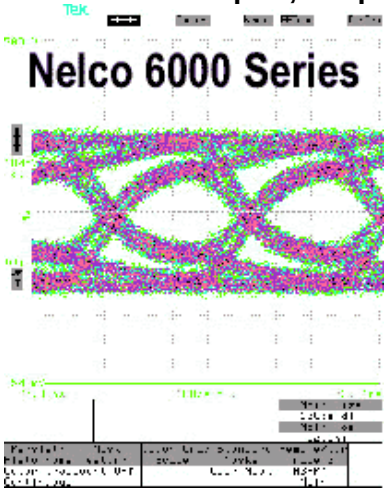


Figure 33. Megtron
Time=66.7% Open; Amplitude=23.3% Open

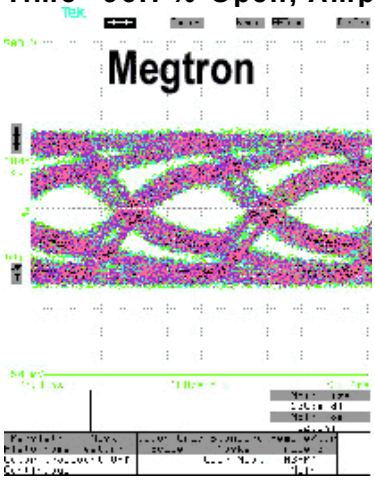


Figure 34. FR–4
Time=50% Open; Amplitude=16.7% Open

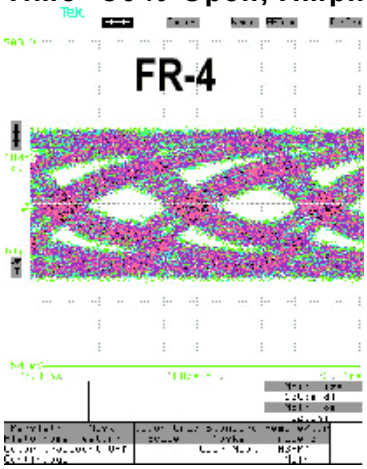
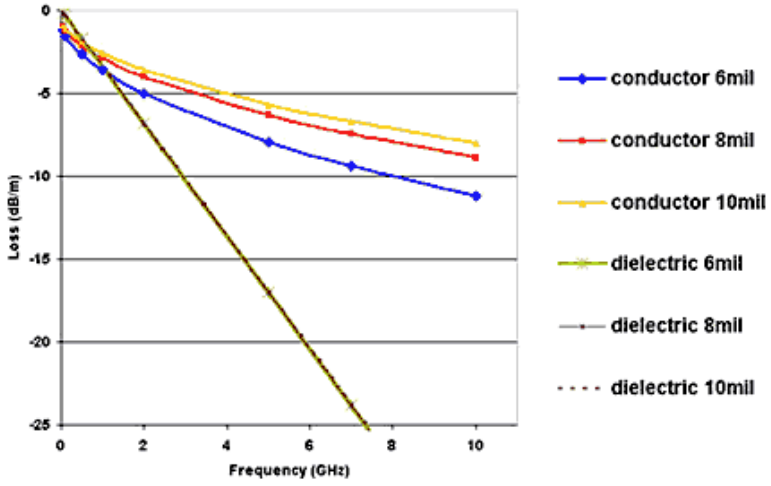


Figure 35. Comparison of Conductor and Dielectric Losses



Self-Test

1. For the study presented in this tutorial, _____ Gbps was chosen as the data rate for sample system comparison.

    a. 1.25

    b. 2.5

    c. 3.5

    d. 5

2. Which of the following differential trace topologies demonstrates marked superiority?

    a. broadside-coupled lines

    b. edge-coupled lines

    c. neither

3. _____ percent risetimes are a better indicator of conductive losses.

    a. 10 to 50

    b. 20 to 80

    c. 10 to 90

4. _____ percent risetimes are a better indicator of dispersive losses.

    a. 10 to 50

    b. 20 to 80

    c. 10 to 90

5. At high frequencies or fast data rates, using lower loss materials yields more dramatic results than increasing line widths.

    a. true

    b. false

6. Material losses amalgamate with copper losses.

    a. true

    b. false

7. New low-loss material processes and mechanical attributes are much the same as FR–4 and should not be a consideration or concern in new designs.

    a. true

    b. false

8. In order to realize a large electrical advantage from a padded surface mount interconnect system, use it in conjunction with blind and buried or micro-vias.

    a. true

    b. false

9. When individual components are integrated, overall performance will behave the same as the sum of the individual components.

    a. true

    b. false

10. Standard PTHs for press-fit pins suffer which of the following problems?

    a. increased costs as compared to micro or blind and buried vias.

    b. electrical degradation caused by capacitance and stubbing effects.

    c. additional capacitance from large surface pads.

Correct Answers

1. For the study presented in this tutorial, _____ Gbps was chosen as the data rate for sample system comparison.

    a. 1.25

    b. 2.5

    c. 3.5

d. 5

See Topic 1.

2. Which of the following differential trace topologies demonstrates marked superiority?

   a. broadside-coupled lines

   b. edge-coupled lines

   c. neither

   See Topic 2.

3. _____ percent risetimes are a better indicator of conductive losses.

   a. 10 to 50

   b. 20 to 80

   c. 10 to 90

   See Topic 2.

4. _____ percent risetimes are a better indicator of dispersive losses.

   a. 10 to 50

   b. 20 to 80

   c. 10 to 90

   See Topic 2.

5. At high frequencies or fast data rates, using lower loss materials yields more dramatic results than increasing line widths.

   a. true

   b. false

   See Topic 3.

6. Material losses amalgamate with copper losses.

   a. true

   b. false

   See Topic 3.

7. New low-loss material processes and mechanical attributes are much the same as FR–4 and should not be a consideration or concern in new designs.

   a. true

   b. false

   See Topic 4.

8. In order to realize a large electrical advantage from a padded surface mount interconnect system, use it in conjunction with blind and buried or micro-vias.

   a. true

   b. false

   See Topic 5.

9. When individual components are integrated, overall performance will behave the same as the sum of the individual components.

   a. true

   b. false

   See Topic 6.

10. Standard PTHs for press-fit pins suffer which of the following problems?

    a. increased costs as compared to micro or blind and buried vias.

    b. electrical degradation caused by capacitance and stubbing effects.

    c. additional capacitance from large surface pads.

    See Topic 5.

Glossary

PCB
printed circuit board

PRESMT
press-fit surface-mount technology

PTH
plated-through hole

PWB
printed wiring board

SISMT
semi-intrusive surface-mount technology

TCE
temperature coefficients of expansion

TDR
time domain reflectometer

TDT
time domain transmission

VHMD®
Teradyne's very–high density metric connector

VNA
vector network analyzer