EXHIBIT F

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Magma readies assault in RTL synthesis arena

By Richard Goering , EE Times
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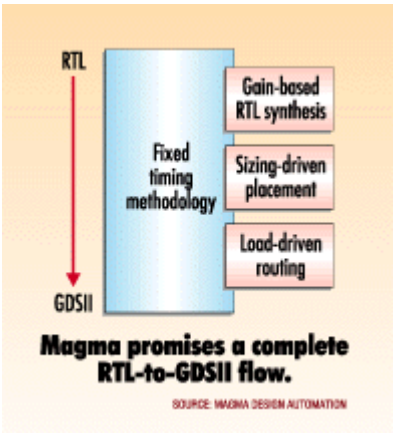
CUPERTINO, Calif. — In a move that underscores its determination to challenge the near-monopoly of Synopsys Inc. in register-transfer level (RTL) synthesis, startup Magma Design Automation will reveal plans to field what it calls gain-based synthesis technology in the second quarter. Vigorously refuting rumors that its technology is "vaporware" or that it's losing money or people, Magma is asserting that it intends to quickly become an EDA industry market leader.

Rajeev Madhavan, president and chief executive officer of Magma, accused Cadence Design Systems Inc. of waging a "public relations war" in an attempt to discredit his company. He said that Magma has had little employee attrition, has won some $51 million in financing and has customers such as Sun Microsystems, Advanced Micro Devices, Realchip, 3D Labs and Fujitsu.

"Absolutely, I believe Magma is headed for an IPO," said Madhavan. "Our goal is to be one of the top two [EDA vendors] by the end of 2002."



Magma promises a complete RTL-to-GDSII flow.
SOURCE: MAGMA DESIGN AUTOMATION

Along with rival startup Monterey Design Systems, Magma fields a complete IC physical design system that could, in theory, uproot existing products from Cadence and Avanti Corp. Now Magma is preparing to add an RTL synthesis capability that will compete head-on with Synopsys' Design Compiler and Physical Compiler, as well as with Cadence's Envisia PKS and Avanti's Jupiter tools.

When combined with the company's Blast Fusion, Magma said its new synthesis technology will provide a complete RTL-to-GDSII design flow based on the company's FixedTime methodology, in which timing is determined up front and held as a constant. The company promises to implement multimillion-gate chips with the best possible timing, with zero iterations and a greatly compressed design cycle.

Single data model

"Our system is all based on one data model that starts with RTL and reads out GDSII," said Bob Smith, Magma's vice president of marketing. "The net-list level goes away and isn't important anymore."

Besides synthesis, Magma is starting to talk about its signal-integrity technology, which includes crosstalk and antenna features already in Blast Fusion and other capabilities to be added in the second quarter.

The term "gain-based synthesis" means that Magma's technology will hold constant the ratio of output capacitance to input capacitance, or "gain," throughout the design flow. "Before layout, you can't have any foreknowledge of what the actual parasitic capacitance will be, yet it's been proven you can predict the performance of a network by using these ratios," said Smith. "The trick is, when you do layout, you have to control these ratios. That's what our product does."

Gain-based synthesis, Smith said, does not use wire-load models. Instead of running placement to get approximate wire loads, it looks at the network topology in terms of gain. The technology uses Magma's constant-delay "supercells."

But Synopsys doesn't see Magma as a major competitive threat, said Sanjiv Kaul, vice president and general manager of the physical synthesis unit of Synopsys. "Magma has made some very strong statements about what they can do, but I haven't seen proof of them yet providing high-value results," he said.

Kaul challenged Magma's notion that timing can be determined up front and held constant. "You can't guarantee timing early and have that be the best possible time you can get out of silicon," he said. "And you can't hold one of the variables constant and not affect other things. When you use a constant-delay algorithm, it usually comes at the expense of area and power."

Gary Smith, principal EDA analyst at Dataquest Inc., said Magma has good synthesis technology that can accommodate large blocks, and a strong synthesis-to-layout flow. But the company's benchmarks so far are against conventional Synopsys-to-Cadence or Synopsys-to-Avanti flows, he noted. Smith said that newer tools, such as Physical Compiler and Envisia PKS, may show different results.

Magma claims that its new synthesis technology will be able to handle 4 million gates flat, and tackle hierarchical designs as well. It doesn't currently offer power optimization, but doesn't really need to, said Madhavan. "Because of the way constant delay works, every cell in the design is only driving what it needs to drive. Power consumption is lower than anything out there today," he said.

Madhavan said that no new ASIC libraries will be needed, since Magma licenses the Synopsys Liberty format and also reads Library Exchange Format and Design Exchange Format files. He named Fujitsu as the company's first major ASIC customer, but added that "every ASIC vendor is benchmarking Magma at this point."

The synthesis technology will also read in Synopsys design constraints and use the Synopsys VHDL and Verilog RTL language subsets, Madhavan said. Thus, he said, it will be very easy for a Design Compiler user to run benchmarks.

Madhavan also said that Magma provides a floor-planning and global routing capability that can be used for RTL synthesis, comparable to Synopsys' Chip Architect; that the company does scan insertion, as does Synopsys' Test Compiler; and that it provides arithmetic and data-path functions similar to those available in Synopsys' DesignWare library.

Magma's approach to merging synthesis with layout is much more serial than that adopted by Synopsys or Cadence, in which synthesis runs interactively along with placement. "Our flow is a stepwise refinement of certain variables," said Madhavan.

Yet synthesis and layout are really part of the same three-part process, he said. "Early on we fix the gain. Subsequently we fix the size to hold the gain constant, and the third thing we do, in the detailed router, is to fix the load to keep the delay and size constant," Madhavan said.

That flow, he said, depends on some new technology. This includes a "sizing-driven" placer as opposed to the timing-driven placers used by other EDA vendors. And it requires Magma's load-driven, variable-width, variable-spacing router.

"In timing-driven routing, you are taking critical nets and routing them first," Madhavan said. "With parasitic-driven routing, you are giving capacitance values that every net is to maintain. So while it is routing, it is adjusting the width of the wire or spacing of the wire to meet the budget."

While Magma's claims are impressive, critics still question how real the company's technology is. No customer has publicly announced taping out a chip with Magma's Blast Fusion.

Offstage customers

"Yes, Cadence has this vaporware story, but it's a myth," said Madhavan. He said that one customer — a communications company he cannot mention — has actually taped out a Magma chip that's in fabrication, and that more customer announcements are coming soon.

Paul Estrada, vice president for IC implementation marketing at Cadence, strongly denied that there's a "Cadence PR war" against Magma. He declined to discuss Magma's technology, saying that his company doesn't have enough information to comment.

Late last year, Fujitsu's worldwide system LSI technology group announced major deals with Magma and Monterey. David Dick, director of advanced technology development at Fujitsu, said that early results for both companies' products looked promising but that Fujitsu had so far just run test cases on preproduction code.

Madhavan also moved to counter rumors that Magma is losing money and people. "We've raised $51 million in financing — I don't think any EDA company has done that.

"If we could talk about revenue numbers, it would surprise the industry," Madhavan said. "It's very high. After another three months or so, I really want to talk about it."