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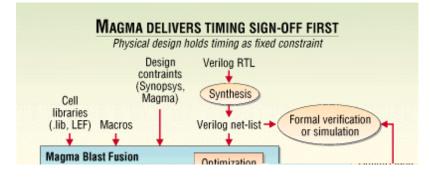


<u>EE Times: Latest News</u> Startup's design tool comes with money-back guarantee

Richard Goering <u>Richard Goering</u> (04/28/1999 5:17 PM EDT) URL: <u>http://www.eetimes.com/showArticle.jhtml?articleID=18301475</u>

CUPERTINO, Calif. — Startup Magma Design Automation Inc. has fielded an approach to IC physical design that promises timing closure, and it is backing that promise with an unusual money-back guarantee. Blast Fusion, the latest in a string of new products challenging EDA market leaders, promises to slash chip design time while boosting area, timing and power optimization. It also challenges prevailing industry perceptions of the need to merge synthesis with layout.

Magma claims Blast Fusion's FixedTiming methodology differs from all competing solutions because it is used before physical design begins to determine whether timing constraints can be met. If they can, Magma promises a layout that meets or beats the constraints; if not, the company promises that no other automated place-and-route system will be able to meet the constraints, either. And Magma says it will refund the user's license fee if those conditions aren't met.



With some 68 employees and \$24 million in venture-capital funding, Magma is an unusually well-heeled EDA startup. The company was launched in 1997 by president and chief executive Rajeev Madhavan, an earlier founder of Ambit Design Systems and Logic Vision.

Madhavan called Magma's approach "revolutionary" because it guarantees timing "up-front in the design process." Competing physical design tools, he said, keep area fixed and let timing vary in an attempt to "converge" on timing. Magma's approach is just the opposite: Timing is held as a fixed constraint and the physical layout is manipulated to meet it.

By offering a complete physical-design system, including floor planning, placement, routing, extraction and verification, Magma will compete head-on with Cadence Design Systems Inc., Avant! Corp. and Synopsys Inc.

It will also compete against Monterey Design Systems, which just announced a single tool that includes all <u>physical design</u> <u>functions</u>.

The two startups nonetheless have different approaches. While Monterey speaks of "simultaneous" execution of the various physical-design steps, Magma is using what Madhavan called a "non-iterative, correct-by-construction flow" with no iterations, even within Blast Fusion. <u>Magma (Cupertino, Calif.)</u> thus appears to have a more sequential methodology.

Unlike Monterey, Magma is naming customers and providing benchmark data. Magma claims Sun and Advanced Micro Devices as customers and has received endorsements from Fujitsu, Gigapixel and Artisan Components. Magma's benchmarks claim 10 to 15 percent better timing performance and 20 to 25 percent reductions in cell area compared with existing tools. And in one customer design, Magma claims to have reduced the design cycle from four months to two weeks.

The solution comes in two pieces. Blast Speed is the front-end timing-optimization portion; it could be sold to ASIC designers who don't do layout. Blast Builder, the integrated place-and-route solution, could be sold to ASIC vendors or to designers who go all the way through layout.

One implication of Magma's approach is that it potentially makes gate-level ASIC signoff, thought to be a dying methodology, viable once again. ASIC designers who use Blast Speed, Magma claims, can be assured their chips will meet timing if the vendor uses Blast Builder.

That challenges the common wisdom on the merger of synthesis and layout. "Synthesis is not the place to make any timing decisions," argued Madhavan, who said that synthesis tools don't need placement information and that physical design does not need to feed any information back to synthesis.

Blast Fusion takes synthesized, gate-level net-lists but does not use the wire-load models employed by synthesis. "We throw out all the assumptions made by synthesis," said Bob Smith, Magma's vice president of marketing and business development.

The startup is so confident of its approach that it offers the Magma Performance Guarantee (MPG), which promises to refund the user's license fee if Blast Fusion can't deliver a final, post-layout timing number that equals the original "sign-off" number and if Magma cannot correct the deficiency in 90 days. MPG assumes the use of Blast Speed and Blast Builder without the insertion of third-party tools into the process.

Madhavan said Magma will market Blast Speed to silicon intellectual-property vendors, which could then take soft cores through the timing optimizer and provide a timing number that the core is guaranteed to meet, as long as Blast Builder is used for the chip's physical design. "Many IP vendors are interested, because today they can't tell customers what timing will be before layout," he said.

Keeping timing as a fixed constraint called for some new approaches. Madhavan noted that existing layout tools change the delay (by varying either cell sizing or loading), measure the results and then make more changes in an attempt to converge on timing. Blast Fusion, in contrast, has already "converged," so it holds the delay as a constant while varying both sizing and loading.

"Every cell in the design is sized to meet the load it's driving," said Smith. He noted that Blast Fusion sizes cells on all paths, not just critical paths, because even non-critical paths can suffer from being over-driven.

'Supercells' process

But cell sizing is postponed until detailed placement and global routing are complete. Magma employs "supercells," which have a fixed delay but a variable size, throughout most of the design process. Supercells are automatically extracted from the logical ASIC library and are replaced with actual library cells only after the wire loads are known.

Magma has developed a "virtual gridless" router that can perform variable width and spacing of metal lines to fine-tune loads and to automatically compensate for signal-integrity problems. Because Blast Fusion operates off one integrated data model, the router can call other functions, such as resistance-capacitance extraction, as needed.

The input to Blast Speed includes a gate-level Verilog net-list, design constraints, a physical library in Library Exchange Format (LEF) and a logical library in .lib format. Timing constraints can be specified in Synopsys format. The initial offering accepts only timing constraints but power constraints will be added, Smith said.

Blast Speed optimizes timing based on supercells and fixes timing for all paths. It restructures the net-list to reduce levels of logic and uses an integrated formal verifier to check for accuracy. It then provides the sign-off timing number on which Magma bases its guarantee.

Blast Builder progresses through area optimization, which freezes cell sizes and placements, and wire optimization, which freezes loads. It takes in the proprietary Lava data model produced by Blast Speed. The user does some floor planning, but not to determine wire loads, Madhavan noted; the purpose of Magma's floor planning goes back to the original intent of the tools,

which is to avoid congestion.

During area optimization, placement is concurrent with global routing so that placement can obtain load estimates. Magma's "force-directed" placement technique is said to provide a uniform congestion while sizing all cells in the design.

The Blast Fusion line is available now with time-based licensing. Blast Speed is \$90,400 per year, Blast Builder is \$255,750 per year and the full Blast Fusion solution is \$330,600 per year. An additional product, Blast Warp, is offered to foundries for library compilation.

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