EXHIBIT B, PART TWO

slack" which is the single "worst" slack number. If the network slack is non-negative, then timing closure is achieved. If the predicted slack calculated in step 650 is larger than the network slack, then it is possible to insert a buffer without increasing the circuit delay.

In step 655, it is determined whether the added area due to buffer insertion does not exceed the area saved by sizing down the source gate. The added area (by inserting the buffer) is equal to the area of the buffer multiplied by the buffer size, wherein the buffer size is determined by the buffer load C divided by the typical load C/S on the buffer. The area saved by sizing down the source gate is determined by first calculating the change in net load due to the buffer insertion. This net load change is due to the following: (1) some sinks (which sink currents) are removed, (2) the input load of the buffer is added, and (3) the number of fanouts of the gate may change.

Using the net weight equation (6), the impact of buffer insertion on the work area can be

estimated (step 660). In step 665, the buffer is inserted if the impact on the circuit area is positive (i.e., the circuit area is reduced). After the buffer has been inserted, then in step 670 the capacitance values need to be updated in the fanin cone of the buffer, while the net weights need to be updated in the fanout cone of the buffer. This updating step serves to keep the net weights accurate, while limiting the net weight re-calculation to those portions of the circuit affected by buffer insertion.

Fig. 8A shows a gate 680 which has buffers 685 and 690 inserted in the gate 680 output load. The buffers 685 and 690 permit the gate 680 to be sized down. The buffers 685 and 690 are inserted if the area impact on circuit 692 is positive (i.e., the area of circuit 692 is reduced due to buffering).

Buffer insertion is a method for optimizing the circuit area. As a result of buffer insertion, the timing of the circuit becomes slower, but the circuit timing will still meet the timing constraints. Buffer insertion causes the net delay

to increase due to the added delay from the buffer. For those portions of the circuit where timing constraints have already been met, adding buffers can still result in meeting the previously determined timing constraints.

While it is preferred to stay within the timing constraints, it is within the scope of the present invention to go beyond the timing constraints and to correct the circuit later in the design process so that the timing constraints are eventually met. Additionally, where it is determined that saving area is of more significance than in meeting timing constraints, buffers can be inserted to save area, even though the previously determined timing constraints are not met. Many paths in a circuit do not have the critical timing requirements, and thus, buffers can be inserted in these paths to save area.

Compressing or Stretching of Gate Delays

Prior to cell placement, the delays of the individual gates may be stretched or compressed to

meet the delay constraints, as shown in step 220 of Fig. 4. As shown in Fig. 9A, by compressing (decreasing) the delay of a given gate, the gate gain decreases. Gates which are on long paths not meeting the delay constraints are compressed (in delay) until the long paths meet the delay constraints. The delay of the gates (or gate) may be decreased as long as the minimum required gain requirements are met.

By stretching (increasing) the delay of a given gate, the gate gain increases (see Fig. 9A). Gates on short paths which easily meet the delay constraints are stretched (in delay), since gates with stretched delays require less area for the same load. The delay of the gates (or gate) in a path are stretched to the extent that timing constraints for the digital circuit are still met.

The step of stretching and compressing of a gate delay is not related to the adjustment of gate sizes. As stated above, to stretch or compress the gate delay, the gate gain is appropriately adjusted. The stretching and compressing step is

discussed in further detail with reference to Fig. 9 which shows a portion of a digital circuit 750. As an example, the gate 752 has a requirement of driving an output capacitance load (C_{out}) of about 2.0 pico-farads, while having an input capacitance load (C_{in}) of about 0.1 pico-farads. Thus the gain requirement of the gate 752 is C_{out}/C_{in} = 2.0/0.1. The gate 754 is assumed to have an output capacitance load of about 2.0 pico-farads and an input capacitance load of about 0.2 pico-farads. Thus, the gain requirement of the gate 754 is 2.0/0.2.

It is also assumed that the gate 752 has a delay, D=1. It is assumed further that the gate 752 is on a "Path 1" which has an arrival time requirement of about 1 at its beginning point 756 and an arrival time requirement of about 4 at its end point 758. Thus, the delay constraint for Path 1 is equal to about 3, as shown by equation (9):

(9) constraint = arr. time (point 756) - arr. time (point 758)

= 4 - 1 = 3

Since the delay D of gate 752 equals 1 and the delay constraint of Path 1 equals 3, the slack for Path 1 equals 2, as shown by equation (10):

(10) slack = delay constraint - gate(s) delay(s)
= 3 - 1 = 2

It is further assumed that the gate 754 has a delay, D=5. It is assumed further that the gate 754 is on a "Path 2" which has an arrival time requirement of about 1 at its beginning point 760 and an arrival time requirement of about 4 at its end point 762. Thus, the delay constraint for Path 2 is equal to about 3, as shown by equation (11):

(11) constraint = arr. time (point 760) - arr. time (point 762)
= 4 - 1 = 3

Since the delay of gate 754 (D=5) is greater than the Path 2 delay constraint of 3, the delay of gate 754 does not meet the timing constraints.

The invention operates on a path-by-path basis whereby the most critical path in a digital circuit 750 is evaluated first. Thus, Path 1 is evaluated first if it is the most critical path. Path 2 is evaluated first if it is the most critical path. Assuming Path 2 is the most critical path, then the

delay of the gate 754 is compressed to meet the Path 2 delay constraint of 3, while observing the effects on the gain of the gate 754. As stated above, the gain requirement of the gate 754 is $C_{out}/C_{in} = 2.0/0.2$. However, as shown in Fig. 9A, the gain of any particularly sized gate decreases as the gate delay D is decreased. Thus, compression of the gate 754 delay may be limited by its gain requirements.

After the gate 754 has been adjusted to meet the Path 2 timing constraints, it becomes "locked," whereby the gate 754 delay will not be adjusted further for the remainder of the compression and stretching step. It is further noted that if a path contains more than one gate, then, preferably, their delays are compressed (or stretched) in equal amounts to meet the path timing constraints. For example, assume that four (4) gates are in a given path and two (2) nano-seconds of delay can be added to the given path. Then according to a preferred embodiment of the invention, 0.5 nano-seconds of delay can be added to each of the four (4) gates to

equally distribute the two nano-seconds of delay which is to be added in the given path.

The invention then proceeds to evaluate the next critical path. Assume that Path 1 is the next most critical path. In Fig. 9, the delay of gate 752 (D=1) meets the Path 1 delay constraint of 3, and thus the gate 752 delay can be stretched based on a slack of 2. The gate 752 is then locked after its delay is stretched. If a plurality of gates are on Path 1, then preferably, their delays are stretched in equal amounts.

The invention will then evaluate the next critical path, whereby gate delays may be stretched or compressed. When reducing slack values during the gate delay stretching step, it is preferable to maintain a small amount of slack for a path, in order to compensate for downstream delay effects, such as wire delay. Additionally, in some instances, library rules may limit the amount of slack value reduction.

For the purpose of stretching and compressing, registers in the circuit are preferably considered

as part of a path from which they originate, but not part of the path from which they terminate. The stretching and compressing steps are further shown in the flowchart of Fig. 9B. In step 770, the most critical path on the circuit is evaluated, and in step 775, the delay of a gate (or gates) in the path are stretched or compressed. In step 780, the next critical path is evaluated, and in step 782, the delay of a gate (or gates) in the path are stretched or compressed. In step 784, if all paths have not been evaluated, then the invention returns to step 780 to evaluate the next critical path. If in step 784 all paths have been evaluated, then the invention proceeds to step 785 wherein placing of cells may be performed.

Cell Placement

In step 225 (Fig. 4), the placement of cells is performed. Figs. 10A and 10B show how a circuit design is transformed from a logical hierarchy 830 to a physical hierarchy 832 during the cell placement step 225 (Fig. 4). In the physical

hierarchy 832, the intermediate logic levels in the logical hierarchy 830 are associated in or grouped in buckets 834 wherein each bucket 834 holds, for example, about one-hundred (100) cells 836. The buckets 834 are arranged in an array as shown in Fig. 10C. If the designer chooses to keep a group of cells 836 together, then the group of cells 836 are grouped in the same buckets 834 or in neighboring buckets. Preferably, a bucket 834 is sized small enough such that cell placement within a bucket 834 has an insignificant effect on timing. In other words, the size of a bucket 834 is such that the wire delay in a bucket 834 can be ignored. However, the size of a bucket 836 should be large enough to accommodate remapping and resizing of the cells 836 contained in the bucket. The number of cells which can be placed within a bucket can range, preferably, from about 20 cells to about 200 cells.

Pre-routes and pre-places (for driving the placer and global router) are driven into the bucket 834 structure. It is further noted,

however, that the present invention may be practiced or incorporated with conventional placement methods and systems.

According to the present invention, timing closure is maintained after placement occurs of cells 836. To maintain timing closure, the size of a particular gate may be adjusted during or after placement. This adjustment compensates for the fact that placement algorithm may assign different net lengths to different nets, and that these different net lengths are difficult to predict prior to the placement step. Thus, by the practice of the present invention, the gate sizes are adjusted in order to maintain the delay values which were determined prior to placement.

In contrast, conventional placement methods optimize the length of wires to compensate for changes in delays, due to net length changes caused by the placement algorithm. Thus, conventional placement methods involve costly and lengthy delay analysis avoided by the present invention.

As stated above, equation (8) determines the cell area of the placed cells:

$$(8) \quad A = \sum (w_i)(\omega_i)$$

As also stated above, the parameter ω_i represents the wire load for a given gate (e.g., gate i). Based on equation (8), the area for each gate is determined based on the product, $(w_i)(\omega_i)$. Thus, a given gate i can be sized appropriately, and avoidance is possible of the costly delay analysis required in conventional methods when the actual net lengths differ from the estimated net lengths prior to placement.

Routing of the Digital Circuit

Finally, in step 230 (Fig. 4), routing of the placed circuit is performed to complete the chip layout 235. The routing step places wires which were previously determined during or prior to the placement step. In step 230, gate delay and gate size are fixed. The router thus controls the wire loads to maintain the delay as essentially constant

and thus achieve timing closure. Gate delay and gate size have been previously fixed. The router thus controls the distance 900 (Fig. 11) between, for example, wires 905 and 910. The capacitance between the two wires 905 and 910 decreases as the distance 900 between wires increases. A conventional router can be used to control the distance 900.

This specification shows the components (e.g., buffers, cells, nets) which exist when the integrated circuit layout is produced. However, it is realized by those skilled in the art that when performing the steps in accordance with the present invention prior to producing the layout, the shown components are data representation stored in the computer and not the actual devices.

Thus, while the present invention has been described herein with reference to particular embodiments thereof, a latitude of modification, various changes and substitution are intended in

the foregoing disclosure, and it will be appreciated that in some instances some features of the invention will be employed without a corresponding use of other features without departing from the scope of the invention as set forth.

What is claimed is:

1. An automated method for designing an initial integrated circuit layout with a computer, based upon an electronic circuit description and by using a cell library containing cells that each have an associated relative delay value, comprising the steps of:

(a) selecting a plurality of cells from the cell library that are intended to be coupled to each other with a plurality of wires and that can be used to implement the digital circuit based on the electronic circuit description input to the computer; and

(b) determining, using a portion of a computer program that contains a sequence of instructions, an initial intended area of each of the selected plurality of cells, the initial intended area of at least some of the selected plurality of cells being determined using the associated relative delay value of the selected cell and the initial intended lengths of some of the wires coupled to each of said some cells in order to meet predetermined

timing constraints associated with each of said some cells that are coupled to another cell.

2. The automated method of claim 1 further comprising:

routing the digital circuit to generate the integrated circuit layout using the finalized area of each of the selected plurality of cells and the finalized wire lengths.

3. The automated method of claim 2 further comprising:

prior to the step of routing, finalizing the area of each of the selected plurality of cells and the lengths of the wires.

4. The method of claim 1 wherein the plurality of cells are coupled to each other based on the electronic circuit description input to the computer.

5. The automated method of claim 1 wherein each of the plurality of wires has an associated capacitive load value; and

wherein each wire is associated with a net weight value that represents the sensitivity of the total area of the digital circuit of step (a) with respect to the associated capacitive load value of the wire.

6. The automated method of claim 5 wherein the net weight w_i of the wire coupled to a selected cell is:

$$w_i = \partial A / \partial C_i$$

where A is the total area of the digital circuit of step (a) and C_i is the associated capacitive load of the wire coupled to the selected cell.

7. The automated method of claim 6 wherein the initial intended areas of said some selected cells are chosen based upon the net load w_i in order to meet said predetermined timing constraints.

8. The automated method of claim 1 wherein the initial intended areas of said some selected cells are chosen based upon the length of said some wires coupled to said some selected cell.

9. The automated method of claim 6 wherein the initial intended areas of said some selected cells are chosen based upon the net load w_i of the wires coupled to said some selected cells and the lengths of the wires coupled to said some selected cells.

10. The automated method of claim 1 further comprising:

inserting a buffer in one of the wires of step (a) to reduce an area of a cell coupled to the wire.

11. The automated method of claim 10 wherein the step of inserting the buffer comprises:

determining a wire in the digital circuit of step (a) into which a buffer can be inserted to

reduce an area of a cell coupled to the wire by a specific area size; and

inserting the buffer into the wire if an area of the buffer is less than the specific area size, prior to the step (b) of determining the initial intended area of each of the selected plurality of cells.

12. The automated method of claim 1 further comprising:

stretching the associated relative delay value of a selected cell to decrease the area of the selected cell.

13. The automated method of claim 1 further comprising:

stretching the associated relative delay values of a plurality of selected cells coupled to each other to decrease the area of each of the coupled cells.

14. The automated method of claim 1 further comprising:

compressing the associated relative delay value of a selected cell to assist in satisfying the predetermined timing constraints.

15. The automated method of claim 14 wherein the compressing step is limited by a gain requirement of the selected cell.

16. The automated method of claim 1 further comprising:

compressing the associated relative delay values of a plurality of the selected cells to assist in satisfying the predetermined timing constraints.

17. The automated method of claim 1 wherein a group of said some cells are assigned in buckets and operated upon in order to determined the initial intended area of each of the group of said some cells.

18. The automated method of claim 17 wherein the group of said some cells ranges from 20 to 200 cells.

19. An integrated circuit layout produced in accordance with the automated method of claim 1.

20. An automated method for designing an integrated circuit layout using a computer, based upon an electronic circuit description and based upon cells which are selected from a cell library, each of the cells having an associated area, comprising the steps of:

(a) placing each of the cells in the integrated circuit layout so that the cells can be coupled together by wires to form a circuit path having an associated predetermined delay constraint wherein the cells are coupled together by wires based upon the electronic circuit description input to the computer; and

(b) adjusting an area of at least one of the cells to satisfy the associated predetermined delay constraint of the circuit path.

21. The automated method of claim 20 wherein each of the wires has an associated capacitive load value; and

wherein each wire is associated with a net weight value that represents the sensitivity of the total area of the integrated circuit layout with respect to the associated capacitive load value of the wire.

22. The automated method of claim 21 wherein the net weight w_i of the wire coupled to a cell is:

$$w_i = \partial A / \partial C_i$$

where A is the total area of the integrated circuit layout and C_i is the associated capacitive load of the wire coupled to the cell.

23. The automated method of claim 22 wherein the

areas of at least some of the cells are chosen based upon the net load w_i in order to meet said predetermined timing constraints.

24. The automated method of claim 20 wherein the areas of said some cells are chosen based upon the lengths of at least some of the wires coupled to said some cells.

25. The automated method of claim 22 wherein the areas of said some selected cells are chosen based upon the net load w_i of the wires coupled to said some selected cells and the lengths of the wires coupled to said some selected cells.

26. The automated method of claim 20 further comprising:

inserting a buffer in one of the wires of step (a) to reduce an area of a cell coupled to the wire.

27. The automated method of claim 20 further

comprising:

stretching the associated relative delay value of a selected cell to decrease the area of the selected cell.

28. The automated method of claim 20 further comprising:

compressing the associated relative delay value of a selected cell to assist in satisfying the predetermined timing constraints.

29. The automated method of claim 28 wherein the compressing step is limited by a gain requirement of the selected cell.

30. The automated method of claim 20 wherein a group of said some cells are assigned in buckets and operated upon in order to determined the initial intended area of each of the group of said some cells.

31. The automated method of claim 30 wherein the group of said some cells ranges from 20 to 200 cells.

32. An integrated circuit layout produced in accordance with the automated method of claim 20.

33. An automated method for designing an integrated circuit layout of at least four cells by using a computer and based upon an electronic circuit description containing information on the digital circuit, comprising the steps of:

(a) selecting a plurality of cells which can be used to implement the digital circuit based upon the electronic circuit description, each of the plurality of cells having an associated load, the plurality of cells comprising a first cell having a first load, a second cell having a second load, a third cell having a third load, and a fourth cell having a fourth load, each of the cells and the associated load having a predetermined associated delay value;

(b) determining initial placement locations for each of the selected plurality of cells including the first cell, the second cell, the third cell, and the fourth cell;

(c) setting the size of each of the selected plurality of cells and the loads of each cell so that the predetermined associated delay value of at least some of the selected plurality of cells with associated loads remain relatively constant; and

(d) routing the digital circuit based on the finalized location and size of each of the selected plurality of cells.

34. The automated method of claim 33 wherein each of the load has an associated capacitive load value; and

wherein each load is associated with a net weight value that represents the sensitivity of the total area of the integrated circuit layout with respect to the associated capacitive load value of the load.

35. The automated method of claim 34 wherein the net weight w_i of the load coupled to a cell is:

$$w_i = \partial A / \partial C_i$$

where A is the total area of the integrated circuit layout and C_i is the associated capacitive load of the load coupled to the cell.

36. The automated method of claim 35 wherein the areas of at least some of the cells are chosen based upon the net load w_i in order to meet said predetermined timing constraints.

37. The automated method of claim 33 wherein the areas of said some cells are chosen based upon the lengths of at least some of the wires coupled to said some cells.

38. The automated method of claim 36 wherein the areas of said some selected cells are chosen based upon the net load w_i of the loads coupled to said some selected cells and the lengths of the loads coupled to said some selected cells.

39. An integrated circuit layout produced in accordance with the automated method of claim 32.

40. An automated method for determining an integrated circuit layout of at least four cells by using a computer and based upon an electronic circuit description containing information on the digital circuit, the automated method comprising the steps of:

(a) selecting a plurality of cells which can be used to implement the digital circuit using the electronic circuit description, the plurality of cells each comprising a first cell having a first load and a first predetermined timing constraint, a second cell connected to the first cell and having a second load and a second predetermined timing constraint, a third cell connected to the second cell and having a third load and a third predetermined timing constraint, and a fourth cell connected to the third cell and having a fourth load and a fourth predetermined timing constraint;

(b) determining the placement locations for each of the selected plurality of cells including the first cell, the second cell, the third cell, and the fourth cell;

(c) selecting the size of the first cell based on the first load of the first cell and on the first predetermined timing constraint;

(d) selecting the size of the second cell based on the second load of the second cell and on the first predetermined timing constraint and the second predetermined timing constraint;

(e) selecting the size of the third cell based on the third load and on the first predetermined timing constraint, the second predetermined timing constraint and the third predetermined timing constraint;

(f) selecting the size of the fourth cell based on the fourth load and on the first predetermined timing constraint, the second predetermined timing constraint, the third predetermined timing constraint, and the fourth predetermined timing constraint;

(g) routing the digital circuit based on the placement location and size of each of the selected plurality of cells.

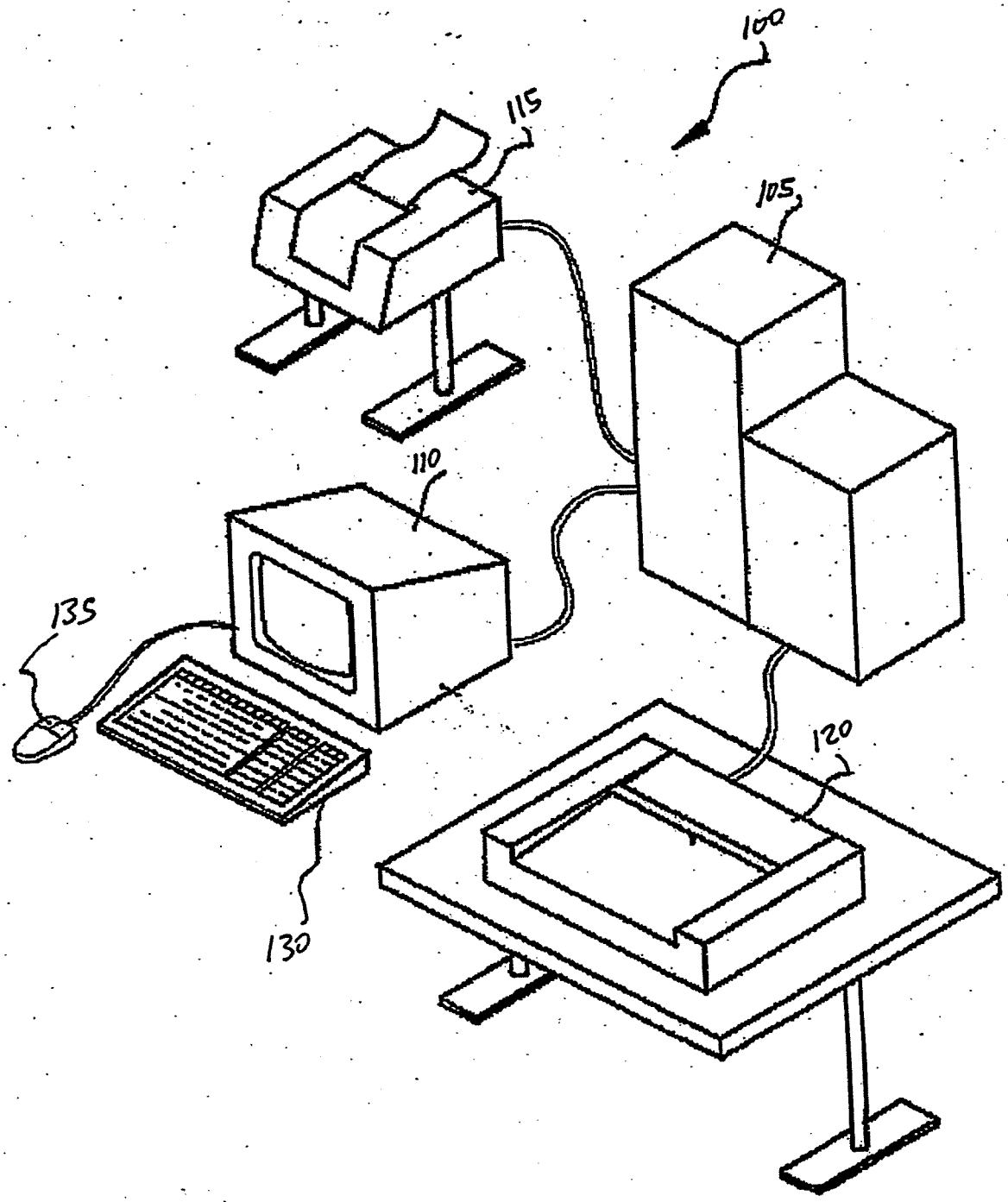
41. An integrated circuit layout produced in accordance with the automated method of claim 40.

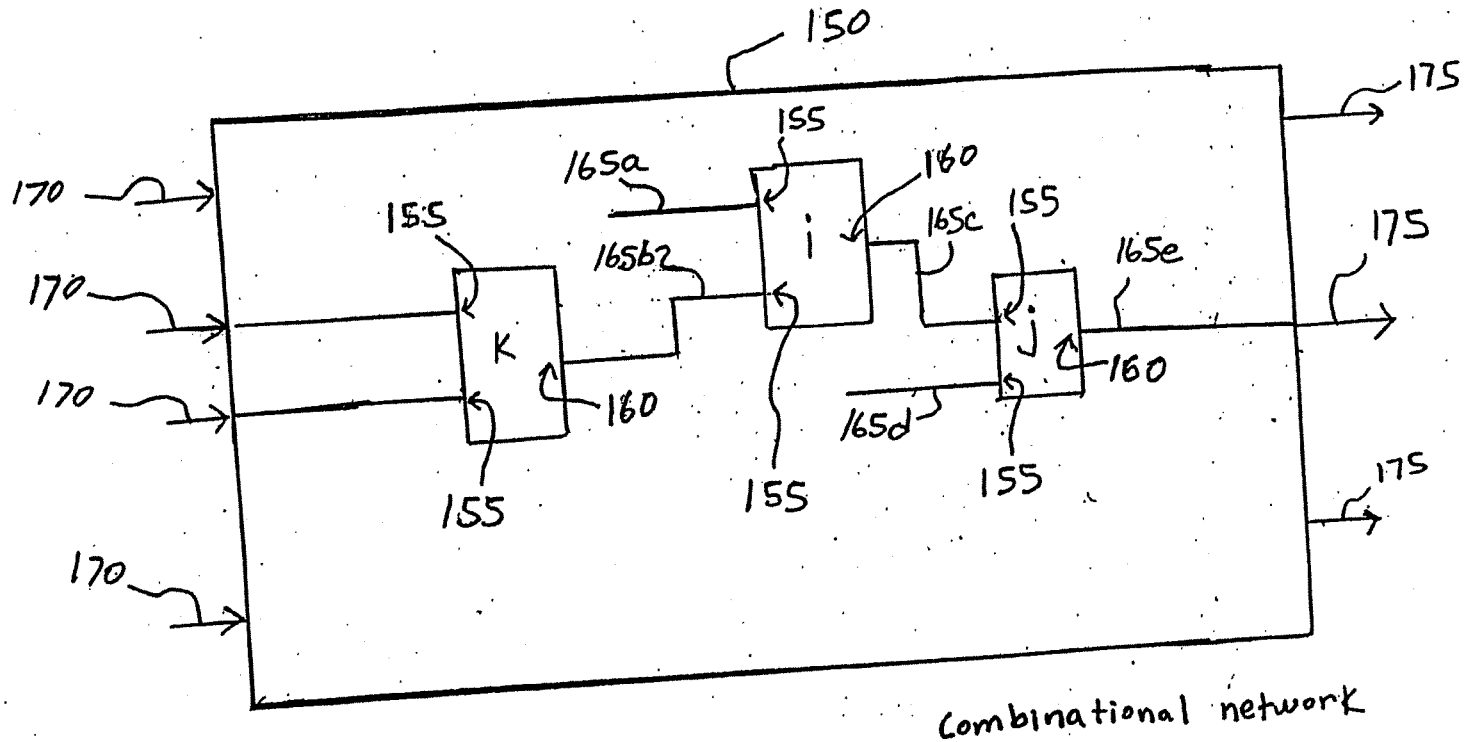
Abstract of the Invention

TIMING CLOSURE METHODOLOGY

An automated method for designing an integrated circuit layout using a computer based upon an electronic circuit description and based upon cells which are selected from a cell library, each of the cells having an associated area, comprising the steps of: (a) placing each of the cells in the integrated circuit layout so that the cells can be coupled together by wires to form a circuit path having an associated predetermined delay constraint wherein the cells are coupled together based upon the electronic circuit description input to the computer; (b) connecting the cells together with the wires to form the circuit path; and (c) adjusting an area of at least one of the cells to satisfy the associated predetermined delay constraint of the circuit path.

FIG. 1

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170
155
165c
155
175
165b2
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170
K
i
j
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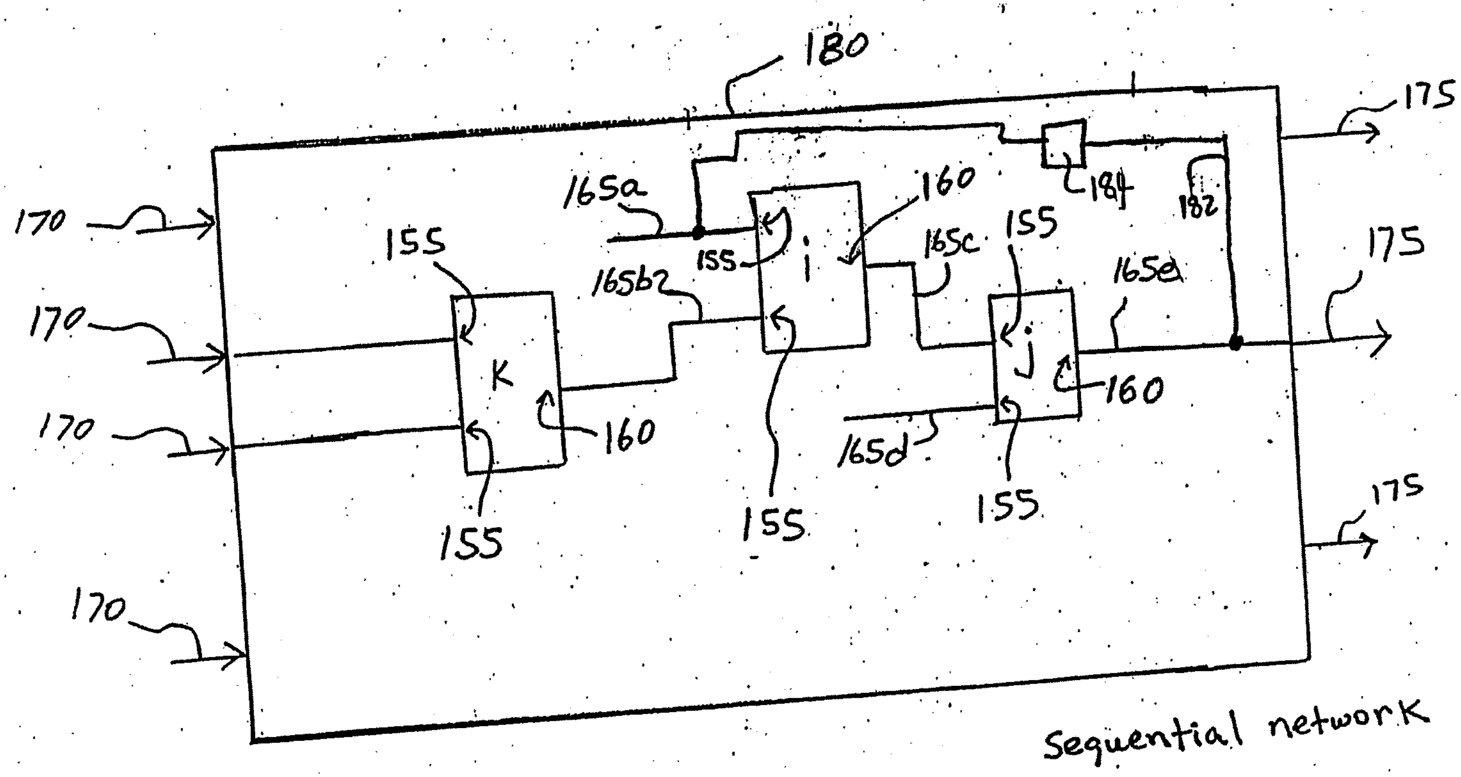
170
160
165d
155
155
155
175
170
combinational network

Fig. 2



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165a
165b2
165c
165d
165e
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160
K
i
j
184
182
Sequential network

Fig. 3

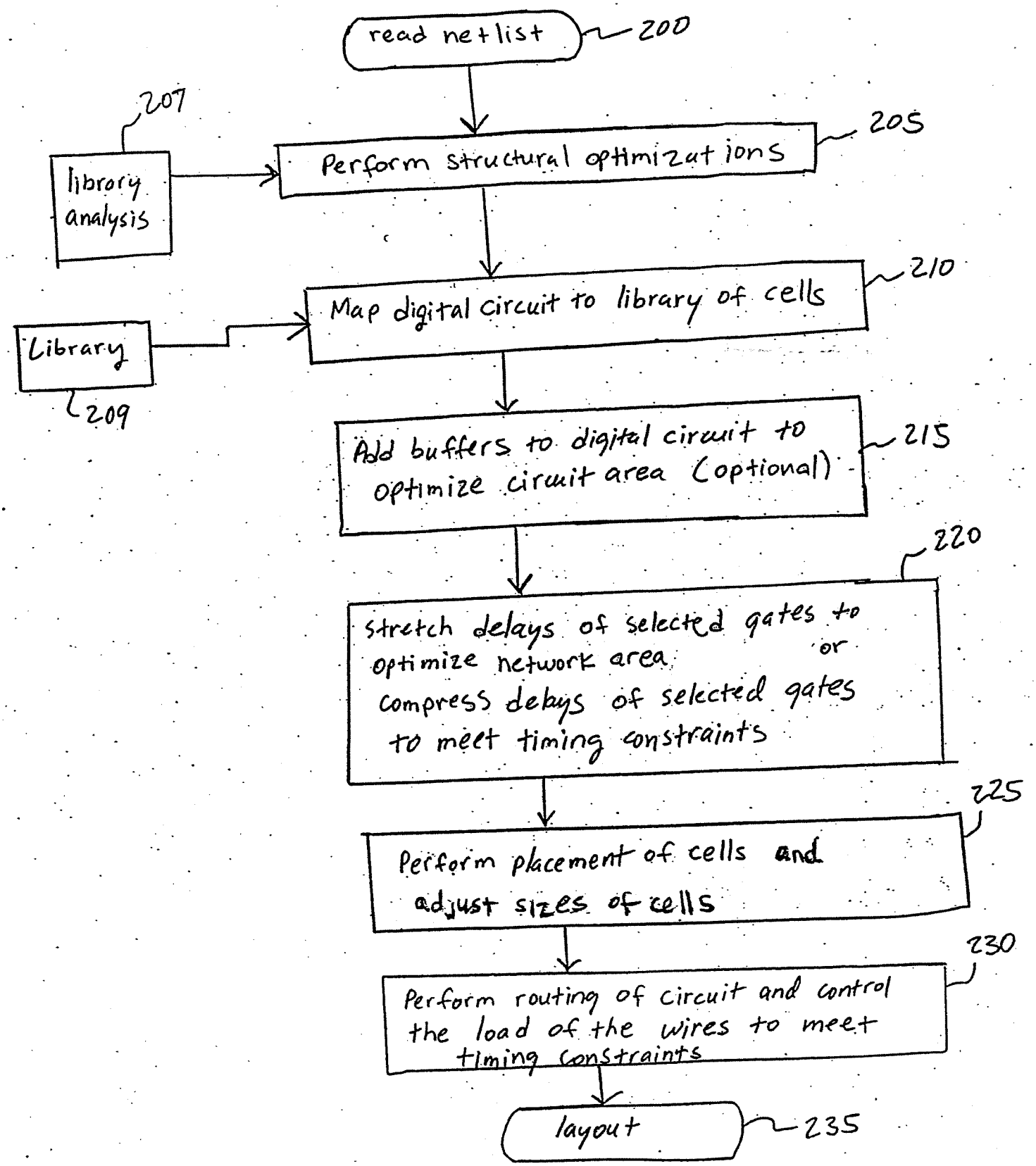

read netlist
200
207
library analysis
Perform structural optimizations
205
Map digital circuit to library of cells
210
Library
209
Add buffers to digital circuit to optimize circuit area (optional)
215
220
stretch delays of selected gates to optimize network area
or
compress delays of selected gates to meet timing constraints
225
Perform placement of cells and adjust sizes of cells
230
Perform routing of circuit and control the load of the wires to meet timing constraints
layout
235

Fig. 4

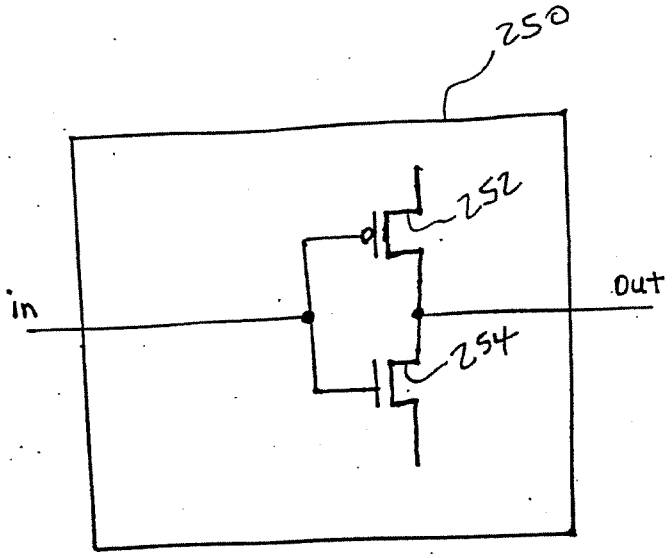


Fig. 4A

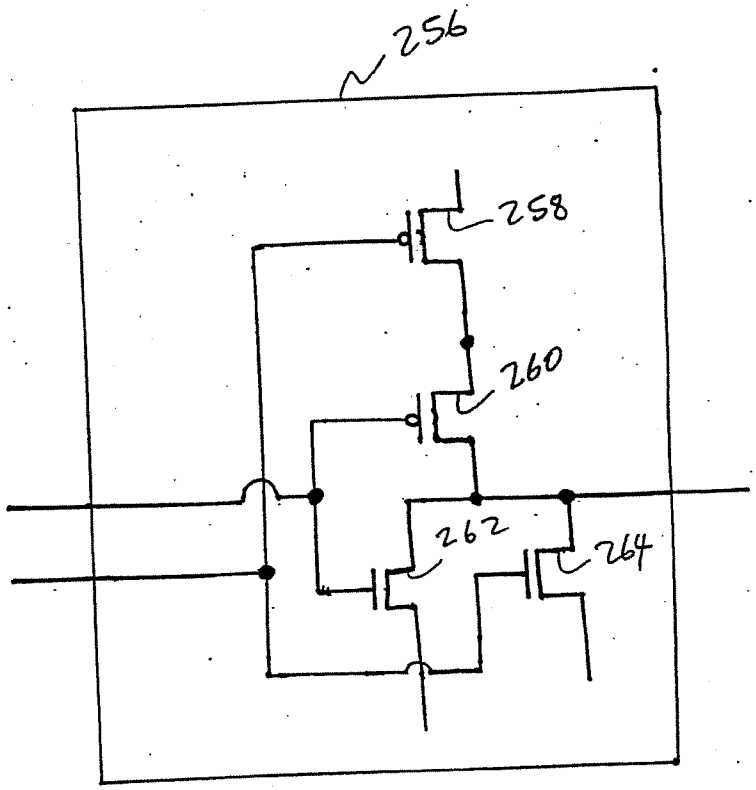


Fig. 4B

Mapping

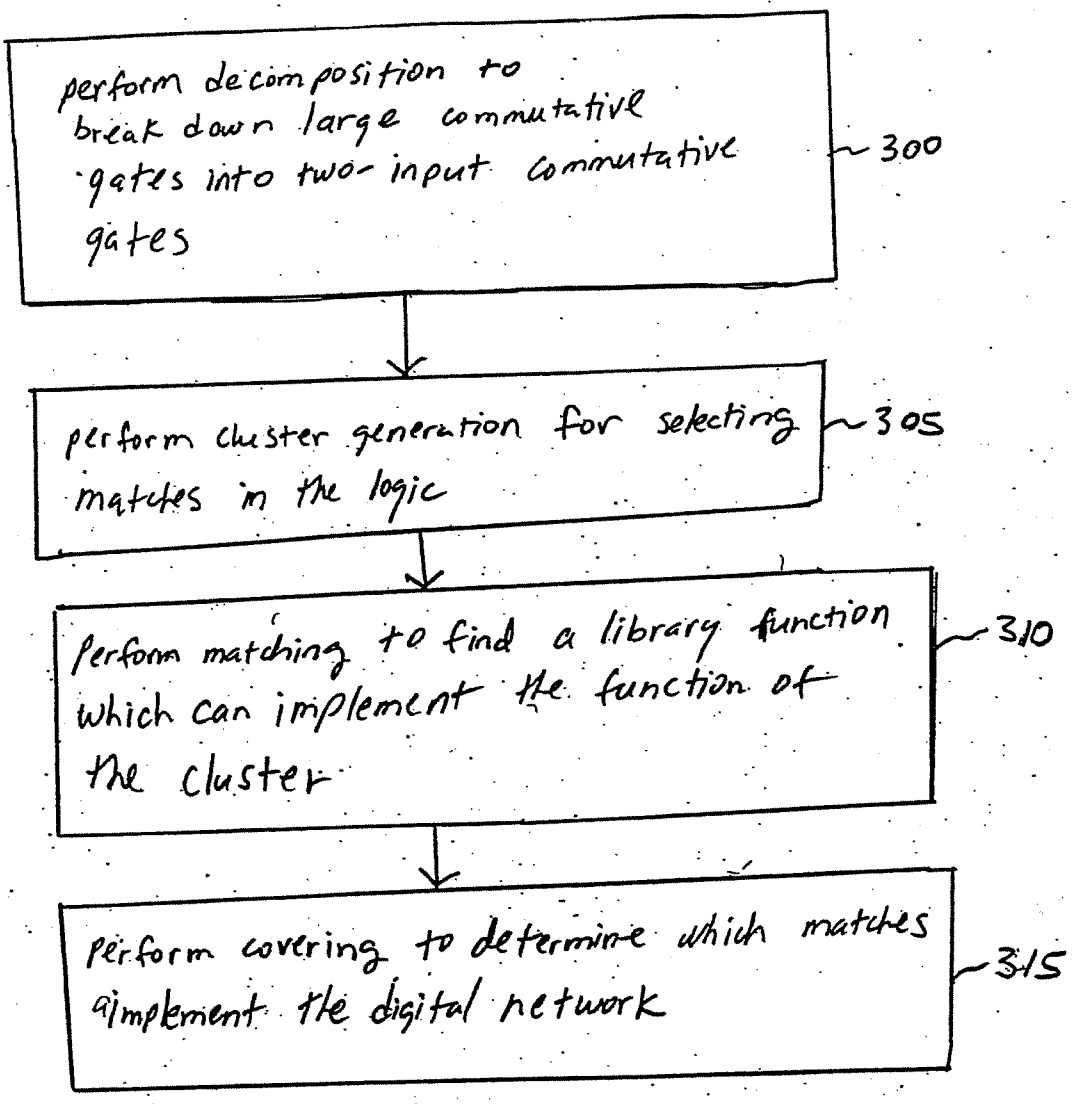


Fig. 5

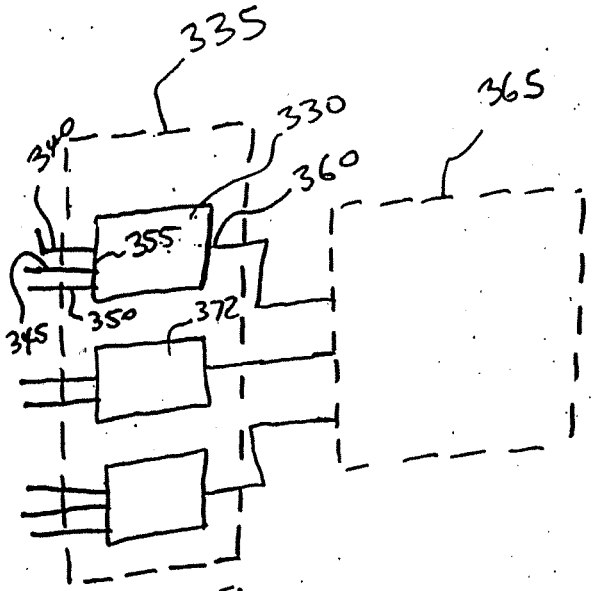


Fig. 6A

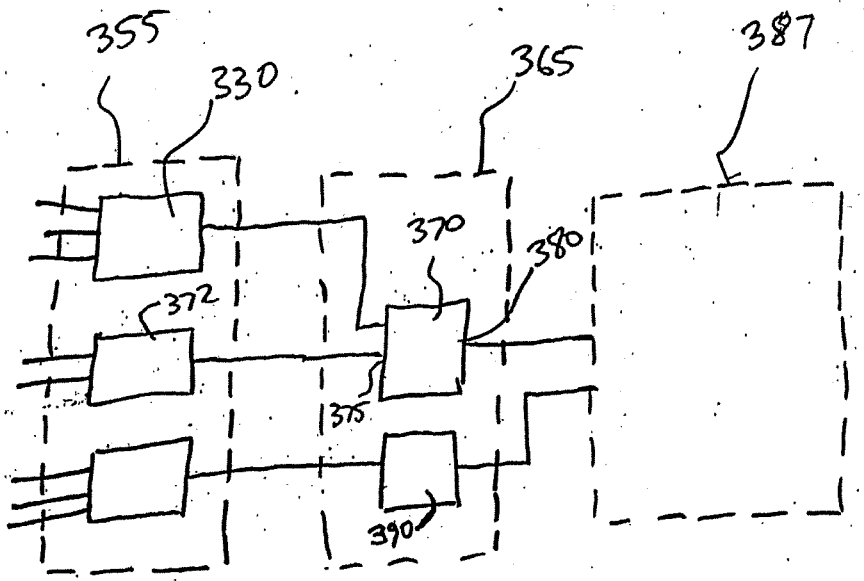


Fig. 6B

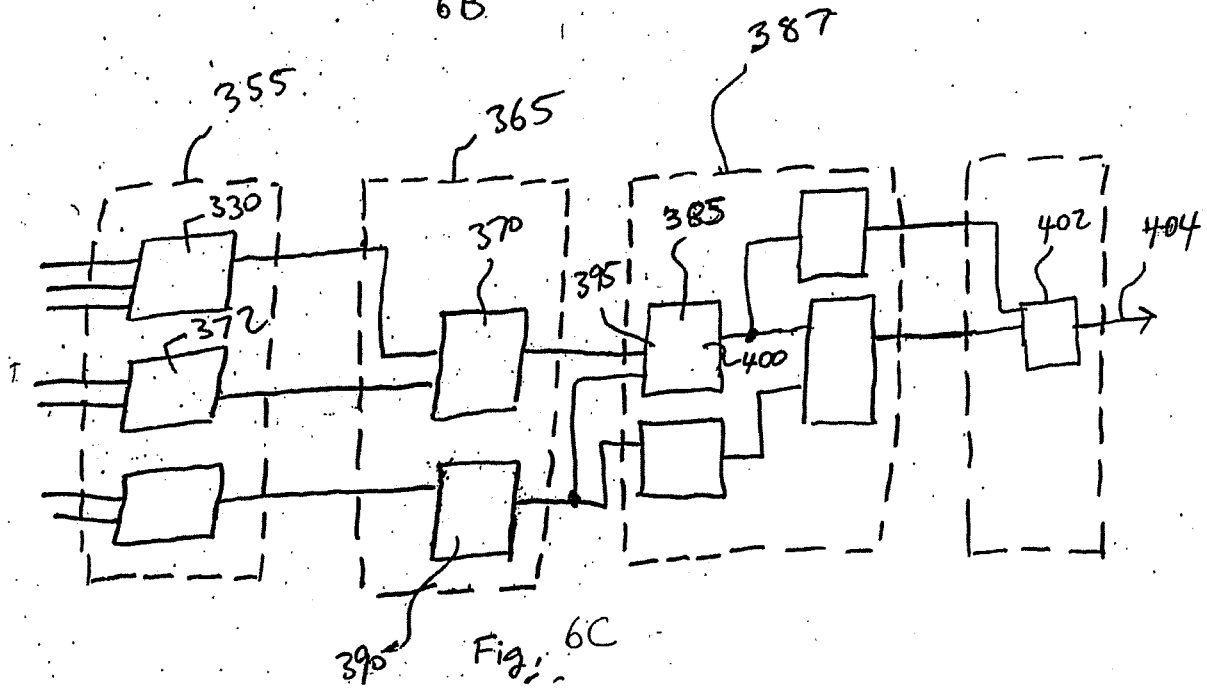


Fig. 6C

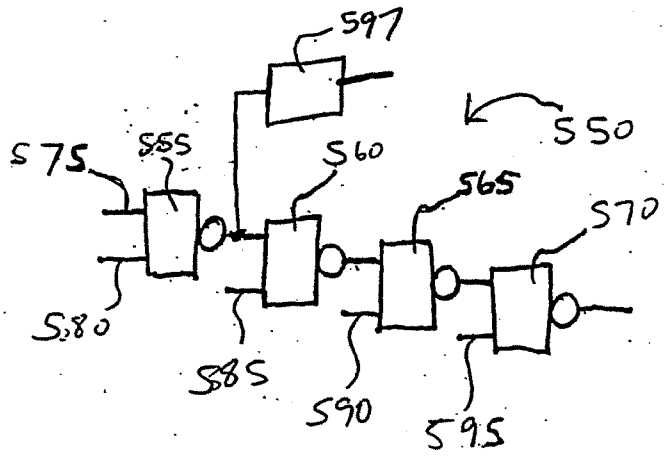
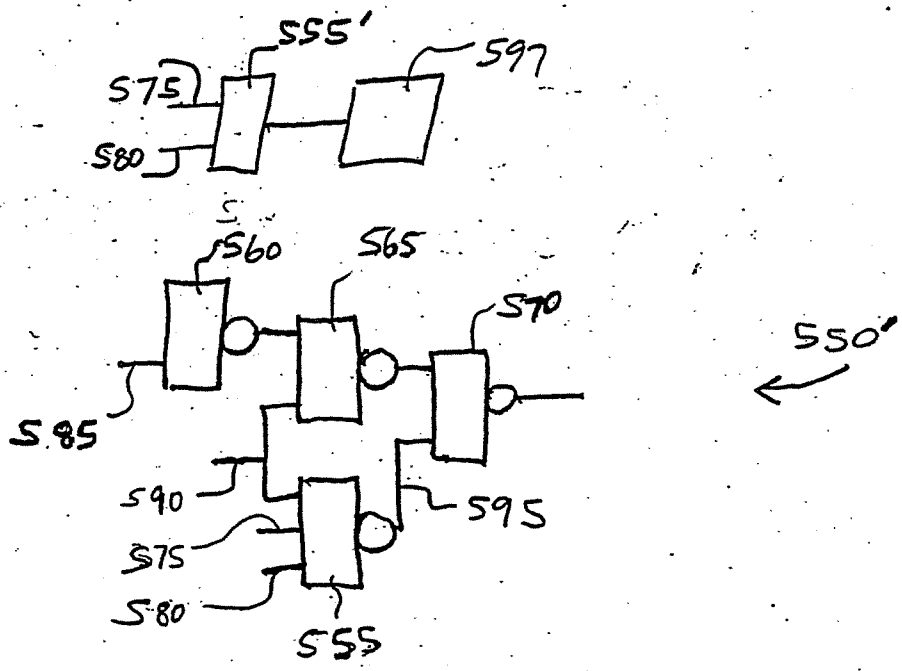

597
550
575
555
560
565
570
580
585
590
595

Fig. 7A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580
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565
570
550'
585
590
595
575
580
555

Fig. 7B

Buffering

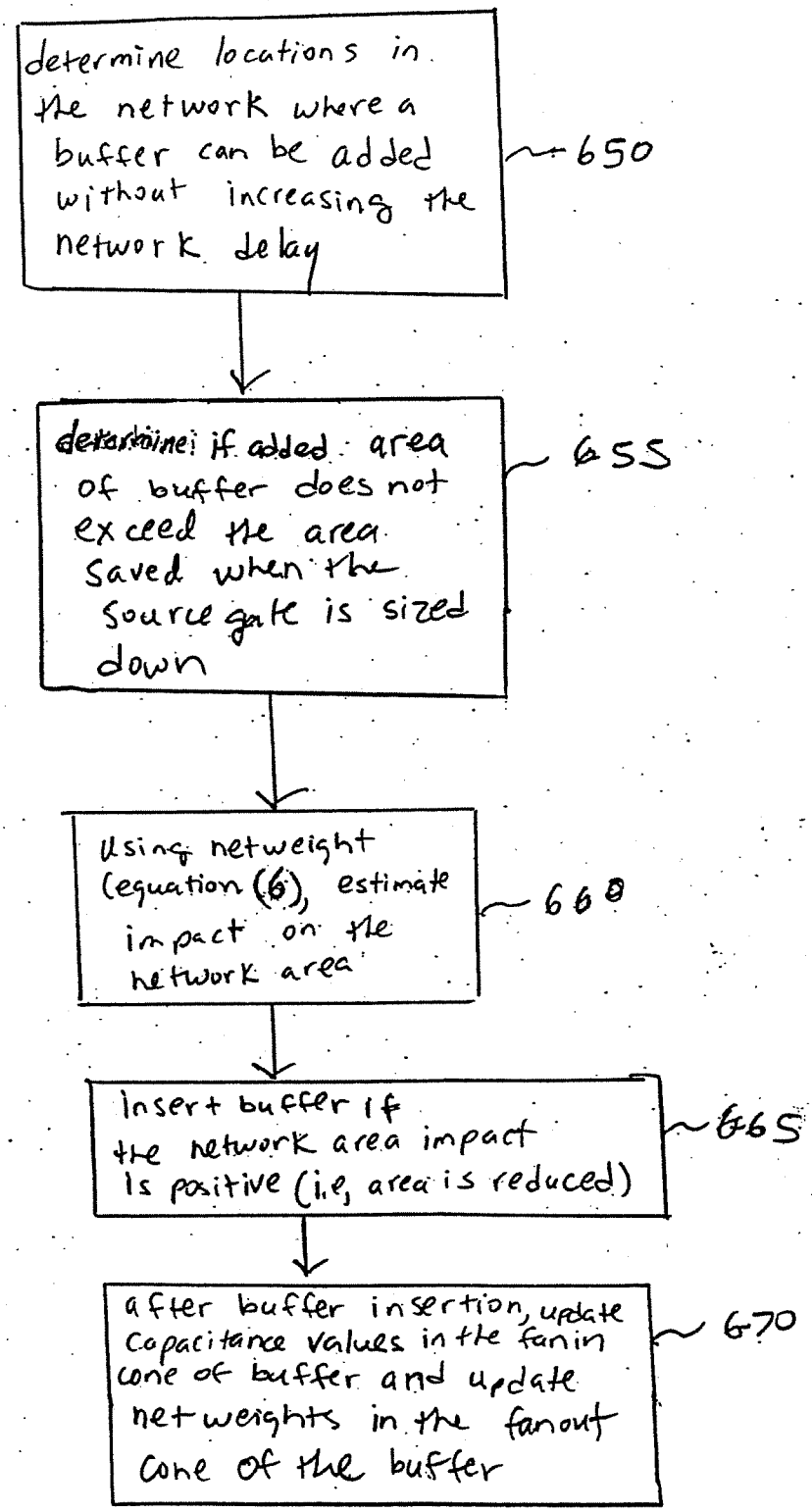

Fig. 8

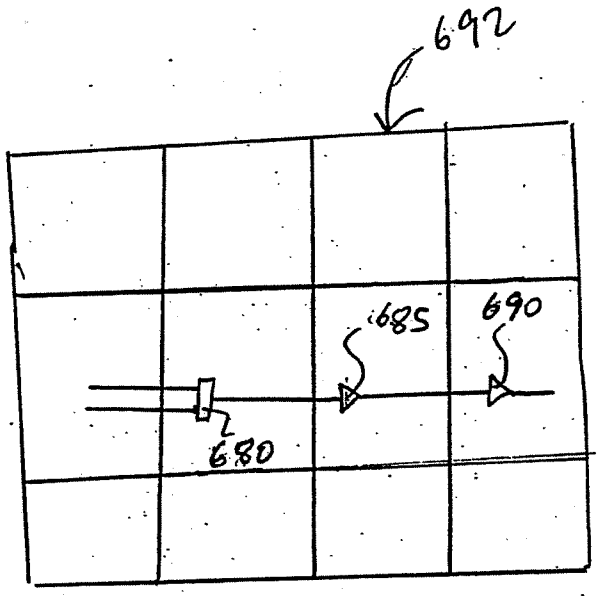

Fig. 8A

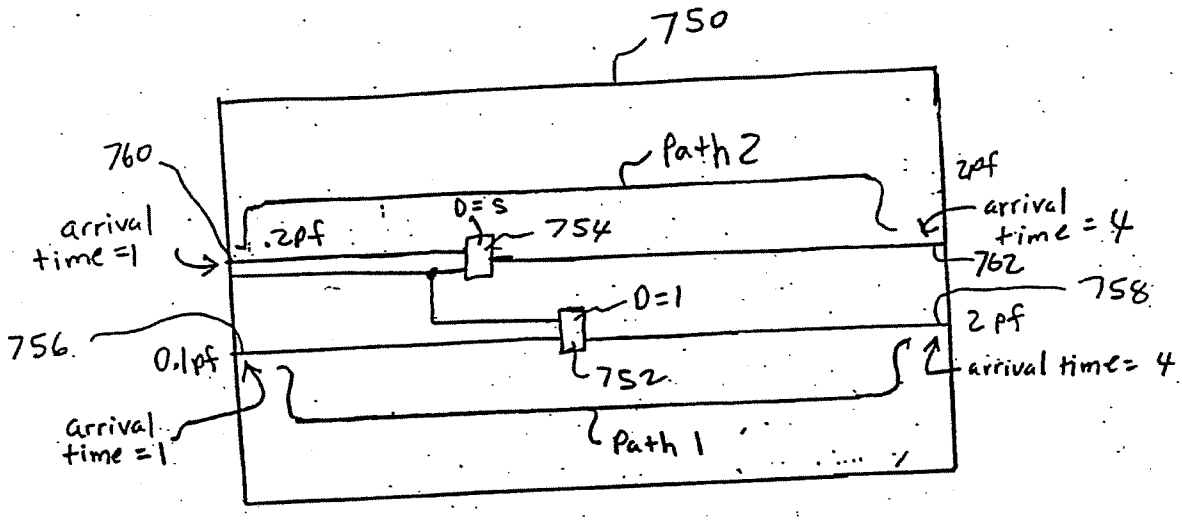
750
760
Path 2
2pf
arrival time = 4
arrival time = 1
.2pf
D=5
754
762
D=1
758
2 pf
756
0.1pf
752
arrival time = 4
arrival time = 1
Path 1

Fig. 9

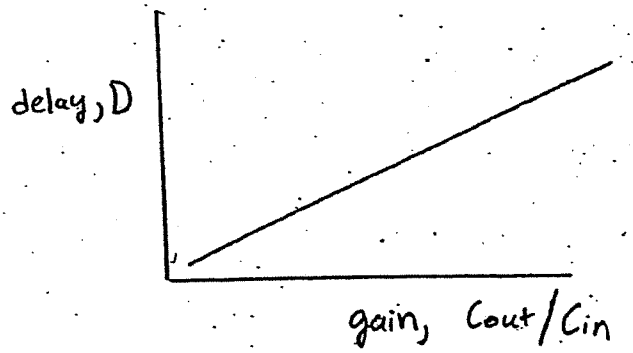
delay, D
gain, Cout/Cin

Fig. 9A

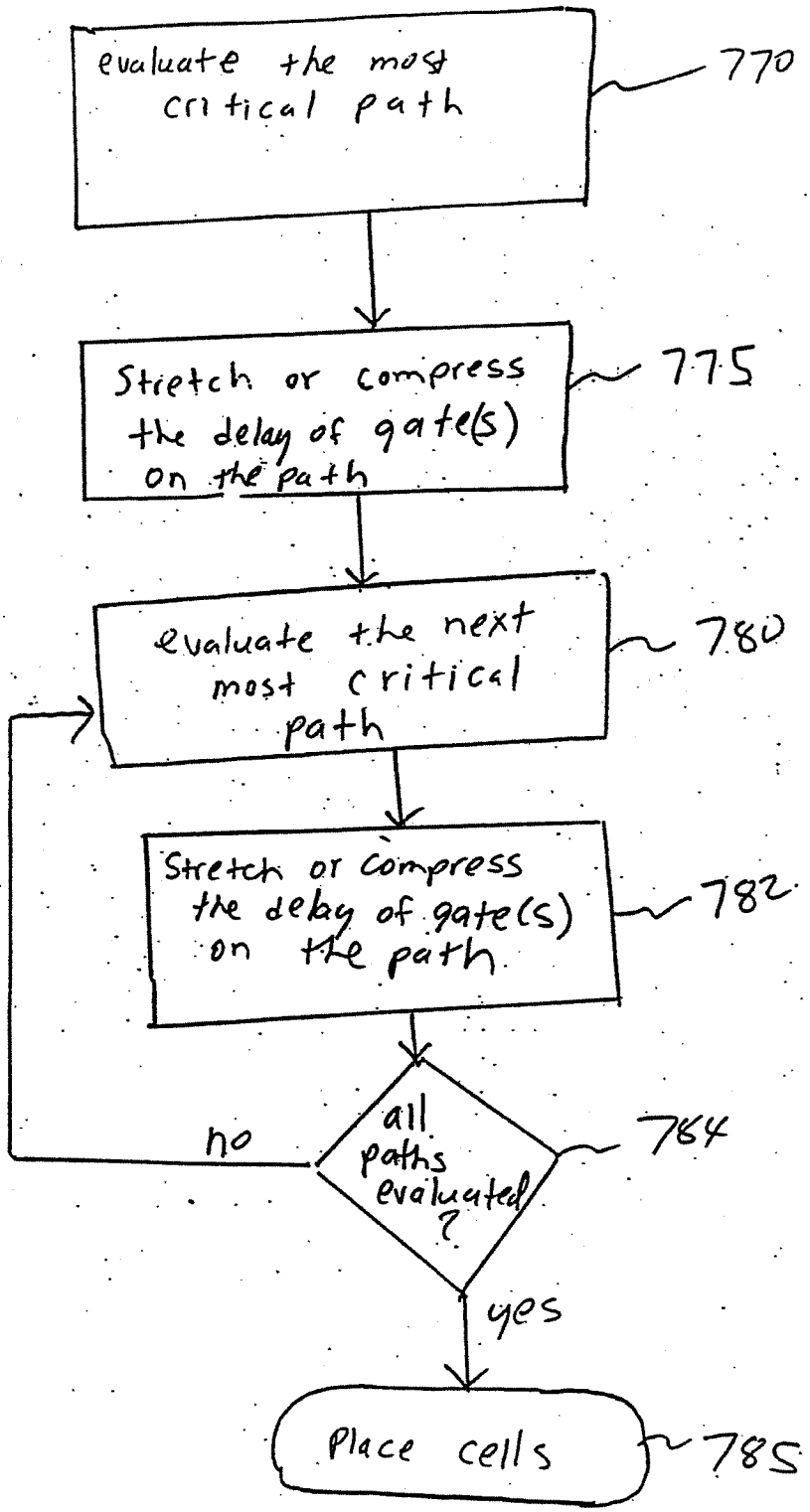
evaluate the most critical path
770
Stretch or compress the delay of gate(s) on the path
775
evaluate the next most critical path
780
Stretch or compress the delay of gate(s) on the path
782
all paths evaluated ?
764
no
yes
Place cells
785

Fig. 9B

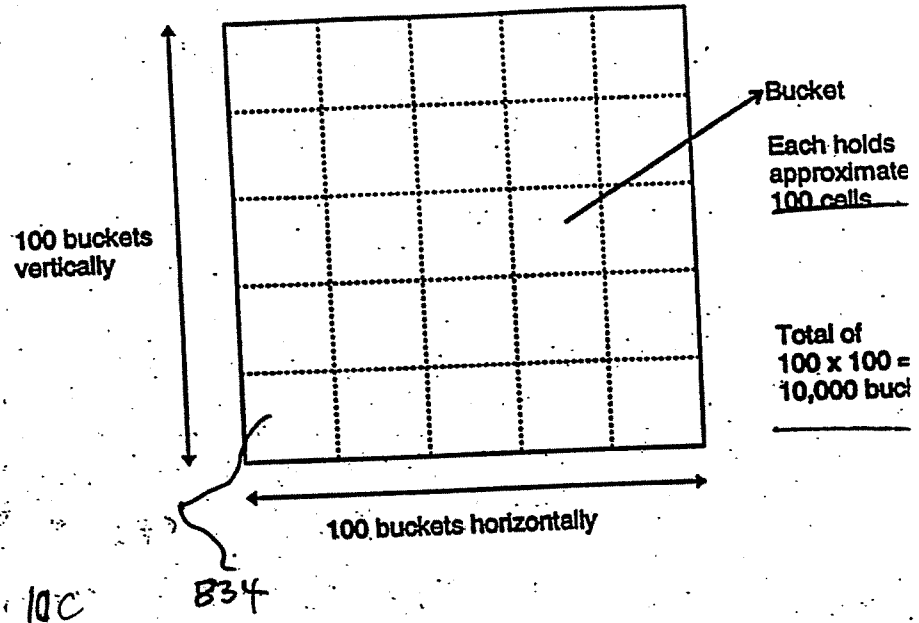

Fig. 10C

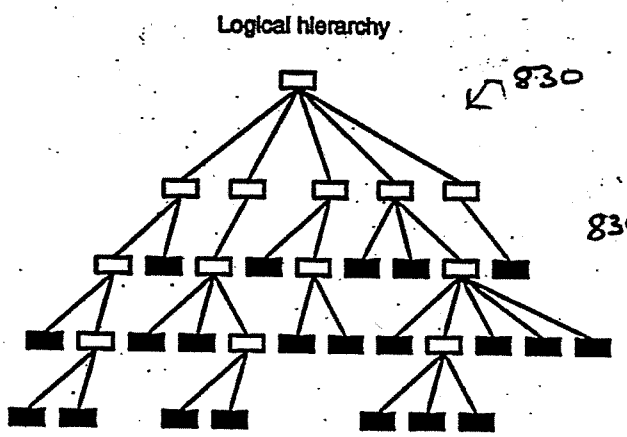

Fig. 10A

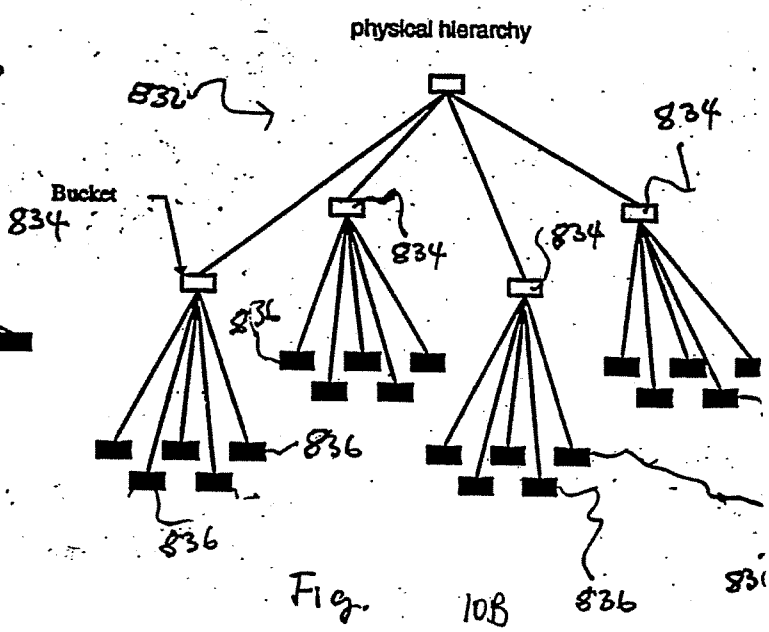

Fig. 10B

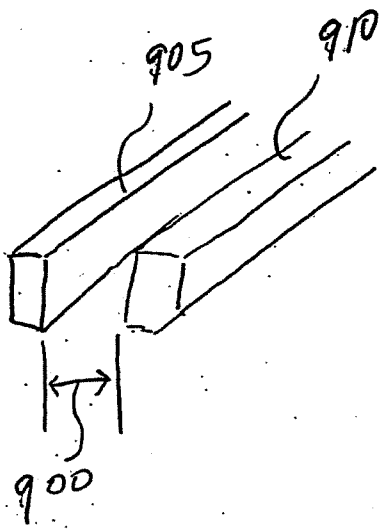

Fig. 11

CDC-103 11/95 PTO RECEIPT FOR INDICATED ITEMS

Appln. No: 0 /Unknown

Inventor(s) Lukas P.P.P. van Ginneken

Title: TIMING CLOSURE METHODOLOGY

Atty AMD/SV
Date 4/2/98
Client Magma
C# 54355
M# 238258

ENCLOSED:

_____ Amendment
1 No. of Pages Abstract
75 No. of Pages Spec and Claims
41 No. of numbered Claims only
14 No. Sheets Drawings (Fig(s) 1 to 11) [ ] 1 set Formal
_____ Declaration (___ #pgs) [X] 1 set Informal
_____ Assignment [ ] Cover Sheet
#_____ No. of Priority Documents
[ ] IDS including PTO-1449 [ ] cited docs. [ ] search rept.
_____ Issue Fee Transmittal Form PTOL-85(b)
$ 0 Fee (Check)
Other: Rule 53(f) Transmittal Letter (2 copies)
Express Mail No.: EL 020 115 594 US
/ Express Mail Certificate

CURRENT DUE DATE: _____

CDC-103 11/95 PTO RECEIPT FOR INDICATED ITEMS

Appln. No: 0 /Unknown

Inventor(s) Lukas P.P.P. van Ginneken

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