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Stability Analysis of CdTe/CdS cells under Illumination

by

Ashok Rangaswamy

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Approved, Thesis Committee:

Chris Ferekides ,Major Professor,
Associate Professor of Electrical
Engineering

Don Morel
Professor of Electrical Engineering

Y.L.Chiou
Professor of Electrical Engineering

Tampa, FL

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ABSTRACT

Stability Analysis of CdTe/CdS cells under Illumination

by

Ashok Rangaswamy

The CdTe solar cell is a leading candidate for cost-effective thin-film solar cells having demonstrated small area cell efficiencies of 16.4%. A Key issue associated with CdTe thin film photovoltaic modules is the analysis of degradation behavior of the device. The analysis is complicated as changes due to degradation may be reversible. Solar cell measurement techniques were used to understand the changes in device parameters after light soaking for 1000 hours. An automated measurement setup was implemented as part of this thesis work. The main objective of this thesis was to study the effect of $CdCl_2$ heat treatment on the device stability. The temperature for this heat treatment was varied from 360^oC to 400^oC. Cells were stressed under illumination at both short circuit and open circuit conditions. It was found that the increase $CdCl_2$ heat treatment temperature slowed down the degradation rate.This was true for both short and open circuit stress conditions. Also when the device was light soaked at short circuit condition,the degradation of the device was slowed down

considerably when compared with open circuit conditions. Also it became evident that the recombination current mainly got affected when the device was said to be degraded.

Chapter 1
Introduction:

The only reason for time is so that everything doesn't happen at once ...

Albert Einstein

The stability of solar cells acquires importance since it is generally assumed that terrestrial photovoltaic systems must have a useful life of at least 20 years. Thin film fabrication processes are being developed as low cost technique for producing terrestrial solar cells. Semiconductors with band gaps of around 1.5eV are optimum in terms of efficiency. Hence CdTe is the material of choice. Published data [1][2] show that CdTe/CdS solar cells may exhibit instability under certain conditions.

In general, degradation of solar cells occurs when they are light soaked for prolonged time and/or at elevated temperatures. The reasons for the observed degradation may be junction degradation, degradation of the electrical contact to CdTe and shunting. The degradation is frequently represented by perturbation of current voltage characteristics, the development of rollover at high forward bias, a decrease in open circuit voltage (Voc), an increase in the series resistance and a decrease in the fill factor (FF). The short circuit current (Isc) is generally less affected.

The most suspected cause for cell instability is the diffusion of Cu from the back contact into the CdTe region and the CdTe/CdS interface. A small amount of Cu

is often added to back contacts to effectively p^+ dope the CdTe surface and allow the formation of better ohmic contacts to CdTe[3][4]. At the cell junction Cu was proposed to form recombination centers and shunting pathways, limiting the lifetime of the cell.

Other probable degradation mechanisms in CdTe/CdS solar cells are oxidation, electromigration and diffusion of native and other impurities.

1.1 Objectives

The objectives of this work were:

- to Construct and automate a measurement setup needed for stability testing of CdTe/CdS solar cells under various stress conditions and
- to study the effect of prolonged illumination and $CdCl_2$ heat treatment on the performance of CdTe/CdS solar cells.

Chapter 2
Solar cells under Illumination

It is necessary to first understand the device behavior under illumination to know the effect of prolonged illumination on device stability.

A solar cell is generally a p-n diode. In our case, CdS was used as the n-type semiconductor and CdTe as the p-type semiconductor. The junction formed between CdS and CdTe is called heterojunction. If the light passes through the substrate first, then device is said to have a superstrate structure. CdTe solar cells for this experiment had the superstrate structure as shown in fig. 5.1. When the radiation is received from the sun, it gets absorbed in the semiconductors which generates charge carriers in them. The most of these carriers are separated by the junction due to its internal electrical field and then collected at the contacts of the device, thus delivering power to an external load connected to the solar cell.

The following regions of a solar cell are of interest to explain the electronic process involved:

1. The back contact to CdTe: can form barrier with CdTe, possibly increasing series resistance and roll over

2. The bulk of CdTe: where electron/hole pairs are generated by the absorption of light outside the depletion region and where the minority carriers (electrons)

are transported by diffusion and are partially lost by recombination

3. The heterojunction: where the change in interface states and high recombination takes place, increasing the dark current

4. The bulk of CdS, which contributes to series resistance, but does not contribute to Jsc.

The idealized junction current in the dark is given by

$$I = I_0[\exp[qV/AkT] - 1] \tag{2.1}$$

where I_0 is the reverse saturation current, k is the boltzman constant,q is electric charge,T is temperature in $^o kelvin$ and A is the diode factor.

Some heterojunction solar cell structures show a variation in Io and A with illumination level and wavelength. This is because, when trapping centers at or near junction are not in good thermal communication with conduction or valence bands (slow states), their occupancy and hence charge can be changed by illumination. Also the ionized donor or acceptor density in the n or p type semiconductor may change upon illumination, which in turn modifies the depletion layer width, the shape of the junction barrier, and finally the junction transport[7].

Under illumination, the equation 2.1 becomes

$$I = I_0[\exp[qV/AkT] - 1] - I_L \tag{2.2}$$

Where I_L is the light generated current determined by the processes in CdTe during illumination.

Equation 2.2 is valid only if the shunt (R_{sh}) and series (R_s) resistances of the solar cell approach ∞ and 0 respectively. In practical devices, this is not true. Equation 2.3 includes the effect of these resistances.

$$I = I_0[\exp[q(V - IR_s)/AkT] - 1] + [(V - IR_s)/R_{sh}] - I_L \tag{2.3}$$

Here the shunt resistance R_{sh} may account for the effects of the current paths provided by imperfections like pinholes, surface recombination, three dimensional imperfections in the junction etc. R_s is due to bulk resistances of layers present in the device,front and back contact resistances etc.

If the the device is kept open(i.e. no load),the potential difference across the front and back contacts is measured as the open-circuit voltage, V_{oc}. When the contacts are shorted with zero resistance load, the resultant photo generated current is known as short circuit current I_{sc}. J_{sc} is the corresponding current density. At a certain load, the output power is maximized(P_{max}). The ratio between P_{max} to the product of V_{oc} and J_{sc} is called the fill factor(FF) which is the measure of the "squareness" of the current-voltage characteristics under illumination.

R_{sh} affects the current-voltage characteristics in the low voltage region and R_s at high current region of current-voltage curve.

2.1 Interface States

Optical absorption by states at the interface and in the bulk material near the junction produces changes in the junction profile, and hence changes in Io and A upon illumination.

The interface states density N_{ss} affects the carrier transport. These surface states act as a recombination centers, which can provide a tunnelling path for the carriers[6].

The increase in interface states density due to illumination will lead to a decrease in the barrier height Φ_b and consequently enhance the saturation current. The consequences of the decrease in potential barrier height are an increase in both dark current and series resistance, and a decrease in open circuit voltage, photocurrent and conversion efficiency of the solar cell[6].

Chapter 3
Literature Review

It is important to understand the failure mechanisms that lead to cell degradation. Table 3.1 lists major failure modes in CdTe/CdS solar cells along with the possible causes.

Table 3.1 CdTe Failure Modes and Possible Causes[8]

Failure Modes	Possible Causes
Main junction, increased recombination	Diffusion of dopants, impurities etc., electromigration
Back barrier, loss of ohmic contact	Diffusion of dopants, impurities etc., electromigration
Shunting	Diffusion of metals, impurities etc.

These mechanisms can cause the following change in the current-voltage (I-V) characteristics:

- an increase in Roc and "Rollover" in I-V curves at voltages larger than Voc, possibly from the back contact barrier formation,
- a reduction in Voc and

- an increase in the slope of I-V curve, through Jsc, possibly from increased shunting or from increased recombination in the space charge region[9].

Roc is the slope of light I-V curve at Voc. It is found that the formation of back contact barrier leads to high values of Roc and “Rollover”. A high series resistance can also lead to an increase in Roc.

A Non ohmic back junction can be due to[10]

- loss in acceptor density in the p^+ layer and

- Oxide interface layer.

A loss in acceptor density is mainly caused by diffusion of impurities. Here, Cu with diffusion coefficient of 5E-14 cm^2/sec at 100^oC and activation energy of 0.66 eV is a prime suspect. The degradation also depends on bias, as the charge state of vacancies can affect the rate of diffusion of an atom. Also, grain boundaries have some effect on diffusion, electromigration of charged atoms, and local compensation effects in degradation[10].

3.1 Effect of Copper Diffusion on device Stability

Even though Cu forms better ohmic contact at the back contact interface, it can degrade the cell, by diffusing through the CdTe layer to the junction and CdS, as Cu is the fast diffuser in single crystal CdTe(Diffusion Coefficient $D \sim 3E - 12cm^2$). Cu as an interstitial ion $[Cu_i^+]$ gives shallow donor state or substitutes Cd atom to form

a deep acceptor state in single crystal CdTe. In polycrystalline films, the diffusion of Copper is even more as the surface bonds are weaker and two surfaces are available at grain boundaries.Electric field may also enhance Cu diffusion. "Roll over" after light soaking indicates the decrease in Cu density near the back contact and possible increase of Cu density near the junction[10]. When cells with and without Cu in in the carbon back contact was light soaked, only cells with Cu showed some recovery after rested in dark for 6-12 months. This suggests that Cu can return to the CdTe/back contact interface under some circumstances[10].Also when the Cu content in the back contact was increased, Voc and FF degraded faster[10].

One possible mechanism which drives the Cu into junction and CdS may be grain boundary diffusion and surface reaction to form Cu-S bonds. This process would be aided by S/Te interdiffusion and also due to the fact that Cu-S bond is stronger than Cu-Te bond as derived from the heats of formation[10].It is to be noted here that the interdiffused CdS_xTe_{1-x} region adjacent to the CdS acquires a low concentration of Cu compared to the less Te-rich CdS[10].

While the built in voltage slows the concentration gradient driven Cu diffusion, forward bias and/or light lowers that barrier for diffusion[11].

3.2 Effect of $CdCl_2$ Treatment on Device Stability

After $CdCl_2$ treatment, Cl moves via grain boundary (GB) diffusion through the CdTe layer. The accumulation of Cl near the CdS interface is due to the greater GB

area in the smaller-grain CdS layer compared to the CdTe. This is also due to the fact that Cl of atomic radius 167 pm is expected to substitute for S(170 pm) in CdS over Te(207 pm) in CdTe[2].This accumulation improves the initial performance. The net acceptor concentration near the interface increases by increasing the temperature of $CdCl_2$ heat treatment[2].

Also structural changes in CdTe thin films occur only when $CdCl_2$ is present due to recrystallization and subsequent grain growth. Recrystallization is the function of lattice-strain energy, and initial strain energy increases due to Cl diffusion[12].

It has been shown that during vapor $CdCl_2$ treatment diffusion of CdS into the absorber layer proceeds faster than the diffusion of CdTe into window layer and is enhanced by reaction temperature[14].

Chapter 4
Solar Cell Characteristics and Characterization Techniques

4.1 Current-Voltage Characteristics

4.1.1 Current-Voltage Characteristics in Dark

Under thermal equlibrium, when the diode is zero biased or reverse biased, no current flows due to the potential barrier. When it is forward biased, barrier potential is reduced, holes(or electrons) from the p(or n) region are injected to create excess minority carrier in (n or p) region.

In low injection, the majority carrier concentration doesnt change significantly. But minority carriers change several orders of magnitude.The total current in the junction is the sum of the individual electron and hole currents. Since the electron and hole currents are continuous functions through the junction, the total pn current will be sum of minority carrier diffusion currents. Since it is assumed that the electric field at space charge edges is zero, there is no minority drift current.

So for ideal p-n junction diode,current density equation in dark is,

$$J = J_s[\exp \frac{qV}{kT} - 1] \tag{4.1}$$

where

$$J_s = qn_i^2[\frac{1}{N_a}\sqrt{\frac{D_n}{\tau_{n0}}} + \frac{1}{N_d}\sqrt{\frac{D_p}{\tau_{p0}}}] \tag{4.2}$$

Here J_s is called ideal reverse saturation current density.

But this ideal diode equation neglects any effects occurring within the space charge region. Since other current components are generated within space charge region, the actual I-V characteristics deviate from the ideal one.These additional currents are generated from the recombination processes. Under reverse bias,since number of electrons or holes are said to be zero in the space charge region as they are swept away,electrons and holes are generated to reestablish thermal equilibrium.This reverse bias generation current should be added to get the total reverse saturation current.It is given by,

$$J_0 = J_s + J_{r0} \tag{4.3}$$

Where J_0 and J_s are total and ideal reverse saturation current densities. J_{r0} is the reverse generation current in the space charge region and is given by,

$$J_{r0} = \frac{qn_iW}{2\tau_O} \tag{4.4}$$

Where W is the depletion width and τ_O the average carrier life time.

Under forward bias, some excess carriers are injected into the space charge region. Recombination current density is then,

$$J_{rec} = J_{r0}\exp[\frac{qV}{2kT}] \tag{4.5}$$

Hence in general, the diode equation becomes

$$J = J_0[\exp\frac{qV}{AkT} - 1] \tag{4.6}$$

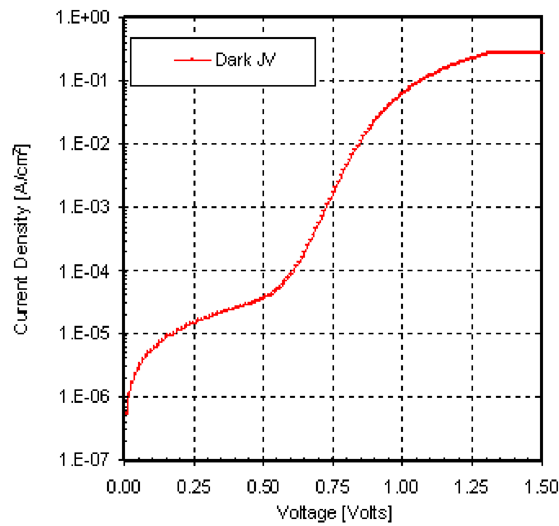

Figure 4.1 Typical dark JV characteristics

where A is the diode factor. For a large forward bias voltage, A≈1 when diffusion dominates and for a low forward bias voltage,A≈2 when recombination dominates. There is a transition region where $1 < A < 2$.

The typical dark JV characteristics is shown in fig.4.1. The dark JV characteristics bend over at high current region due to series resistance[21].

4.1.2 Current Voltage Characteristics Under Illumination

The simplest model for a solar cell is a diode in parallel with a voltage independent current source.For an ideal cell, the I-V curve is just shifted along the current axis as the device is illuminated.This implies that light and dark characteristics will not cross,and also that dI/dV for any voltage remains unchanged with illumination.

But in real devices, there is a cross-over of dark and light J-V characteristics. Such cross-over relates to change in diode parameters with illumination; the light may cause a lowering of the junction barrier. Also there is change in dI/dV at small reverse bias as the light intensity increases.Since conduction is negligible at this bias, the change in slope must be a result of a voltage dependent current source. The cross over can be explained by the collection function g(V), the factor that includes the bias dependance of light generated current. This effect is included to J as,

$$J = J_0(exp(\frac{qV}{AkT}) - 1) - g(V)J_L^{\Delta} \tag{4.7}$$

where g(V) is the collection function and J_L^{Δ} is the voltage independent light generated current.

Since both the current transport and junction barrier may be sensitive to light, the diode factor A often takes on different values as the illumination intensity and wavelength is varied. Light saturation current J_{OL} is related to dark saturation current J_0 as,

$$J_{OL} = \frac{g(0)}{g(Voc)}J_0 \tag{4.8}$$

J_{OL} is slightly higher than J_0 due to collection function. There is also the change in junction barrier when cells are light soaked[17].

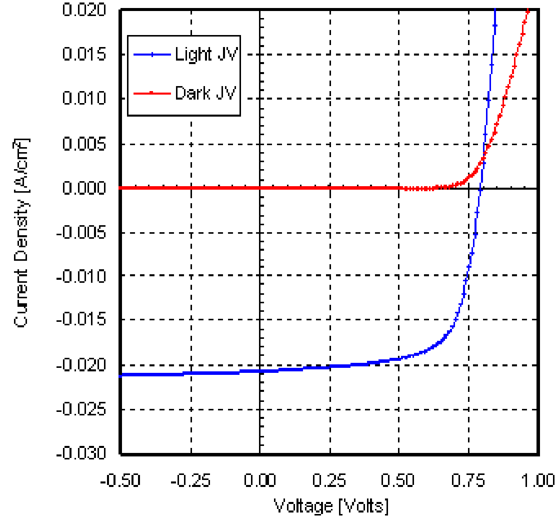

Figure 4.2 Cross over in IV curves

4.1.3 Roll Over in IV Curves Due to Back Contact Barrier

The roll over of IV curves occurs because the junction voltage saturates at high bias.This saturation occurs because of a back contact barrier. The saturation voltages for roll over under dark and illumination are given by[18],

$$V_{sdark} \simeq \frac{nkT}{q} \ln \frac{J_c}{J_s} \tag{4.9}$$

and

$$V_{slight} \simeq V_{sdark} + \frac{nkT}{q} \ln[1 + \frac{J_c}{J_s}] \tag{4.10}$$

respectively.Where J_c is the contact saturation current density and J_0 is the total reverse saturation current density.

4.1.4 Dynamic Resistance

The derivative dV/dJ is used to understand light and dark JV characteristics more clearly. Due to the non linearity of the physical phenomenon of the solar cell, the current voltage characteristics is non ohmic. This behavior is shown in the plot of the derivative dV/dJ with respect to voltage. The minimum resistance corresponding to a chosen value of high forward current(say 0.08 A/cm^2) can be taken as Rs, though this quantity doesn't reflect the real value of seies resistance of the device[20]. However this quantitity is useful to the extent, can represent the degradation of the device quantitatively.

The shunt resistance R_{sh} can be approximated by the slope of the current voltage characteristics in the low voltage region (say, -1.7V to -1 V).

4.1.5 Fill Factor Loss Due to Back Contact Barrier

The non-ideal FF is given by[18],

$$FF \approx FF_o(V_{oc}^1)[1 - \frac{kT}{qV_{oc}} \ln[1 + \frac{J_L}{J_c}]] \tag{4.11}$$

where,

$$FF_o(V_{oc}^1) \approx [1 - \frac{\ln V_{oc}^1}{V_{oc}^1}][1 - \frac{1}{V_{oc}^1}][\frac{1}{1 - \exp(-V_{oc}^1)}]$$

and

$$V_{oc}^1 = \frac{q(V_{oc} - \Delta V)}{nkT}.$$

Where ΔV is the forward bias at the back contact when light current flows under reverse bias. When the back contact diode saturation current J_c is larger than or equal to the light current, the FF loss due to the back contact is only a few percent. In contrast, considerable FF losses occur, if J_c is considerably smaller than J_L.

4.2 Spectral Response

There are a variety of possible optical losses before photons reach a solar cell's absorber, and there are additional losses from non radiative recombination or from photons exciting the absorber. Figure 4.3 is one example of the fraction of photons of each wavelength that contributed to photocurrent and the fractions that are lost in each of several ways. The loss includes the reflection from the cell, the absorption of the glass substrate,the absorption of the SnO_2 contact,and the absorption of the CdS window layer. Some photons are lost due to deep penetration at CdTe region.

4.3 CV Measurement

Information like doping profile, depletion width,acceptor concentration and barrier height of the junction Φ_b can be obtained from Capacitance-Voltage (CV) characteristics.

As the CdS film has carrier concentration (approximately 1E+16 to 1E+17 electrons / cm^2) several orders of magnitude higher than that of CdTe (approximately 1E+13 to 1E+15 holes/cm^2), the depletion layer mainly spreads into the CdTe ab-

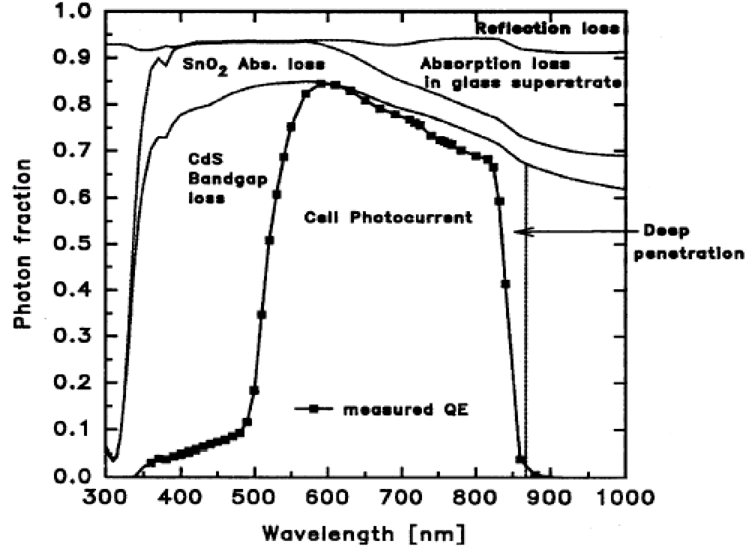

Figure 4.3 Photon Accounting for a CdTe Solar Cell [19]

sorber layer to separate the photo-generated carriers. Hence only the permittivity of CdTe layer is used to calculate the depletion layer width(W_d). This width changes as the external bias V is applied across the contacts of the solar cell. The depletion layer width(W_d) at particular bias V is calculated using

$$W_d = \frac{\epsilon_o \epsilon_r}{C/A} \tag{4.12}$$

Where ϵ_o is permittivity of free space(8.854E-14F/cm),ϵ_r is relative permittivity of CdTe layer(10.2), C is the capacitance(F) at that bias V and A is the effective contact area of the device.

The net acceptor concentration is then found from

$$N_A = \frac{2}{[q\epsilon_o\epsilon_r][d[C^2/A^2]/dV]} \tag{4.13}$$

where q is electic charge,1.6022E-19 Coulombs.

The accuracy of predicting real values using equations 4.12 and 4.13 may be affected due to following reasons:

- The equation 4.13 is valid only for homogeneously doped uncompensated p-type CdTe. For partially compensated CdTe layer, the value equals $N_A - N_D$ as $N_A > N_D$.

- The equations completely neglect minority carriers and assume total depletion of majority carriers in the space charge region[SCR].This is valid only when the SCR is reverse biased and substrate is uniformly doped.

- Also these equations are based on a single junction model.But CdTe/CdS has separate capacitance components for the main junction as well as the junction due to back contact schottky diode.This two diode circuit also affects the accuracy of values.

Though these sources of errors affect the real device parameter values, a relative comparison of the device parameter values may be valid in general.

Chapter 5
Experimental

5.1 Device Structure

The device used for this study had the superstrate structure (that is light enters through substrate first, which is 7059 Boro silicate glass) as shown in the fig.5.1.

The deposition procedures are described in detail elsewhere [22]. In brief, the front contact SnO_2 was deposited by the MOCVD [Metal Organic Chemical Vapor Deposition] technique and was deposited as $low - \rho/high - \rho$ bilayer. The sheet resistance of SnO_2 was below $10\Omega/\Box$. Cadmium sulfide of approximately $1000\mathring{A}$ was deposited using Chemical bath deposition(CBD) method. The CdTe deposition was carried out by Closed space sublimation(CSS) method at $550 - 600^oC$ as substrate temperature. The CdTe/CdS structure was then heat treated in the presence of $CdCl_2$.

The main objective of this thesis work was to analyze the the effect of $CdCl_2$ heat treatment on device stability. For this, the $CdCl_2$ annealing temperature was varied from 360 to 400^oC.

Excess $CdCl_2$ was then removed by etching the samples in methanol/bromine solution for 8 seconds which results in smooth Te rich surface for contacting. Cu doped graphite paste or sputtered Cu_2Te was applied as back contact and heat treated at 270^oC for 25 minutes in vacuum.

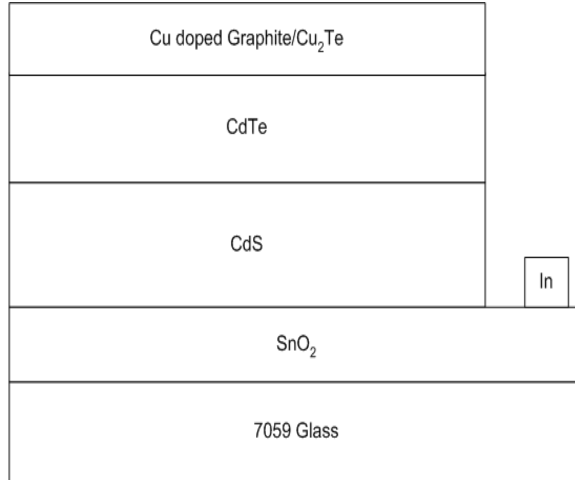

Figure 5.1 Device Structure

5.2 Measurement Setup

The measurement setup shown in fig.5.3 consists of a vacuum chamber which can be evacuated and back filled with ultra high purity N_2 gas prior to the beginning of light soaking. All devices under test were fabricated under identical conditions except the annealing temperature of the $CdCl_2$ treatment. Eight identical cells for each annealing temperature were stressed under one sun(AM1.5) illumination intensity(4 at short circuit and 4 at open circuit conditions).

The cells were placed on the copper plate sample bed as shown in fig.5.2.The samples were placed in such a way that the front contact(glass side) facing the light and back contact was in contact with a thin foil. The heat is transferred from the devices to cooling water with the help of high thermal conductivity thermal compound.

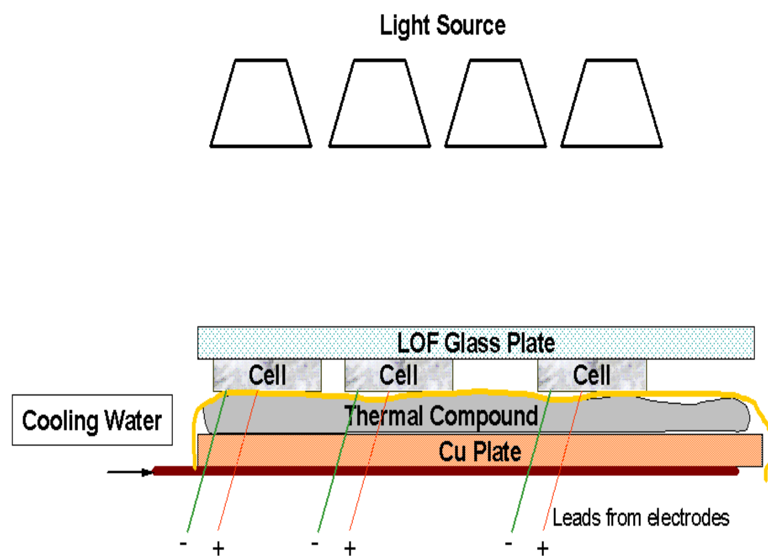

Figure 5.2 Sample Bed

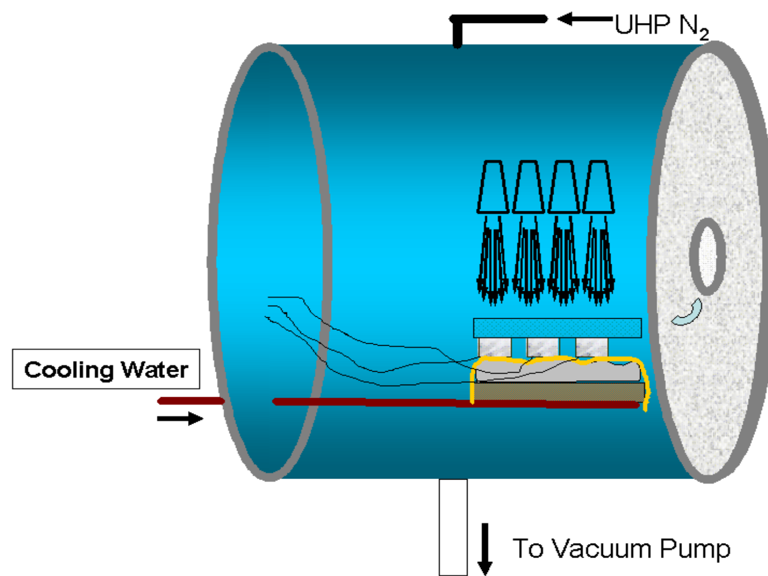

Figure 5.3 Measurement Setup

The light intensity is calibrated to approximately AM1.5 conditions($\pm15\%$). Samples were under continuous light stress and N_2 ambient during the measurement.The samples were kept at dark and light cycle of 4 hours each.The temperature of the copper plate sample bed was controlled using water circulation.

The light source was made using GE 12V,71 W 25° Beam MR16 lamps. Two sets of 10 lamps each were used to illuminate the samples in the front and back row of the sample bed.

The sample leads are connected to the Keithley Source Meter via low resistance copper electrical wires. The leads are attached to the front and back contacts (which is silver and indium respectively) using conductive silver epoxy. A brief heat treatment of 5 minutes is given to the samples at 100^oC for good adhesion. The samples are kept at vacuum desiccator before light soaking to avoid possible degradation caused by humidity. A clean soda lime glass is used to press the samples to the sample bed for better heat transfer. The light is diffused uniformly throughout the sample bed using quartz plates.

The temperature is continuously monitored and controlled using thermocouples and Euro Therm Controllers which control the water flow. The system was automated during this work and the details are given in the appendix.

Routine current-voltage(IV) measurements were done when the samples were being stressed inside the oven. A Keithley 2400 source meter is used for both Voltage

sweep and current measurement. The voltage sweep was from -2V to +2V with steps of 0.01V.

It should be mentioned that the following events could have an impact on the JV results presented in this thesis.

1. The lamps failed 6-7 times during light soaking which introduced extended dark period and in turn could lead to unpredictable recovery in JV parameters of some cells.

2. There was a water leak inside the chamber after 200 light soaked hours, though the cells did not get wet.

Capacitance-Voltage(CV) and Capacitance-frequency(CF) measurements were done using HP impedance analyzer 4145A. Spectral analysis for desired bandwidth of wavelengths of photons was done using Oriel Cornerstone monochromator (model 74100) with light source of GE 400W/120V quartz line lamp (model 43707). Silicon reference was used to adjust the light intensity prior to measurement.

Chapter 6
Results and Discussions

6.1 Effect of $CdCl_2$ Heat Treatment

The samples were prepared as described in section 5.2. Only the temperature of $CdCl_2$ heat treatment was varied between 360^oC to 400^oC. The dependance of the device parameters on the the $CdCl_2$ treatment was given in 6.1. Open circuit voltage (V_{oc}) was in the range of 800-850 mV for different annealing temperatures. The fill factor (FF) had a maximum for the cells annealed at 390^oc after $CdCl_2$ treatment. The deviation in FF was also more when the temperature was increased. The results were in close match with that of Okamato et.al[23].

Samples were then light soaked under the conditions specified in section 5.2. For this light soaking, eight cells were selected for each annealing temperature.Four of them were stressed at Open circuit(OC) and four at short circuit (SC) conditions. It should be mentioned that the maximum operating temperature during the light soaking period could be 55^oC ($\pm 10^oC$) (refer fig.6.2) depending on the location on the sample bed.

6.1.1 Effect of Light Soaking on Voc and FF

Figure 6.3 shows the degradation of Voc and FF for samples annealed at 360^oC and light soaked at OC. The initial huge difference in Voc was due to the elevated operating

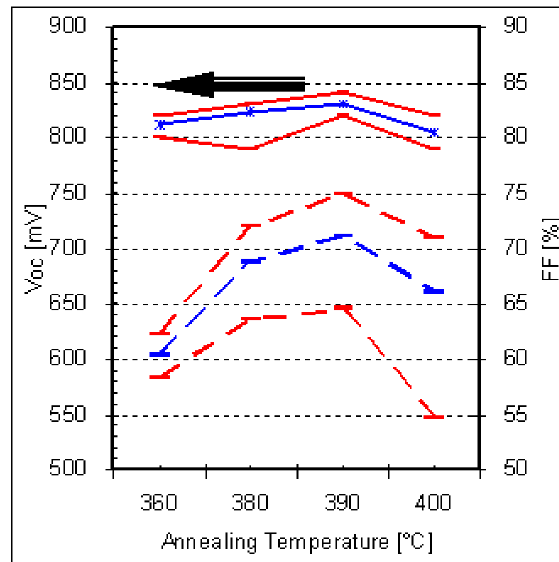

Figure 6.1 Effect of $CdCl_2$ Heat Treatment on Device Parameters

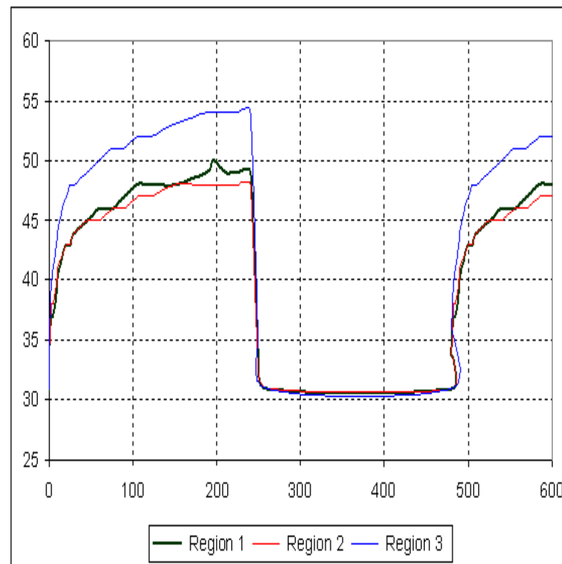

Figure 6.2 Temperature Profile Inside the Chamber During Stress Period. One Dark and Light Cycle Period is Shown(Temperature(^oC) Vs Time(min)). The variation is due to the temperature at various light intensity regions on the sample bed

temperature55^oC ($\pm 10^oC$) when compared to the the room temperature at which initial measurements were taken.Excluding this effect, Voc was increased initially (upto 10 hours of light soaking) and stayed constant essentially thereafter for 360^oC samples stressed at OC. Near 1000 hours of light soaking, Voc started dropping.FF was nearly constant upto 100 hours of light soaking and decreased thereafter almost linearly. The measurements at room temperature (at AM1.5 simulator after taking the samples out from the stability oven) were also given for comparison.

Figure 6.4 shows the degradation of Voc and FF for samples annealed at 360^oC and light soaked at SC. There was nearly no difference in degradation of Voc when compared to OC stress condition. Where as FF was nearly unchanged upto 300 hours of light soaking, and decreased thereafter.Sample 5-20B-1 showed the deviation from this behavior. It can be speculated that the devices were not identical as assumed. As the operating temperature was higher, Voc measured during 4th hour of light soaking was always lower than that of 1st hour.

Figures 6.5 shows the degradation for samples annealed at 400^oC and light soaked at OC.Change in Voc was essentially the same when compared to 360^oC samples. But FF was improved and stayed unchanged upto 400 hours of light soaking and dropped thereafter. Thus it became clearly evident that the increase in the temperature of $CdCl_2$ treatment essentially slowed down the degradation of device.

Figure 6.6 shows the degradation of Voc and FF for samples annealed at 360^oC

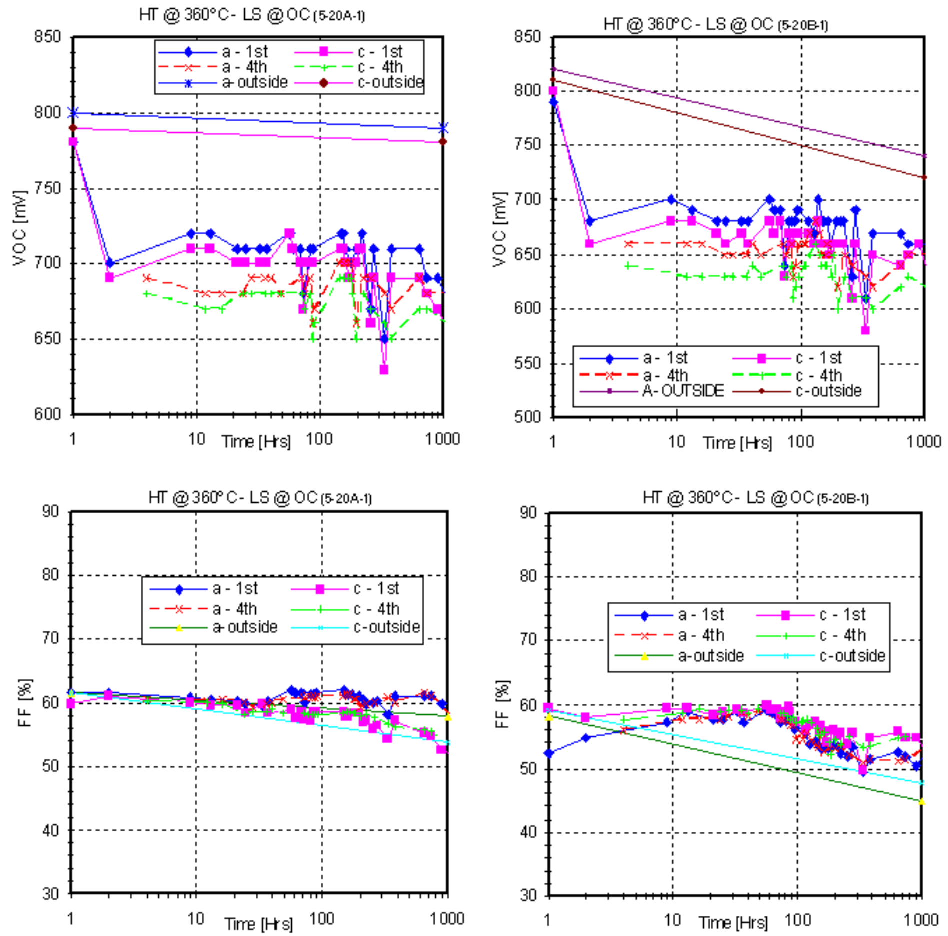

Figure 6.3 Degradation Behavior of Devices Heat Treated(HT) at 360^oC and Light Soaked(LS) @O.C

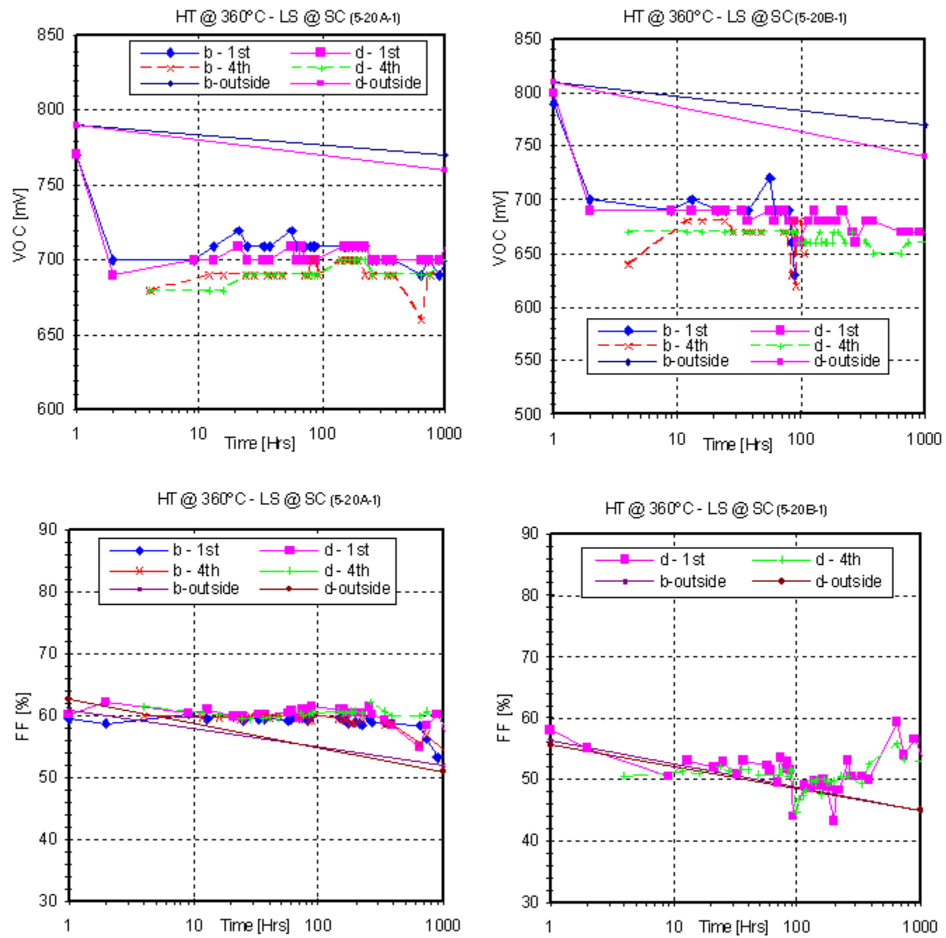

Figure 6.4 Degradation Behavior of Devices HT at 360°C and LS @Short Circuit (S.C) Condition

and light soaked at SC. There was essentially no change in Voc. Whereas FF was decreased initially and stayed constant thereafter upto 400 hours of light soaking. Then it started decreasing again.

The change in Voc and FF for samples with successive annealing temperatures 380^oC and 390^oC during light soaking period was shown in the appendix.Poor contact of sample 5-13B-1 resulted in loss of data.The degradation rate was minimum for this optimum annealing temperatures of 380 and 390^oC.

To summarize, the change in the $CdCl_2$ heat treatment or stress condition essentially did not affect the change in Voc during light soaking. Whereas the increase in the temperature of $CdCl_2$ heat treatment slowed down the drop in FF. Also when the device was stressed at SC, the drop in FF was delayed when compared to the samples at OC.Also the devices annealed at the operating temperatures of 380^oC and 390^oC gave the better performance during light soaking. The effect of the stress condition on the device stability disappeared, as the $CdCl_2$ annealing temperature was increased.

6.1.2 Effect of Micro Defects

Micro defects such as pinholes had the great impact on the performance in the device as shown in table 6.1. The device was light soaked for 1000 hours and measured in standard sun simulator before and after breaking the device into halves. This shows that the observed catastrophic behavior could not be always related to the specific degradation mechanisms, as these micro defects may have considerable effect too.

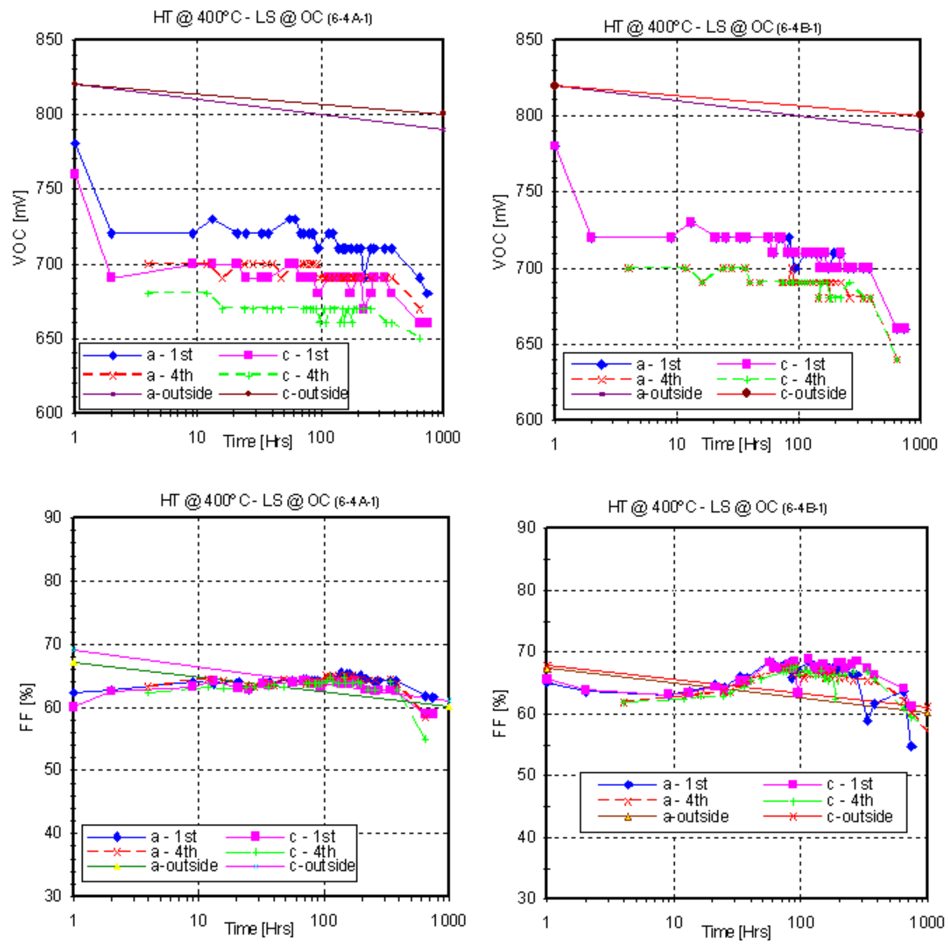

Figure 6.5 Degradation Behavior: HT @ 400^oC and LS @O.C

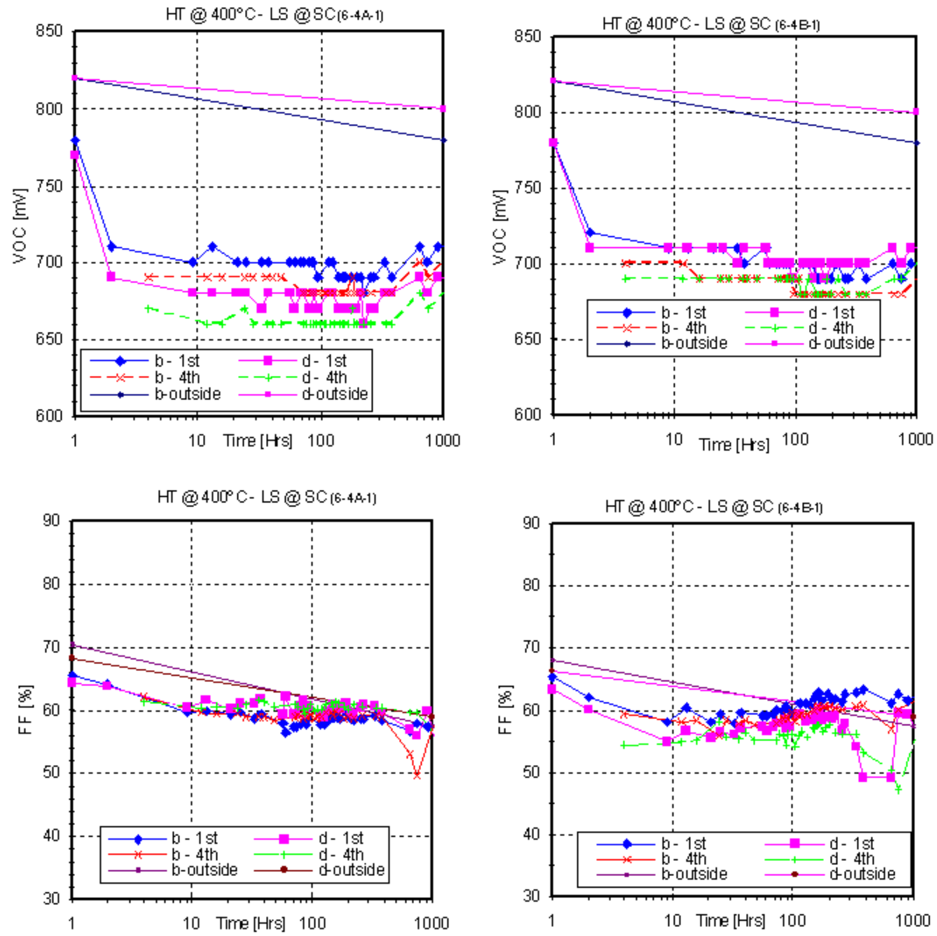

Figure 6.6 Degradation Behavior: HT @ 400^oC and LS @S.C

Table 6.1 Effect of Micro Defects on Results

Device	Voc(mV)	FF(%)
Device as whole	270	29
First half	810	64
Second half	160	28

6.1.3 Recombination Current

The increase in current at small voltages (below 0.5 V) for dark JV curves can be identified as either "shunting" or increase in recombination currents. As the samples shows no shunting in the reverse bias (of light or dark JV curves), the increase is only attributed to increase in recombination currents. The change in this current indicates change in trap levels in the interface region.

For samples annealed at 360^oC and light soaked @ OC, the major changed in recombination current occurred initially within 100 hours of light soaking (refer fig.).Whereas,the SC stress condition limited the change in recombination current initially, though changes after 1000 hours of light soaking were same(refer fig.).The cells shown were from the same substrate(5-20A-1) for both SC and OC stress conditions. When the temperature of $CdCl_2$ treatment was increased to 380^oC there was no change even after 100 hours of light soaking. After 750 hours of light soaking, there was a major change in the recombination current region. Still these changes were low

compared with the 360^oC samples at OC. In case of short circuit condition, there was no change even after 1000 hours of light soaking. This implied that the device annealed at optimum temperature gave good performance during light soaking.

For samples annealed at 400^oC(shown in figures 6.10 and 6.11), the recombination current was changed after 100 hours of light soaking at OC similar to 360^oC case, though changes were less compared to that of the 360^oC samples. In this case also, S.C stress condition provided good control over recombination current change.

To summarize, the changes in recombination current were rapid if the $CdCl_2$ heat treatment was at low temperature. Also, the devices annealed annealed at optimum temperature had better control over recombination current control mechanism(i.e, the changes were minimum). The SC stress condition slowed down the change in the recombination current compared with OC.

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6.1.4 Summary

The change in Voc and FF under OC and SC stress conditions are summarized in fig.6.12 by averaging similar devices under same stress conditions.the change in the $CdCl_2$ heat treatment or stress condition essentially did not affect the change in Voc during light soaking. Whereas the increase in the temperature of $CdCl_2$ heat treatment slowed down the drop in FF. Also when the device was stressed at SC, the drop in FF was delayed when compared to the samples at OC.Also the

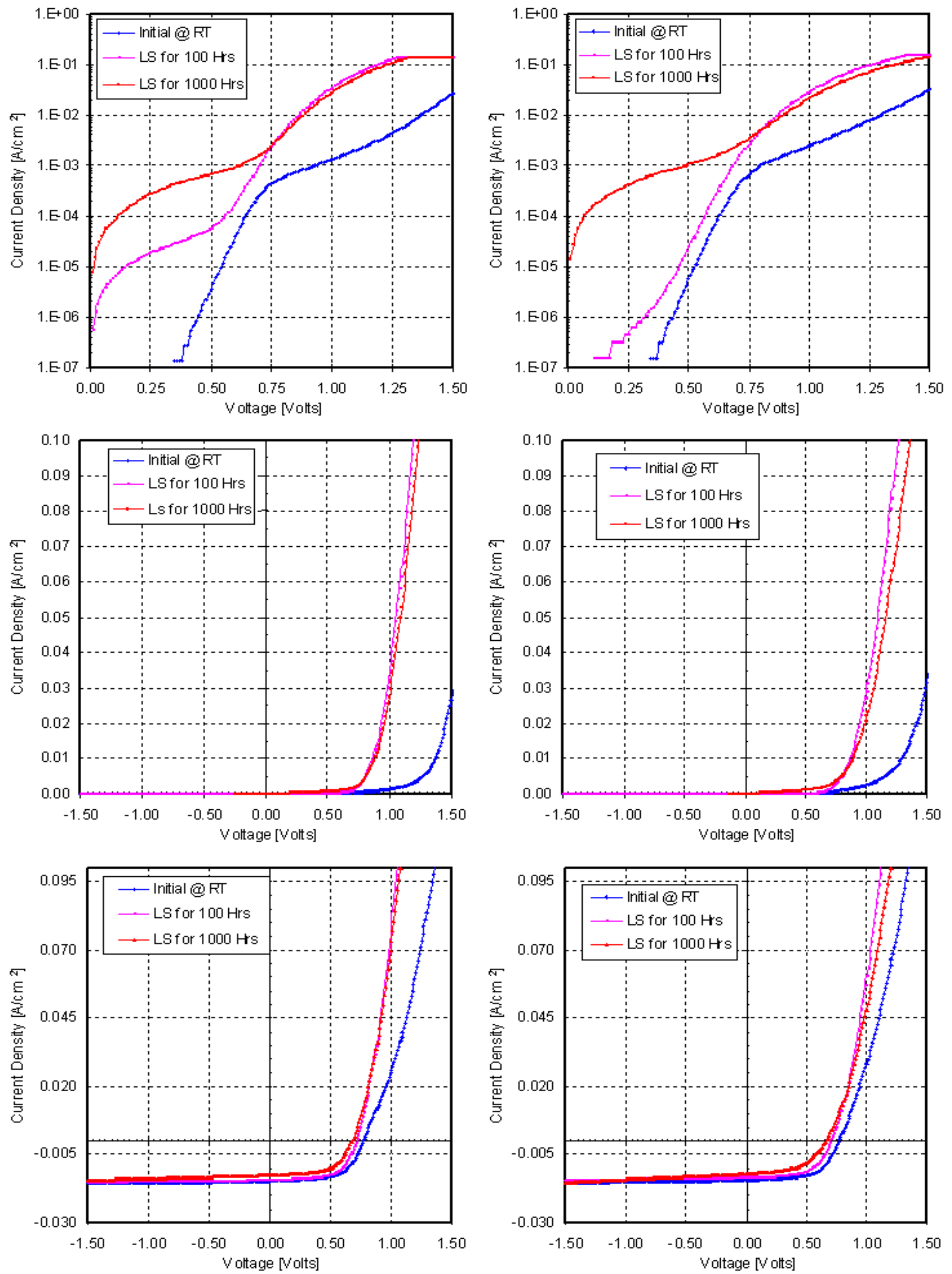


Figure 6.7 JV Characteristics. HT at 360^oC and LS at OC.(Top and Middle: Dark JV and Bottom: Light JV.)

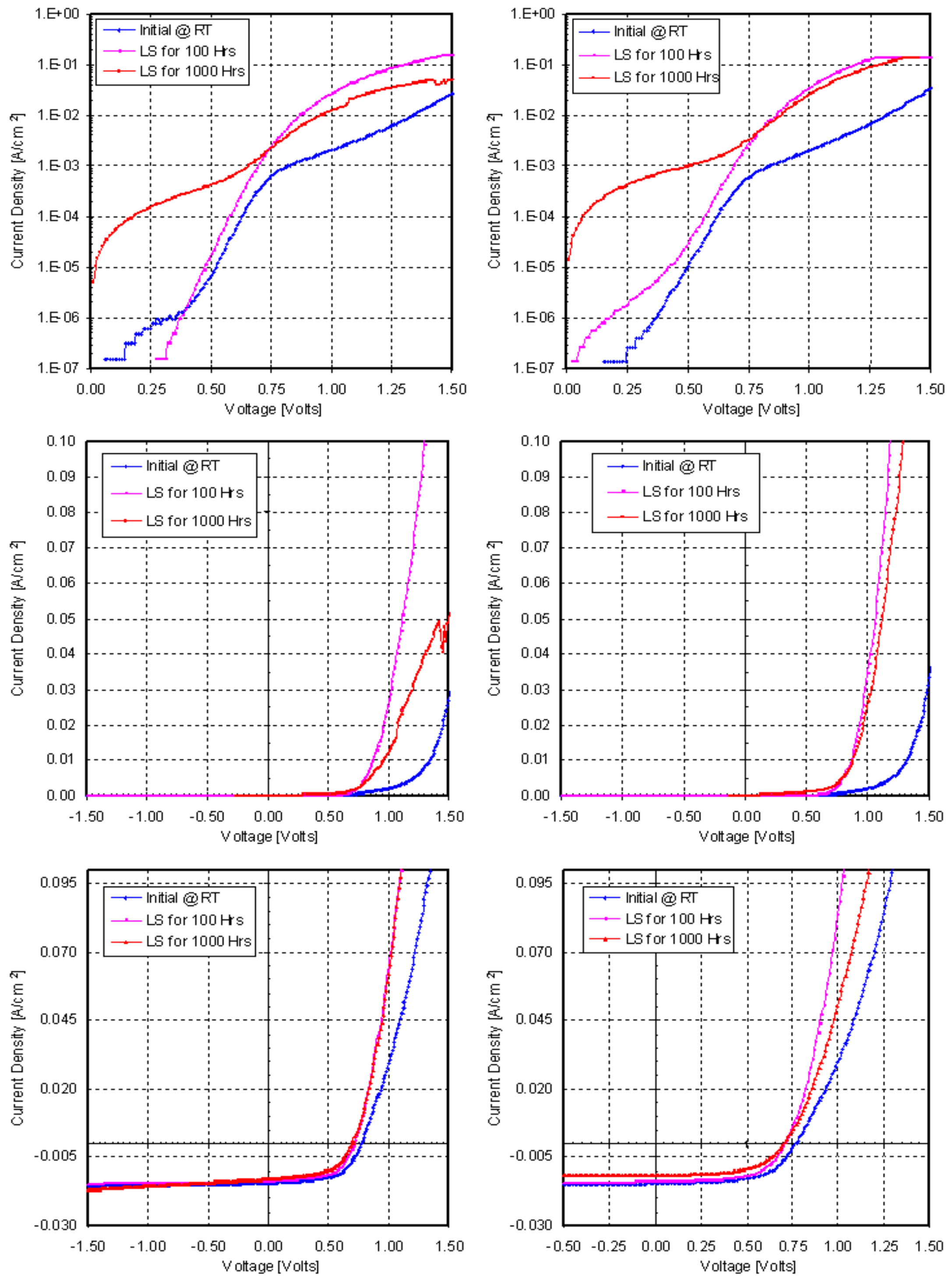


Figure 6.8 JV Characteristics. HT at 360^oC and LS at SC

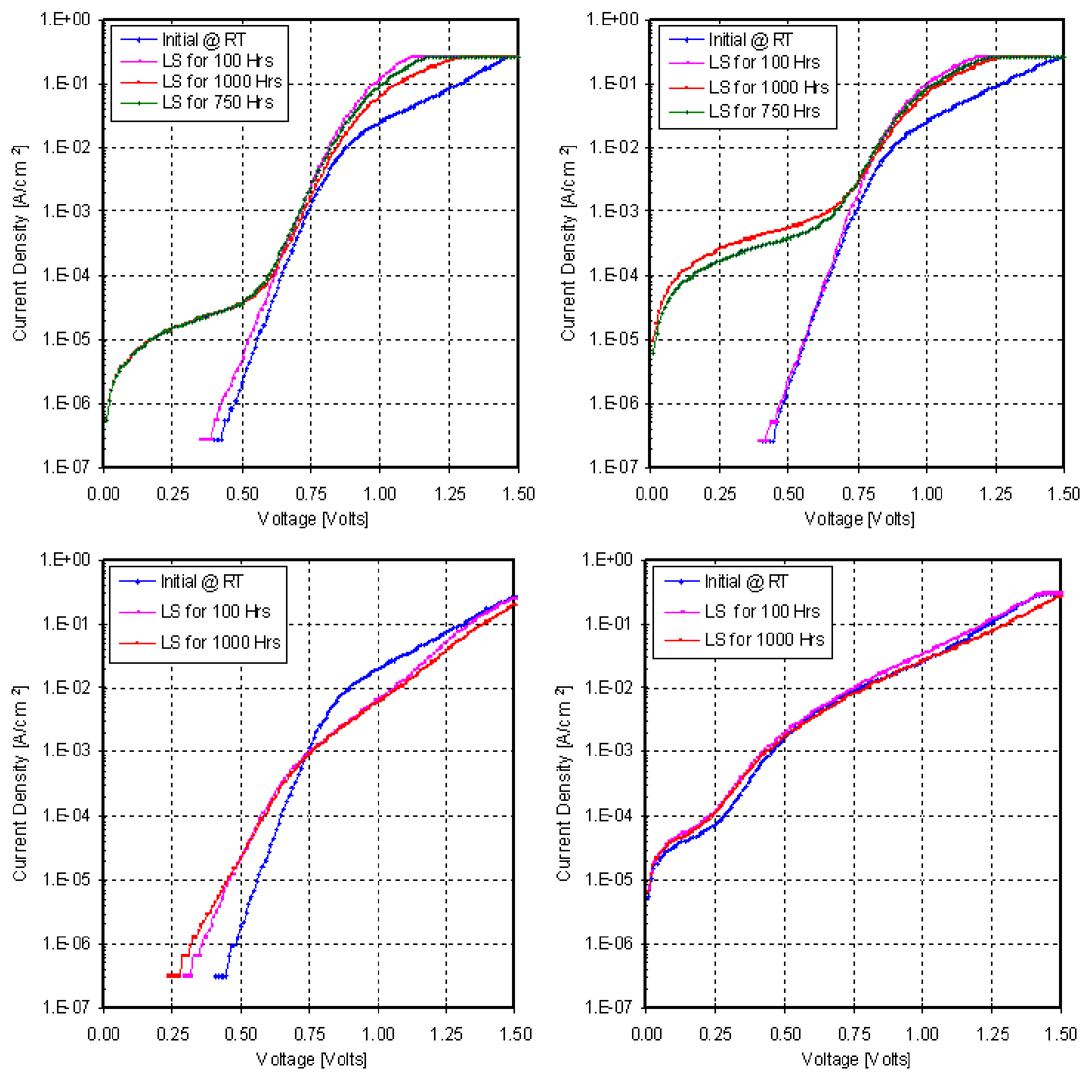


Figure 6.9 Dark JV Characteristics.(HT at 380^oC and LS at Top: OC and Bottom: SC.)

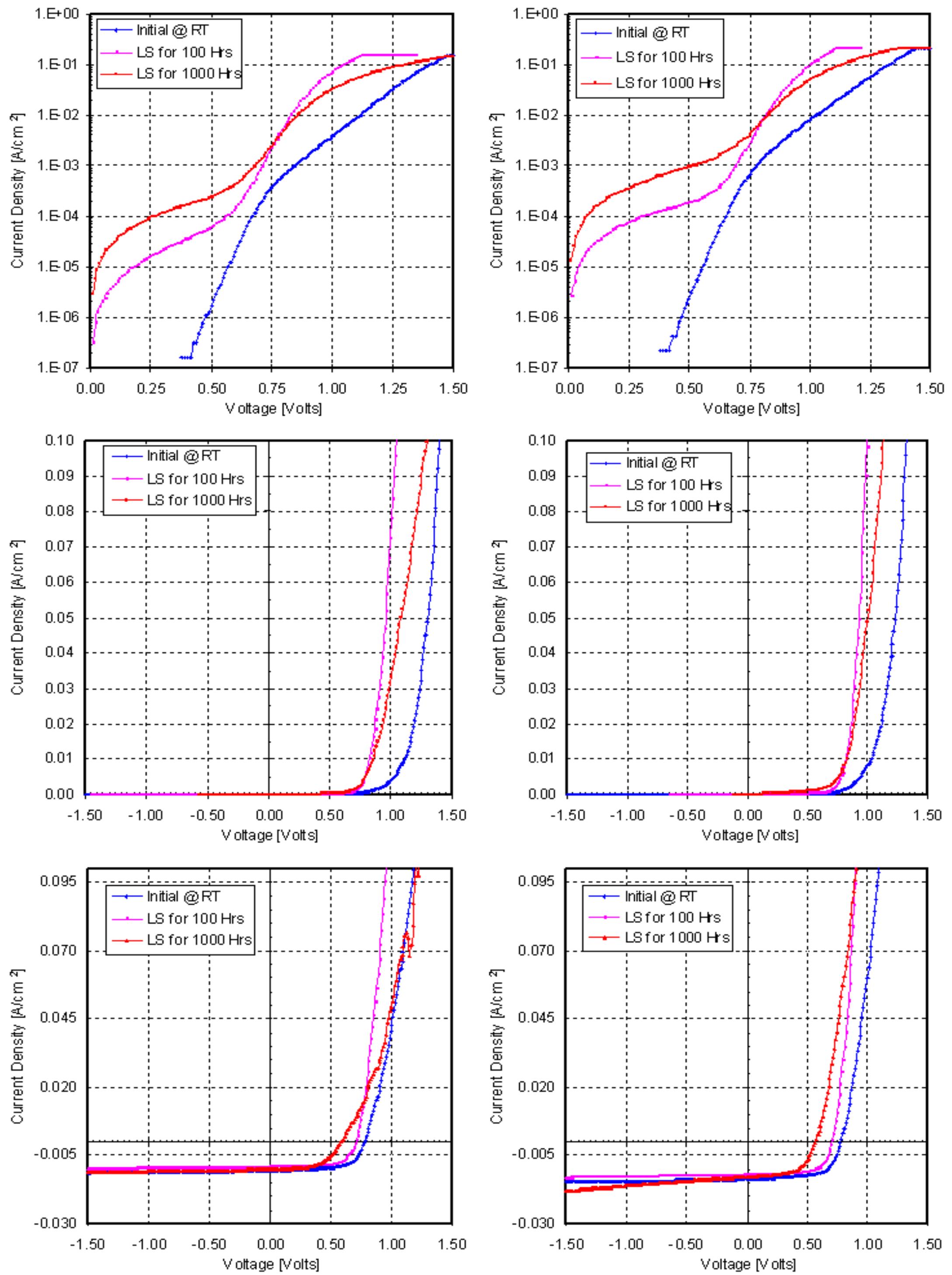


Figure 6.10 JV Characteristics. HT at 400^oC and LS at OC

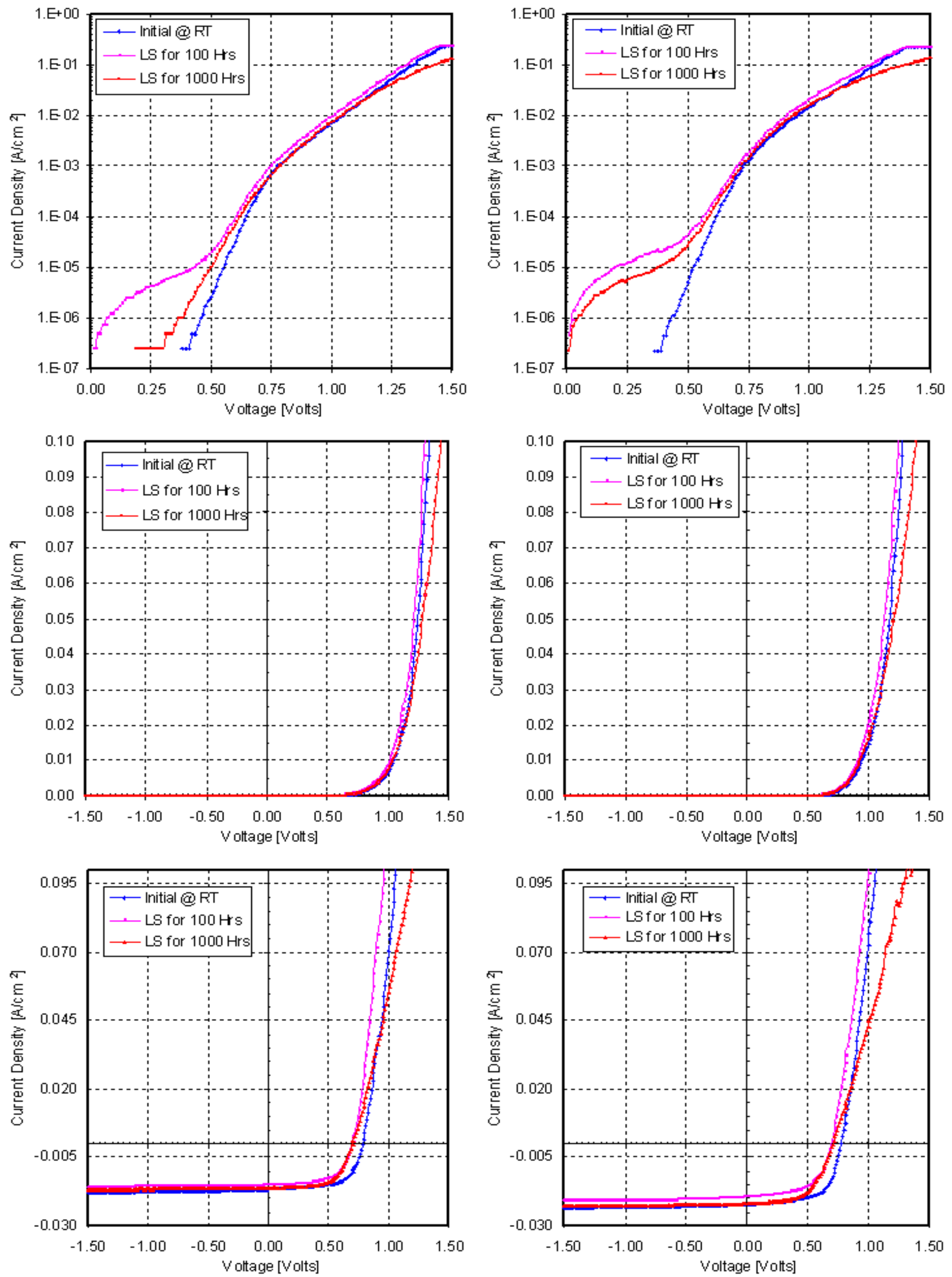


Figure 6.11 JV Characteristics. HT at 400^oC and LS at SC

devices annealed at the operating temperatures of 380^oC and 390^oC gave the better performance during light soaking. The effect of the stress condition on the device stability disappeared, as the $CdCl_2$ annealing temperature was increased.Also the degradation can be attributed mainly to the change in recombination current which was explained previously.

Series and shunt resistances were calculated as explained in section 4.1.4. The results were tabulated in table.6.2 and 6.3. The shunt resistance decreased drastically for samples annealed at 360^oC. The change was reduced as the annealing temperature increased. For the SC condition, the shunt resistance increased for the temperature above 380^oC whereas, the samples annealed at 360^oC had the large decrease.

Table 6.2 Average Estimates of and Series and Shunt Resistances after LS @ OC.

HT(^oC) after $CdCl_2$ treatment	LS Period	$R_{s,light}[\Omega-cm^2]$	$R_{s,dark}[\Omega-cm^2]$	$R_{shunt}[\Omega]$
360	Initial	3.0275	3.975	2497.26
	LS for 1000 Hrs	3.38	3.535	461.6
380	Initial	2.525	6.23	2269.07
	LS for 1000 Hrs	2.99	1.405	591.05
400	Initial	1.882	2.81	2107.86
	LS for 1000 Hrs	3.36	3.25	1730.54

Table 6.3 Average Estimates of and Series and Shunt Resistances after LS @ SC.

HT(^oC) after $CdCl_2$ treatment	LS Period	$R_{s,light}[\Omega-cm^2]$	$R_{s,dark}[\Omega-cm^2]$	$R_{shunt}[\Omega]$
360	Initial	2.73	3.85	2109.77
	LS for 1000 Hrs	3.53	3.1	458.83
380	Initial	2.39	11.62	2160.2
	LS for 1000 Hrs	4.10	4.95	4366.29
400	Initial	2.11	2.63	2248.16
	LS for 1000 Hrs	3.74	5.45	3146.35

6.2 Cu_xTe As Back Contact

Even though detailed study of the effect of Cu_xTe back contact on device stability, some cells were stressed during initial phase of this work. The device structure was 7059 glass substrate/SnO_2/CBD CdS/CSS CdTe/Cu_2Te. $CdCl_2$ heat treatment was given at 390^oC for 25 minutes. The Te rich layer prepared with Bromine/Methanol solution was sputtered with Cu_2Te as back contact. Above Cu_2Te,molybdenum was sputtered as electrode for Cu_2Te. Annealing treatment was given at 270^oC for 25 minutes in He ambient. Indium was used as electrode for front contact. The Cu_2Te thickness varied from 60^oA to 70^oA.

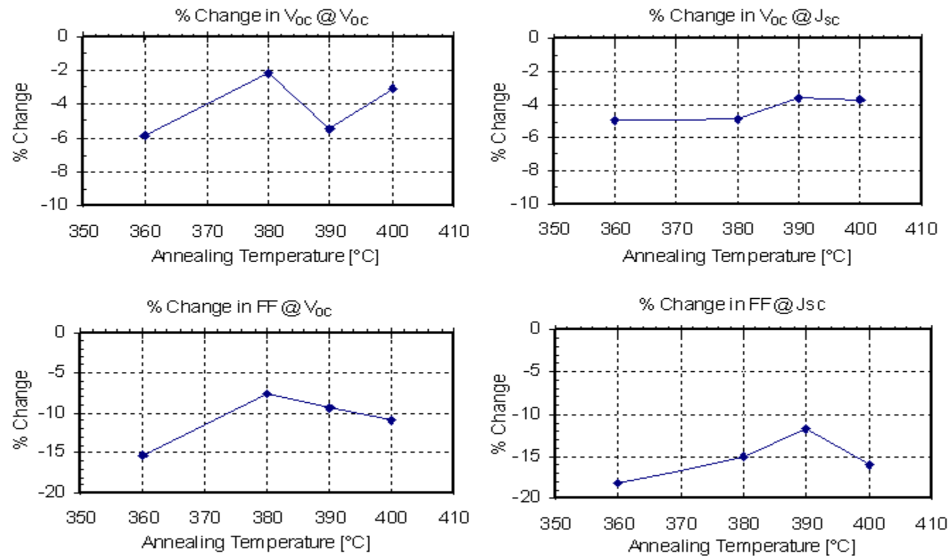


Figure 6.12 Summary of Degradation Behavior

The dark and light JV characteristics for samples with Cu_2Te of 60$\mathring{A}$ and 70$\mathring{A}$ respectively were shown in fig.6.13. It was evident from dark JV that there was no change in the recombination current region of the dark JV characteristic for 70^oA sample and its apparent increase for 60$\mathring{A}$ sample after 1000 hours of light soaking @OC condition. Also there was increase of $R_{s,dark}$ in the case of 70$\mathring{A}$ Cu_2Te sample.Whereas the slope in the high current region (Rs) remained unaffected for 60$\mathring{A}$ sample with the left shift in dark JV curve which was the probable indication that the the front contact barrier was affected. When the Cu_xTe thickness was increased to 70$\mathring{A}$, there was "Roll Over". This suggests that the Cu diffusion may lead to this back contact deformation.But surprisingly the 60$\mathring{A}$ sample did not exhibit any such

behavior.This leads to the conclusion that under certain conditions, the back contact with Cu remains unaffected even after light soaking.

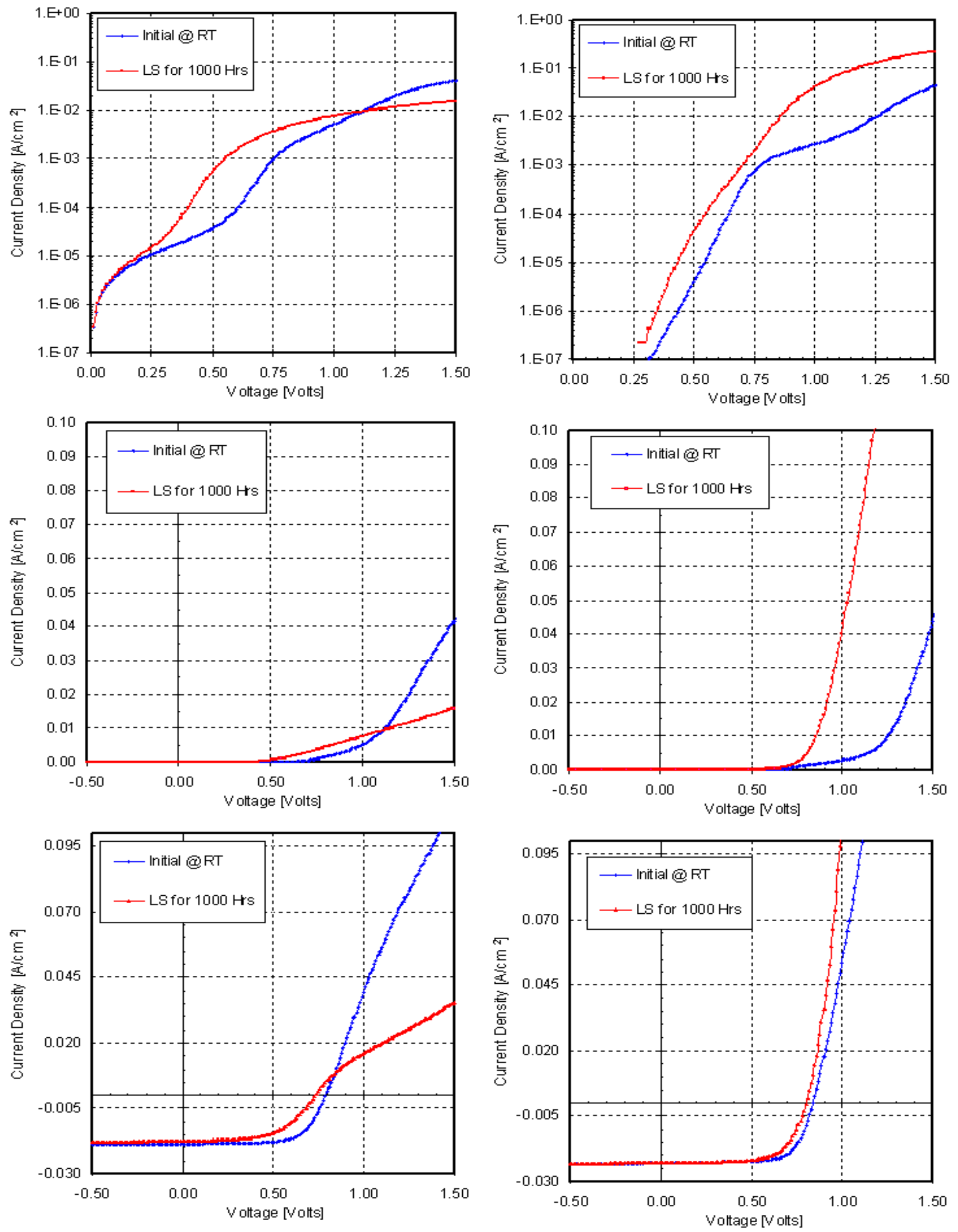


Figure 6.13 Degradation behavior of samples with Cu_2Te as Back contact with Thickness Left: 70^oA and right: 60^oA respectively.

Chapter 7
Conclusion

Light soaking experiment of CdTe/CdS solar under different stress conditions was conducted up to 1000 hours. The cells are made at different process conditions to observe the effect of process conditions on device stability.

The change in the $CdCl_2$ heat treatment or stress condition essentially did not affect the change in Voc during light soaking. Whereas the increase in the temperature of $CdCl_2$ heat treatment slowed down the drop in FF. Also when the device was stressed at SC, the drop in FF was delayed when compared to the samples at OC. When the $CdCl_2$ heat treatment reached optimum temperature of $380 - 390^oC$, the degradation was minimum.The degradation can be attributed mainly to the change in recombination current.

Also under certain conditions, the back contact with Cu remains unaffected even after light soaking.

7.1 Recommendations for Future Studies

As the duration of this investigation is too short to make complete analysis of stability behavior of CdTe/CdS solar cells, the following studies are recommended to be conducted in future.

1. The range of stress conditions can be widened to characterize their effect on

stability of devices produced under various process conditions.

2. More Quantum mechanical and thermo dynamic approaches are needed to understand the non linear behavior of CdTe under stress. Sophisticated approaches like EBIC, photo mapping will provide more evidence to support theory.

3. Devices with CuCl treatment on CdS and also Cu treatment on different layers of device are needed to be tested under light soaking with more frequent measurements of JV characteristics and CV profile.This is possible by using automated measurement setup.

4. Effect of sodium and Hg on device degradation can be analyzed.

5. Effect of different TCOs on device degradation is also needed to be studied.

References

1. S.E. Asher et. al, Determination of Cu in CdTe/CdS Devices Before and After Accelerated Stress Testing,IEEE PV Spec. Conf.,Vol.28, pp. 479-482 (2000)

2. D. Cahen et. al, Overcoming Degradation Mechanisms in CdTe Solar Cells,Final Report,Weizmann Institute of Science,Israel, NREL (1998-2001)

3. D. L. Btzner et al, Thin Solid Films,Vol.387, No.1-2, pp. 151-154 (2001)

4. S.S.Hegedus et al,Analysis of Stress Induced Degradation in CdS/CdTe Solar Cells, NCPV Program Review Meeting, Denver, CO, April 16-19 (2000)

5. Su-Hai Wei et. al, Electronic structures and defect physics of Cd-based semiconductors,IEEE PV Spec. Conf.,Vol.28, pp. 483-486 (2000)

6. E.H Rhoderick et. al, J.Appl.Phys,D:App. Phy.,Vol.4,pp. 1589-1601 (1971)

7. Alan L. Fahrenbruch and Richard H. Bube, Fundamentals of Solar Cells,Academic Press,New York,pp. 234 (1983)

8. T.J.McMahon et. al, Progress toward a CdTe Cell Life Prediction,NCPV Photovoltaics Program Review,CP 462, pp. 54-61(1999)

9. R.C Powel et. al, Stability Testing of CdTe/CdS Thin Film PV modules,IEEE PV Spec. Conf.,Vol.25, pp. 785 (May,1996)

10. K.D.Dobson et.al, Stability of CdTe/CdS Thin Film Solar Cells,Solar Energy Materials and Solar Cells,Vol.62, pp. 295-235 (2000)

11. D.Grecu et.al, Appl.Phys.Letter,Vol.75, No.6, pp. 361-363 (1999)

12. H.R.Moutinho et. al, Studies of Recrystallization of CdTe Thin Films After $CdCl_2$ Treatment,IEEE PV Spec. Conf.,Vol.26, NREL (1997)

13. K.M.Al Shibani, Effect of Iso Thermal Annealing on CdTe and the study of electrical Properties of Au-CdTe Schottky Barriers,Physica B.,Vol.322,pp. 390-396 (2002)

14. B.E McCandless et al, 25th PVSC Conference,IEEE,Vol.25,pp. 781 (1996)

15. R.Ludeke, A Survey of Optical and Electrical Properties of Thin Films of II-VI Semiconducting Compounds,J.Vacuum Science and Tech.,Vol.8,pp. 199-207 (1971)

16. H.Oumous et al, Optical and Electrical Properties of Annealed CdS thin films Obtained from a Chemical Solution,Thin Solid Films,Vol.386,pp. 87-90 (2001)

17. Fredrick Buch, Photovoltaic II-VI Compound Heterojunctions For Solar Energy Conversion,PhD Dissertation, Stanford University, June (1976)

18. A.Niemegeer and M.Burgelman, J.Appl.Phys.,Vol.81, No.6, pp. 2881-2885 (1997)

19. James R.Sites, Solar Energy Materials and Solar Cells,Vol.75, No.1-2, pp. 243-251 (2003)

20. Donald Thomas Morgan, An Investigation into Degradation of CdTe Solar Cells,M.S.Thesis, Colorado School of Mines, pp. 20-29 (1998)

21. Donald A. Neamen, Semiconductor Device Physics: Basic Principles, Third Edition, Tata McGraw Hill, pp. 238-318 (2002)

22. C.S Ferekides et.al, Thin Solid films,Vol. 361-362, pp. 520-526 (2000)

23. T.Okamoto et.al, Thin Solid Films, 387, pp. 6-10 (2001)

Appendix A
Measurement Automation

Automation of the Stability measurement system fulfills the following needs

- Consistency and accuracy of measured data,
- Reduction in measurement time and hassles involved,
- Easy Configuration of Stress Conditions,
- Massive Data Collection and
- Data logging and monitoring of stress temperature,humidity and stress period.

The hardware part consists of solid state relays which is controlled by PCI digital IO card via opto couplers.The relay is in NC position when not energized.The required stress conditions can be configured in this position via terminals provided from NC and GND(which is connected to n side of diode to be tested) outputs.The possible configurable stress conditions are open circuit,short circuit,maximum Load and, forward and reverse bias.When the relay is energized,the device under test(DUT) is connected to measurement device.Care must be taken while programming relays to avoid simultaneous activation of more than one relay.The dip switch is provided to isolate a relay from experiment in case of circuit failure.Totally 48 relays are controlled by a single 48 DIO card which consists of 2-8255 PPI chips. DUT is thus continuously maintained in the desired stress condition except for the duration in few seconds during measurement.Keithley 2400 source meter is used to sweep the voltage from -2V to +2V in steps of 0.02V and measure the current during I-V measurement.

Omega 44-M data logger is used to monitor temperature and humidity.It is connected from the stress oven via RS 232 interface.Software is provided by Omega to collect the data. It contains internal temperature and humidity sensors and two external thermistors.Sampling interval can be varied from 0.5 sec.

The software is developed using LabView.The front panel of main vi program and its block diagram of data flow during dark cycle are shown.Some of the salient features of the software are

- Day and night cycle are monitored and logged,
- Logic is entirely based on real time test condition,
- The measurements are avoided in case of lamp failure,

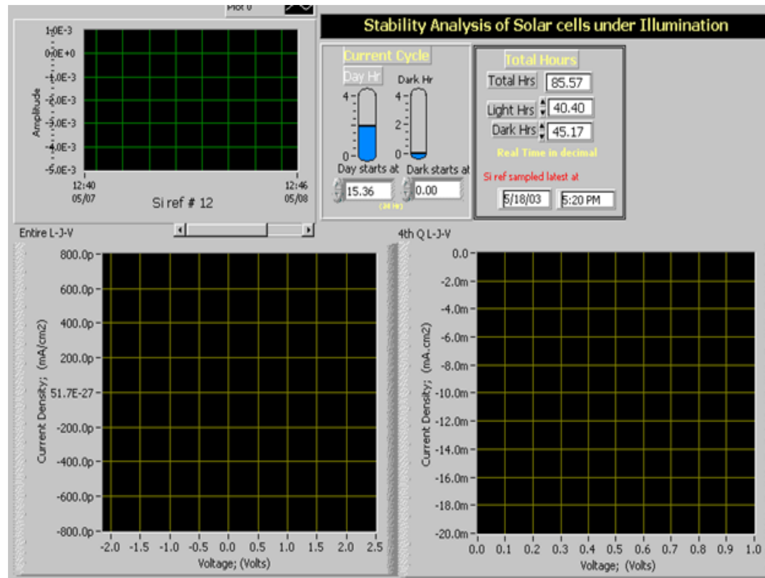


Figure A.1 Front Panel of VI Program for Stability Testing

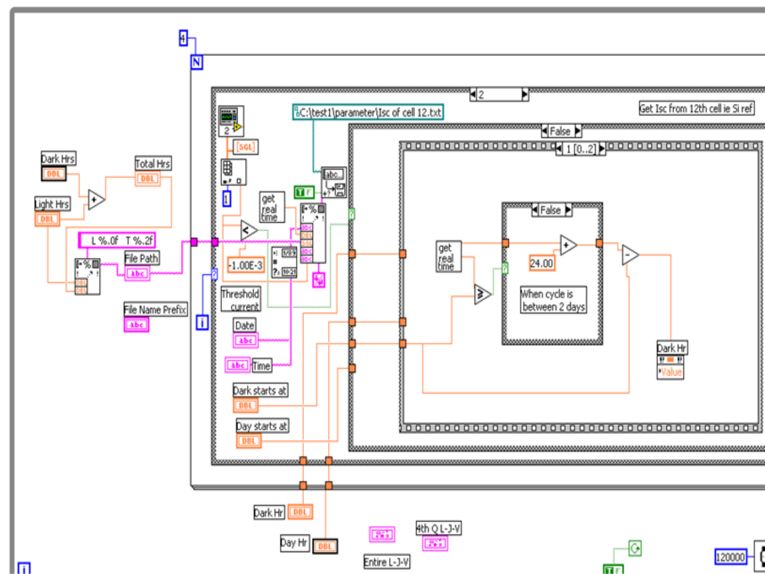


Figure A.2 Snap Shot of Block Diagram

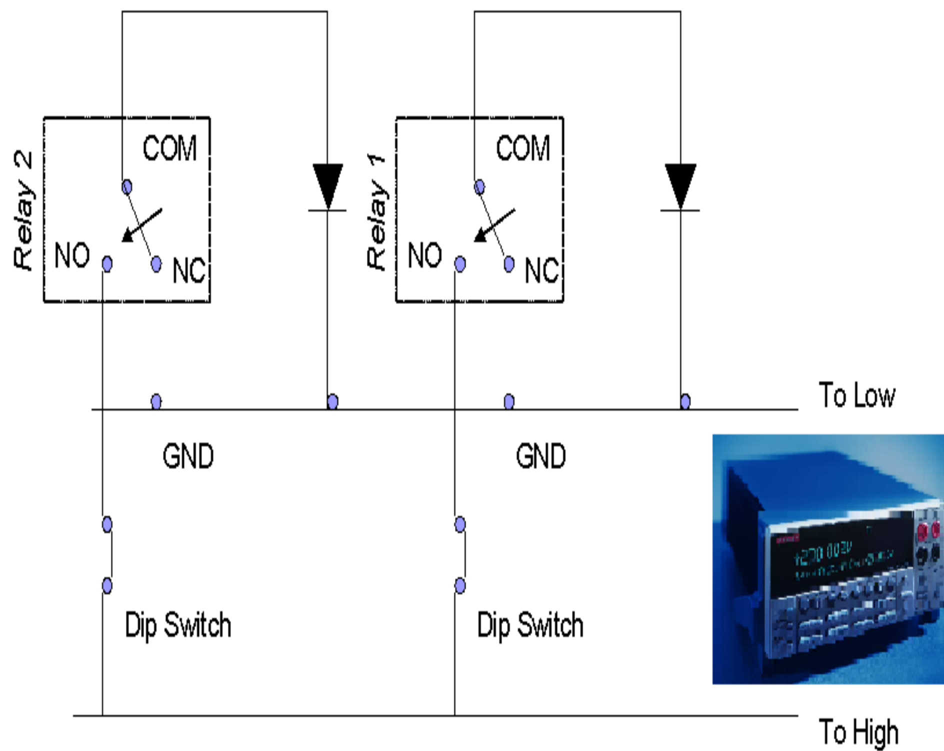


Figure A.3 Circuit Configuration of Hardware Setup

- The total light soaked hours are calculated with milli second accuracy,
- Day transition will not cause problems,
- Measurement timings can be custom defined for any number of times needed
- The code is optmised to avoid memory leaks and
- The device parameters are stored in well defined manner for easy retrieval for data analysis.

  The measurement timings must be given in ascending order.Also the interval should be greater than the single measurement set period of (18+5) minutes to avoid missing of data points.

Figure A.4 Input Panel for Measurement Interval Specification

Appendix B
JV Characteristics

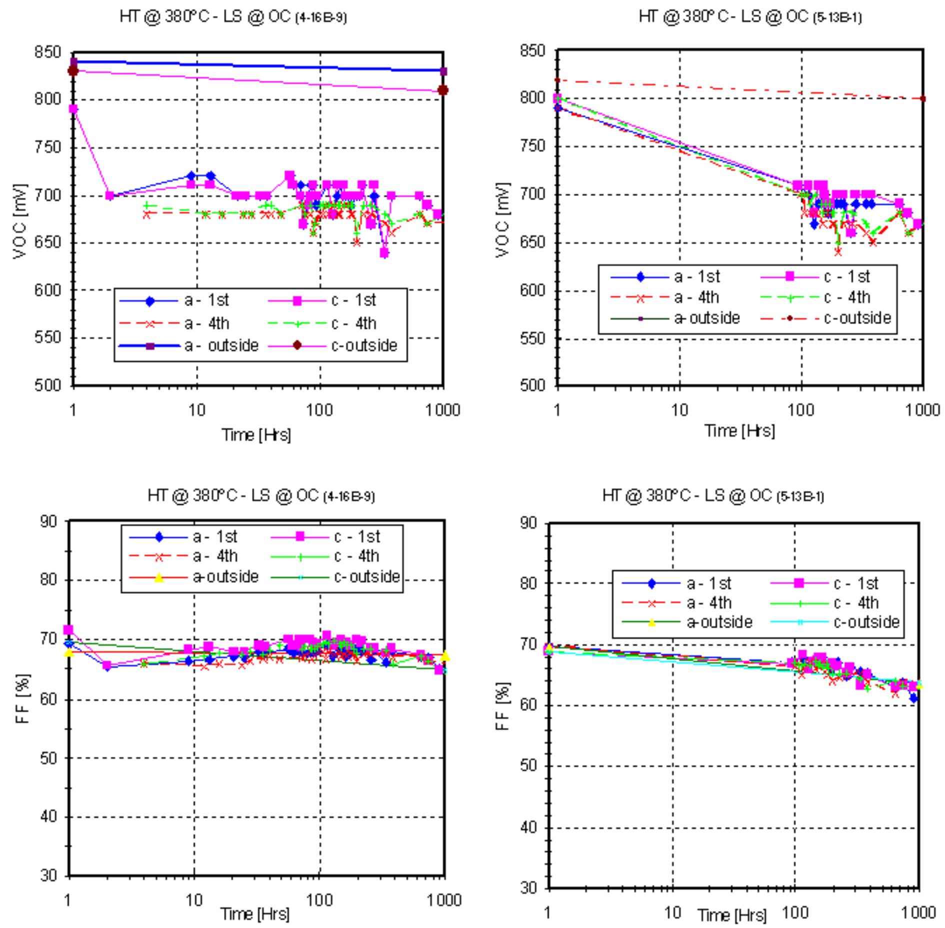


Figure B.1 Degradation Behavior: HT @ 380^oC and LS @O.C

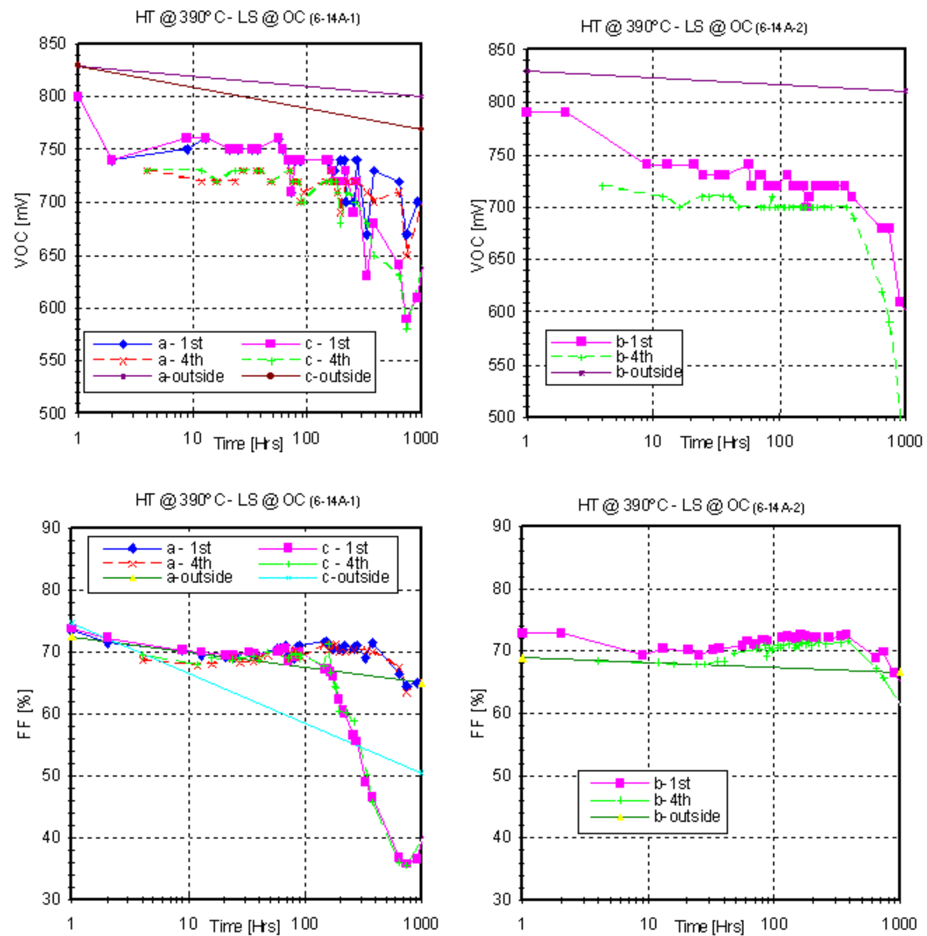


Figure B.2 Degradation Behavior: HT @ 390^oC and LS @O.C

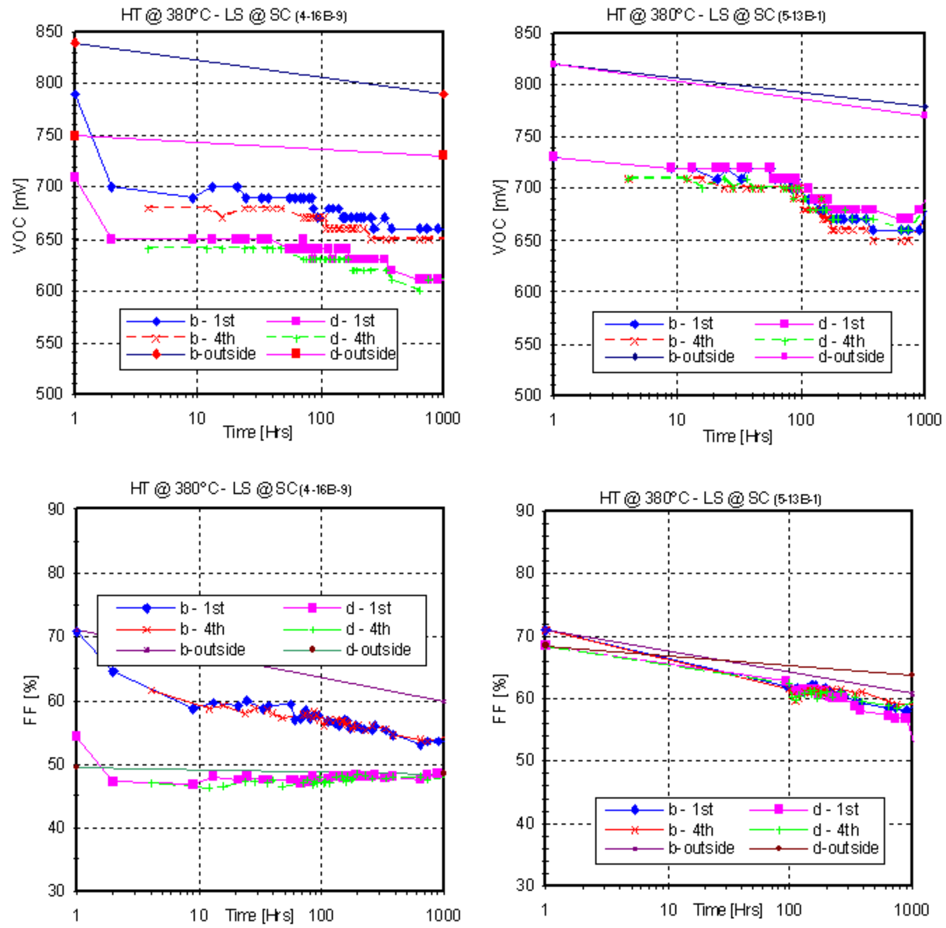


Figure B.3 Degradation Behavior: HT @ 380^oC and LS @S.C

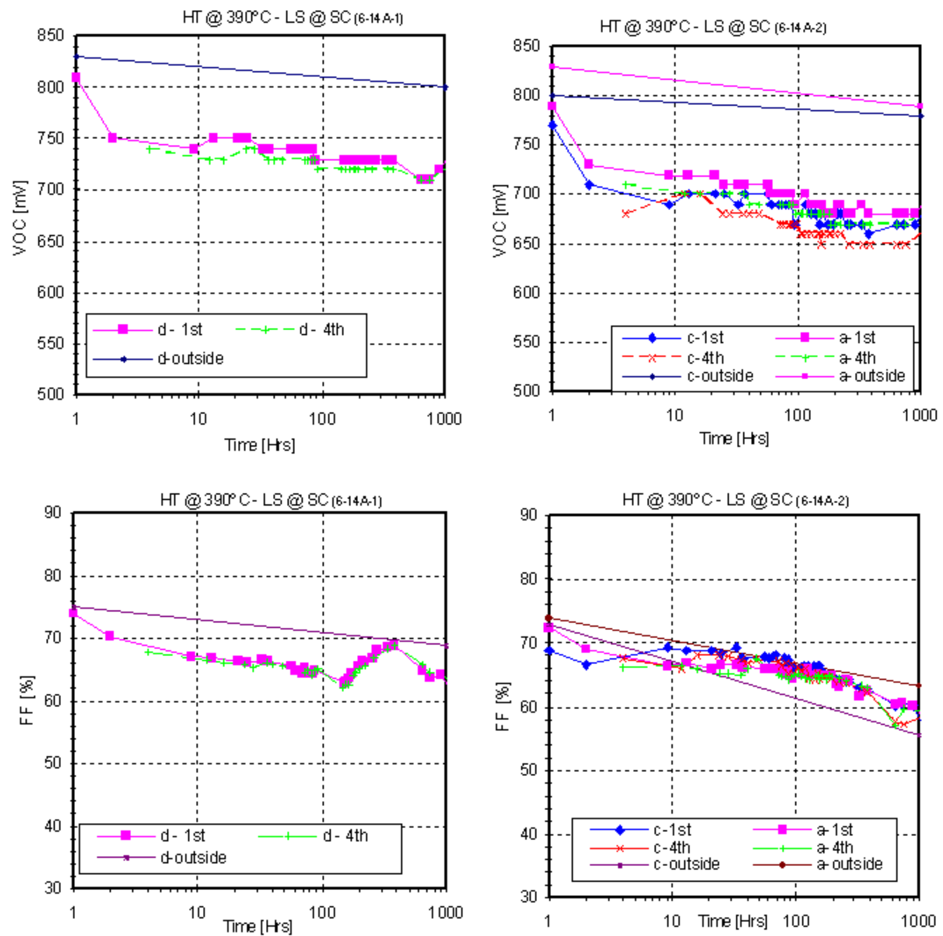


Figure B.4 Degradation Behavior: HT @ 390^oC and LS @S.C

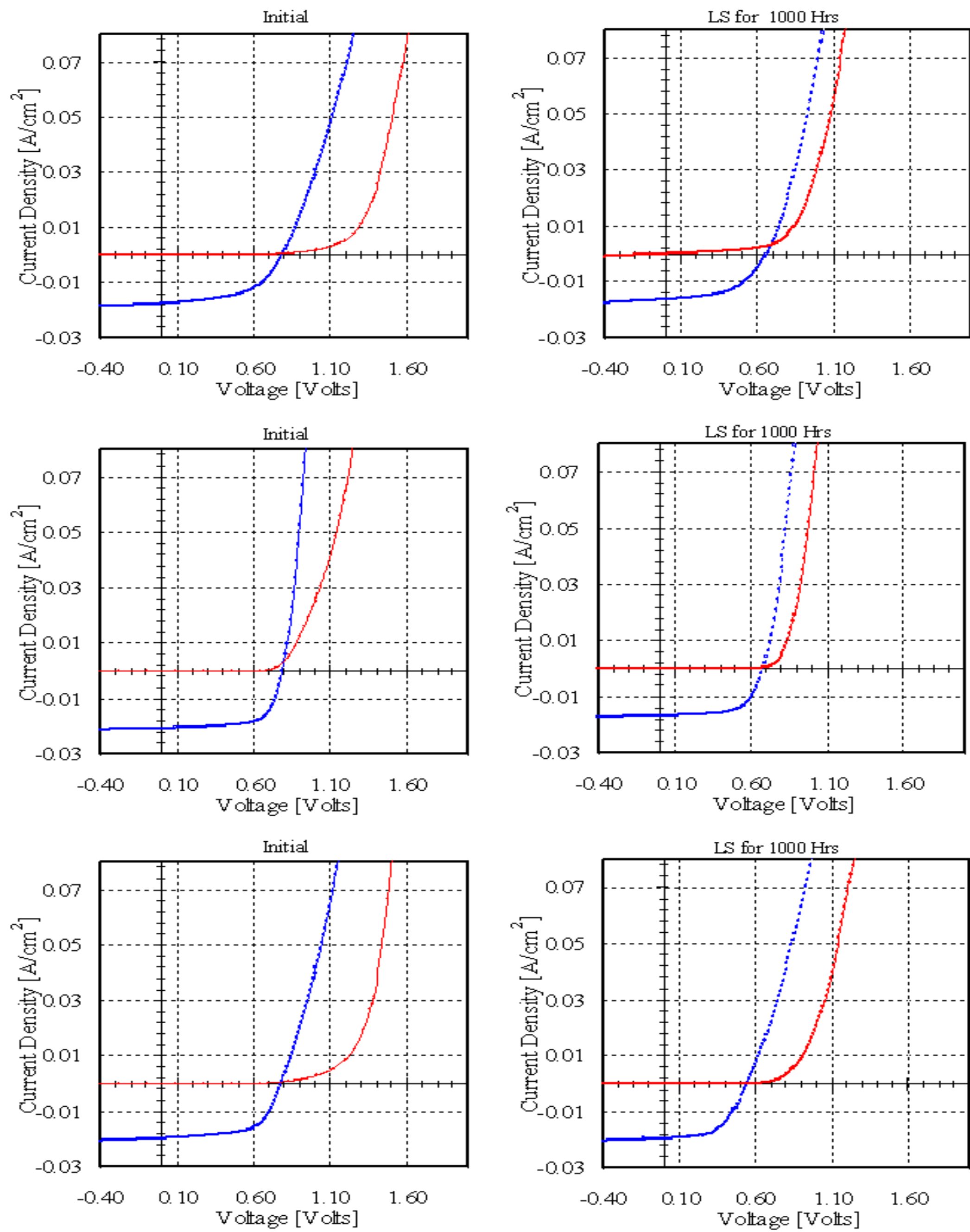


Figure B.5 Cross Over Effect for Samples LS @ OC and HT @ Top : 360^oC , Middle : 380^oC and Bottom : 400^oC

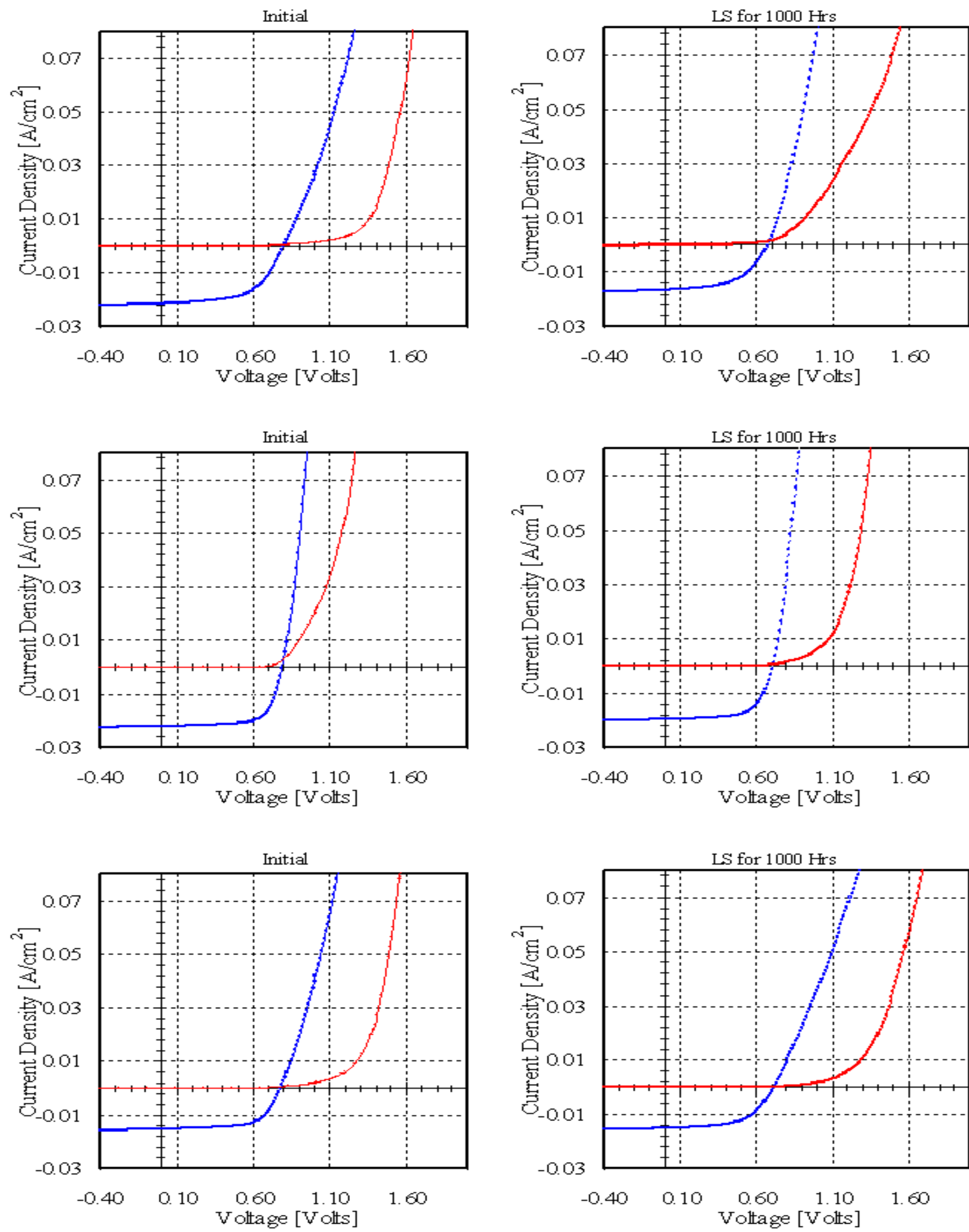


Figure B.6 Cross Over Effect for Samples LS @ SC and HT @ Top : 360^oC Middle : 380^oC and Bottom : 400^oC

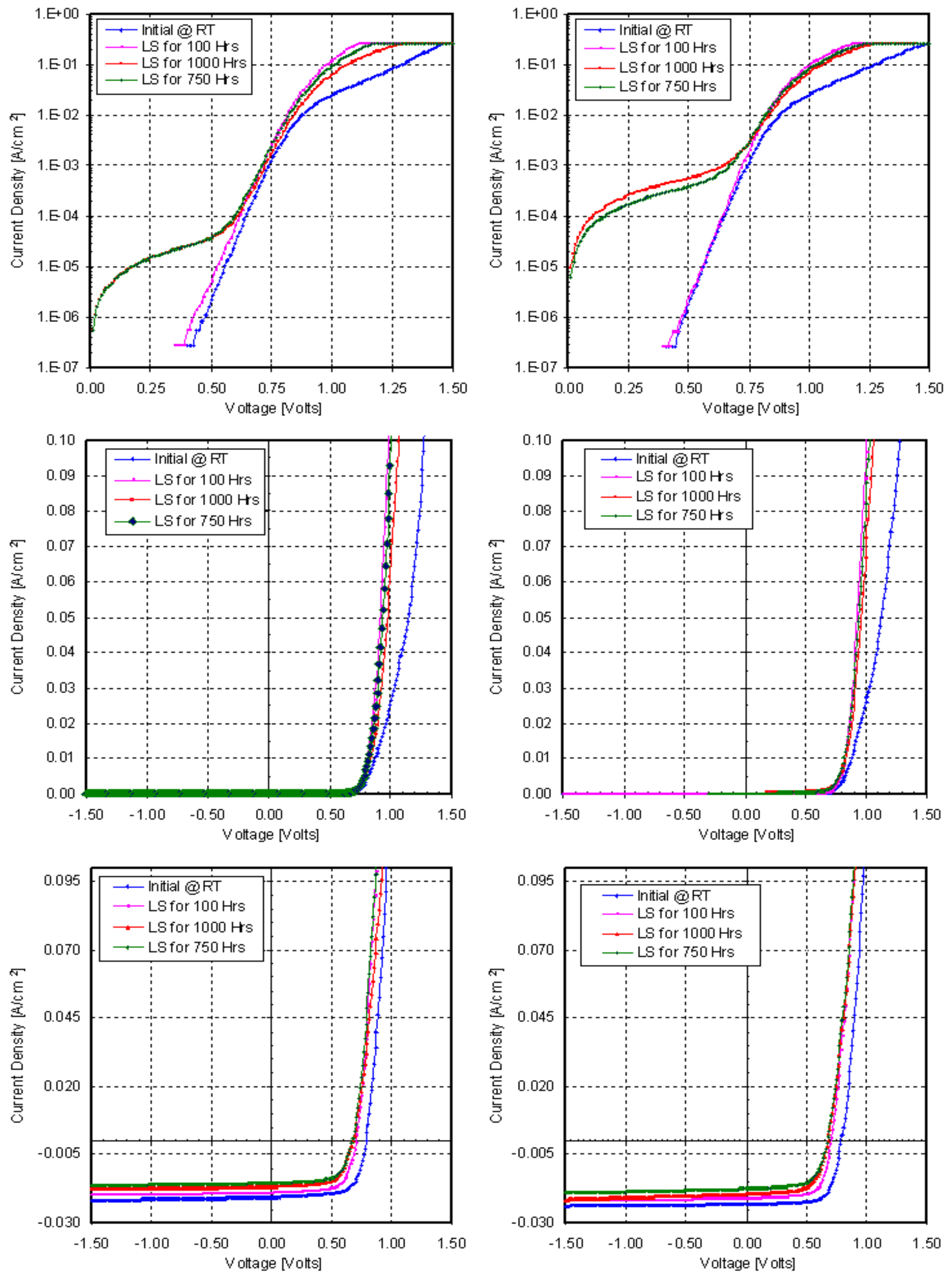


Figure B.7 JV Characteristics. HT at 380^oC and LS at OC.(Top and Middle: Dark JV and Bottom: Light JV.)

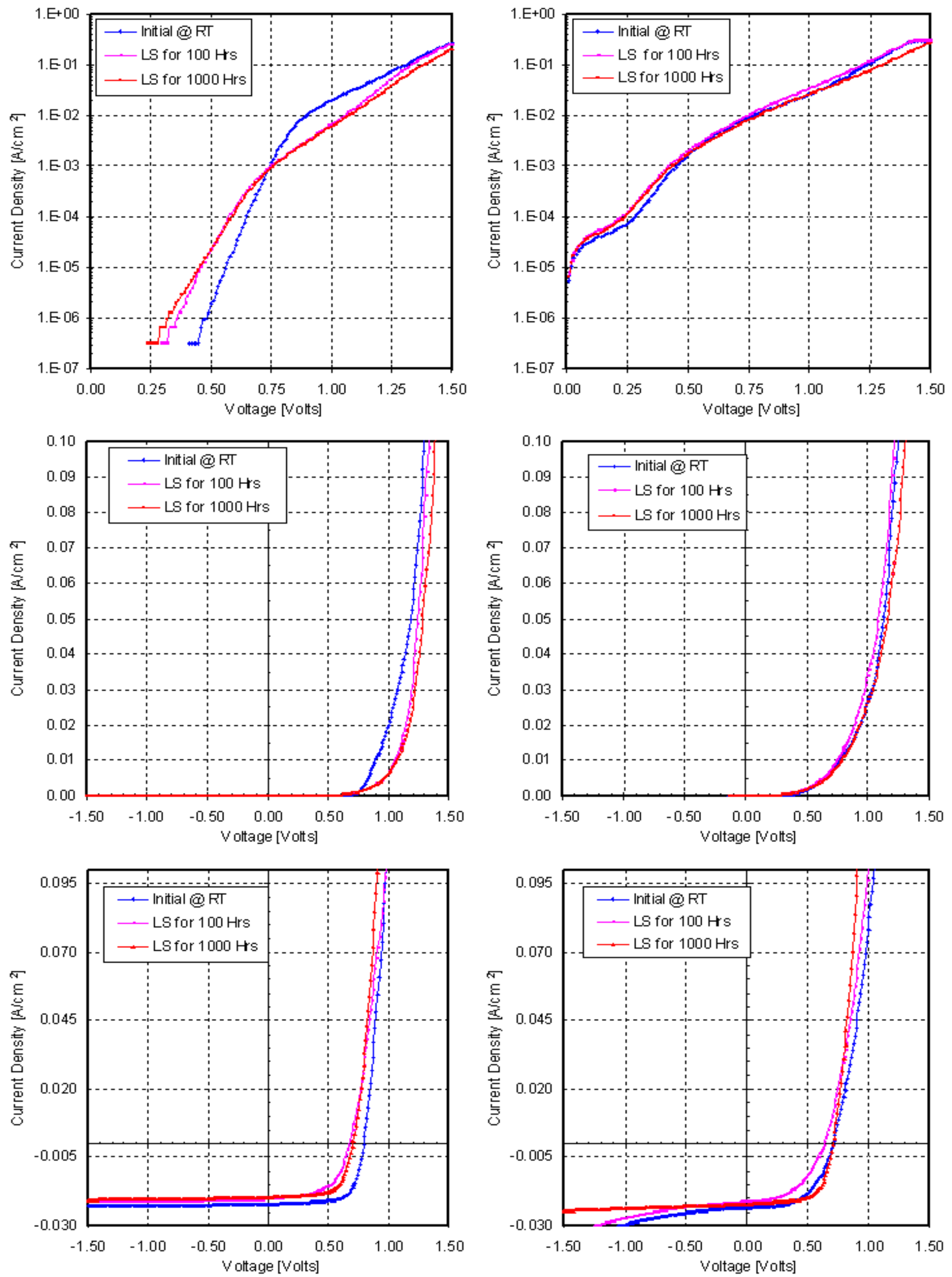


Figure B.8 JV Characteristics. HT at $380^{o}C$ and LS at SC

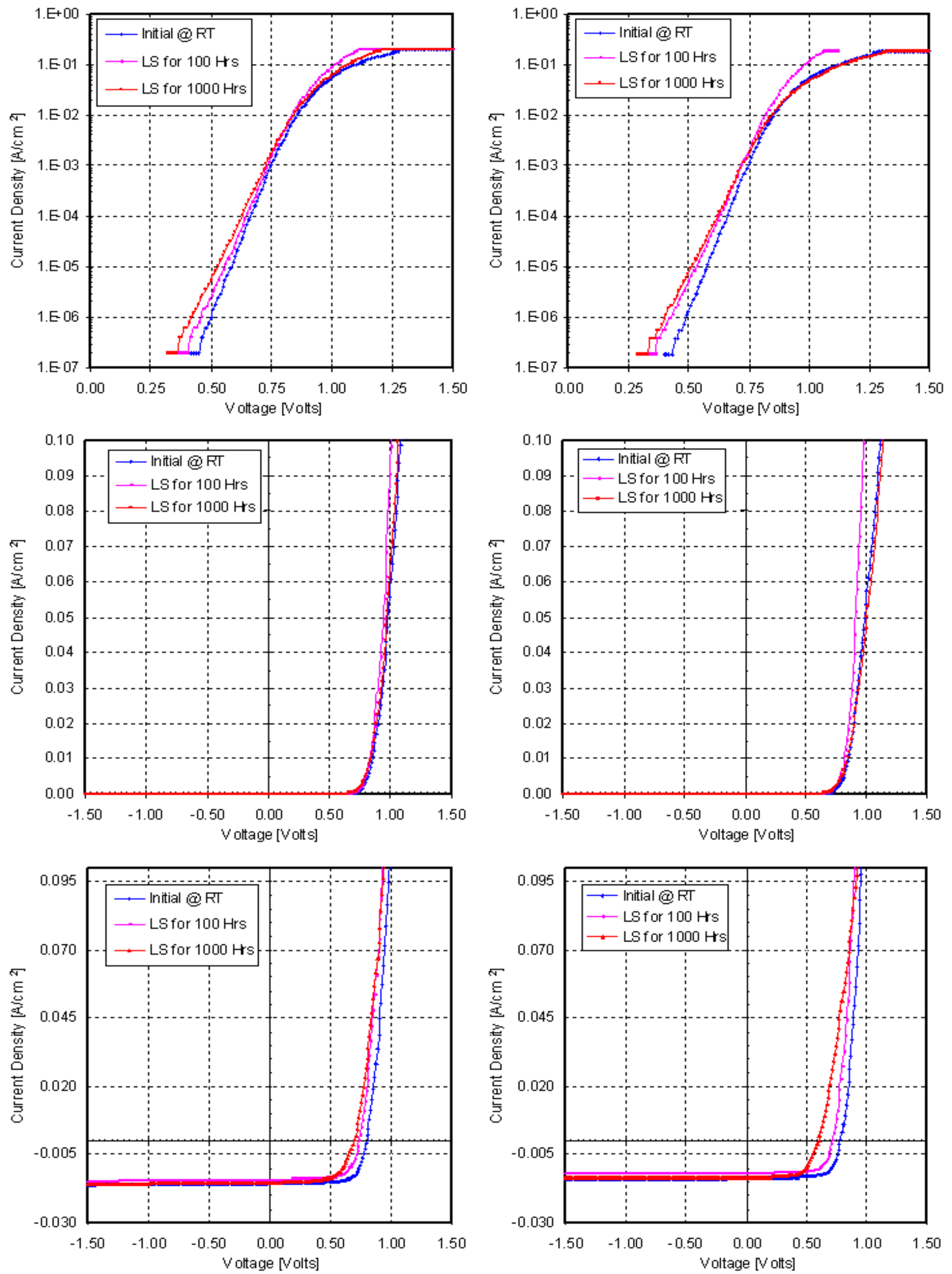


Figure B.9 JV Characteristics. HT at 390^oC and LS at OC

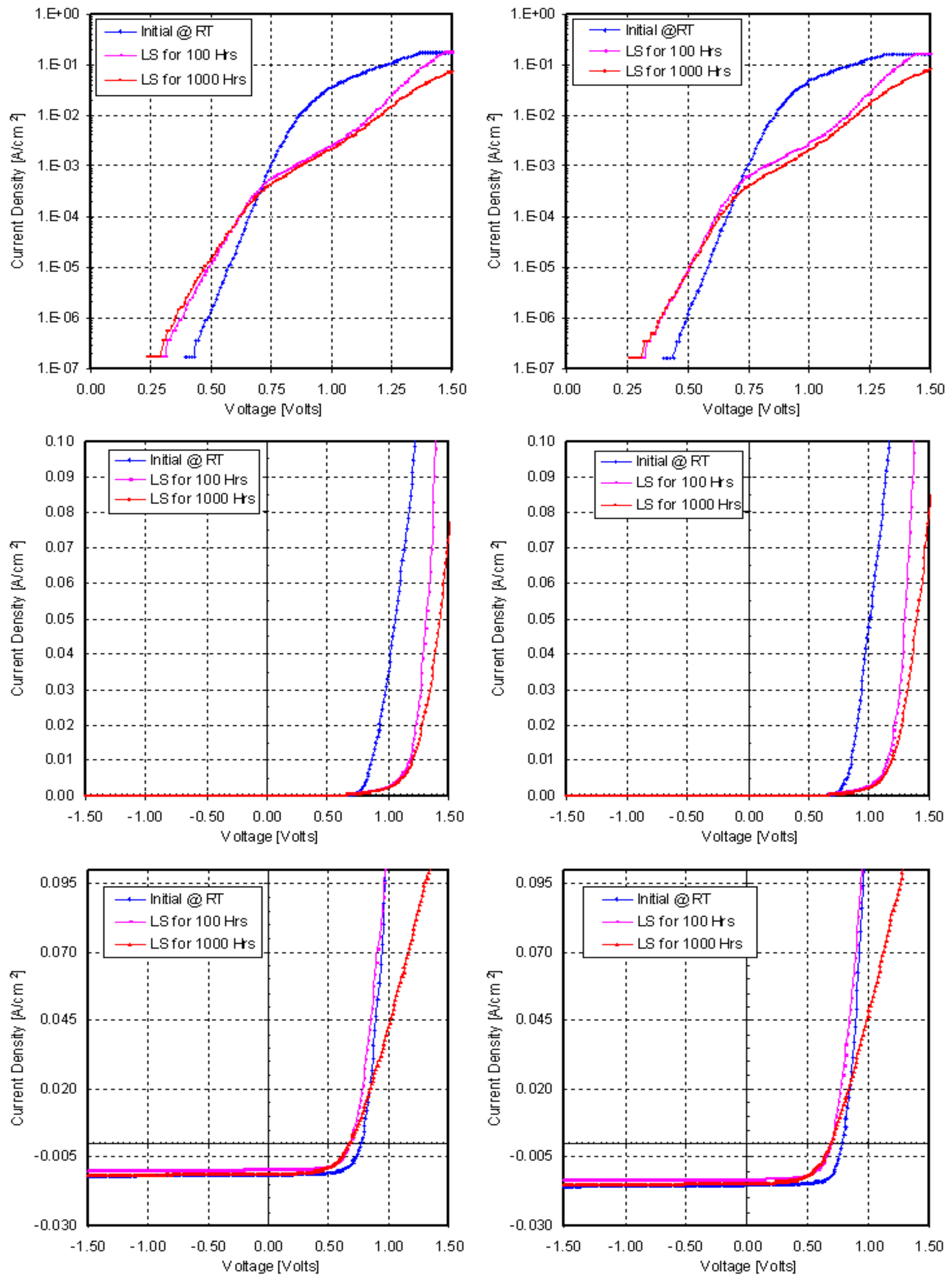


Figure B.10 JV Characteristics. HT at 390^oC and LS at SC

Appendix C
Preliminary Results for Effect of Copper

C.1 Copper in Back Contact

The copper is added with standard HgTe doped graphite paste and used as back contact to make device. The device structure is 7059 glass substrate /SnO_2/ CBD CdS/ CSS CdTe/ HgTe:graphite paste with added copper. $CdCl_2$ is evaporated over CdTe layer and given annealing treatment at 390^oC for 25 minutes. The Te rich layer prepared with Bromine/Methanol solution is then applied Cu added HgTe doped Graphite paste. The sample is then kept at room temperature for 12 hours before heat treatment. Annealing treatment is given at different temperatures ranging from 175^oC to 300^oC for 25 minutes in He ambient. Silver and Indium are used as electrodes for back and front contacts respectively. The added copper content in back contact varies from 0.05 gm to 0.2 gm of Cu in 10 gm of HgTe doped graphite paste.

Figure C.1 indicates the dependance of device parameters over the copper concentration in back contact and Contact Annealing temperature. The optimal temperature is between 225^oC and 240^oC in all cases. The excess temperature in heat treatment results in significant loss in photo generated carriers in bulk CdTe layer which is visible in fig.C.2. This result can be attributed to enhancement of $(Cu_i^+ + V_{cd}^{2-})$ formation in CdTe bulk layer due to high annealing temperatures which in turn raises trap and recombination centers in the CdTe bulk layer.

The dark JV dependance shown in fig.C.3 reveals the fact that the junction is nearly unaffected irrespective copper content in back contact. Further stress studies will reveal the information about stress induced junction degradation. Also the contact rectification is worsened as the Copper content increases in back contact. Further this increase in Cu levels off annealing effect on contact rectification possibly by the increase in formation of recombination because of more Cu diffusion in the CdTe bulk layer.

C.2 Effect of Pre Copper Treatment and Contact Annealing

The copper is directly deposited on CdTe layer by sputtering before applying undoped graphite. The device structure is 7059 glass substrate/SnO_2/CBD CdS/CSS CdTe/Sputtered Cu/undoped graphite. $CdCl_2$ is evaporated over CdTe layer and given annealing treatment at 390^oC for 25 minutes. Cu is directly sputtered over the Te rich layer prepared with Bromine/Methanol solution with Cu thickness ranging from 10^oA to 80^oA. Then undoped Graphite is applied immediately and kept at room temperature for 5 hours before heat treatment. Annealing treatment is given

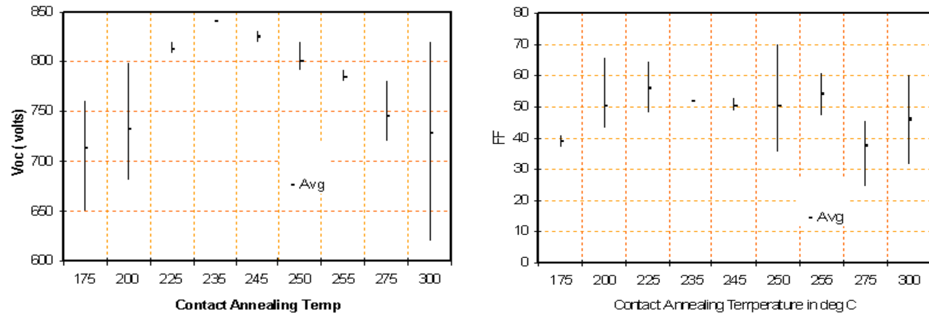
at different temperatures ranging from 200^oC to 275^oC for 25 minutes in He ambient. Silver and Indium are used as electrodes for back and front contacts respectively.

Fig.C.4 indicates the good contact formation as the thickness of Cu sputtered on CdTe increases. The series resistance is also reduced due to increase in Cu thickness. Main junction between CdTe and CdS is unaffected except for the Cu thickness of 80^oA. This indicates the Cu diffusion is not reached the junction enough to degrade the performance. Fig.C.5 gives the summary of average device parameters that get influenced by the Cu thickness and Contact Annealing. The open circuit voltage follows the linear decrease as Cu thickness is increased. Filling Factor(FF) is also decreased in general, as the thickness of Cu is increased.The device parameters in general reach optimum level for the contact annealing temperature of about 240^oC.

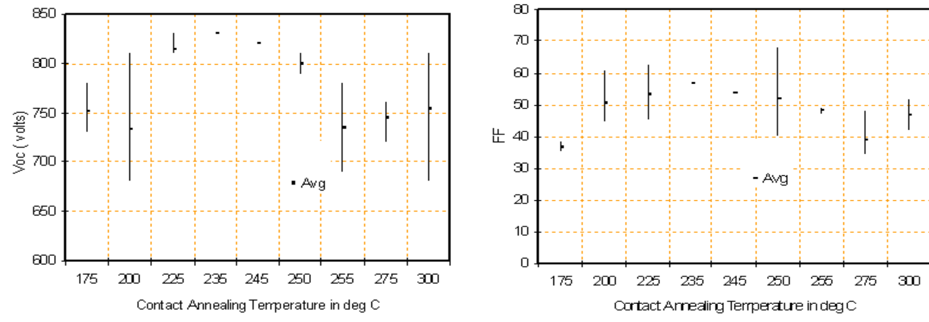
C.3 Effect of Copper on Degradation Behavior

The copper layer thickness over CdTe is varied intentionally to know its effect on device degradation.Copper acts as acceptor in CdTe. The increase in doping profile in the CdTe reduces back contact resistance. An increase in hole concentration in CdTe region increases the built in potential and reduces the saturation current, thereby increasing Voc.Copper diffuses into CdTe during contact annealing. Stressing under operating temperature provide redistribution of copper between the grain bulk and grain boundaries thus leading to change in carrier concentration in the bulk.Electromigration of copper dominates diffusion of copper. Cu_{cd} and $Cu - V_{cd}$ complexes are negatively charged and hence migrate in opposite direction to that of fast moving Cu_i^+. Due to slow diffusion and drift of negatively charged copper complexes, Cu_i^+ dominates in the initial stressing of devices. When device is stressed at OC, the depletion edge shifts towards CdS interface, as the built in potential is reduced. Hence probable advancement of copper towards CdS is expected. This in turn, decreases R_{sh}, Jsc and Voc[20].Voc is reduced drastically when copper thickness is increased and light soaked @ OC when compared with devices stressed at SC condition.This is shown in fig.C.6. The change in FF is shown in fig.C.7.

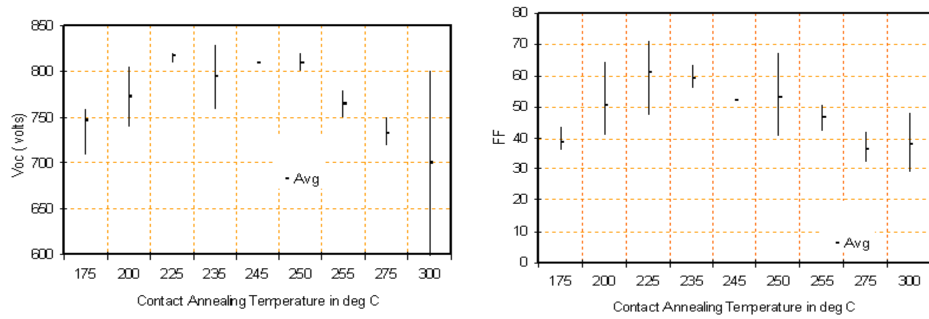
Tables C.1 and C.2 have the average estimates of the ratio of depletion width and acceptor concentration before and after LS for 40 Hrs. The values of devices heat treated(HT) at different temperatures after contact and with different Copper layer thicknesses over CdTe surface. The increase in annealing temperature and/or Cu thickness decreases the change in N_A and W_d during light stress. Doping profile derived from CV measurement as described in section 4.3. This profile is the representation of spatial distribution of holes in CdTe. Though the accuracy of doping profile is questionable as said in section 4.3, it visualizes the change in device behavior during stress to the extent. Figures C.8 and C.9 show the doping profile of devices LS @ OC and SC respectively. Doping level profile thus indicates the change in the



(a)



(b)



(c)

Figure C.1 Effect of Copper Concentration in Back Contact :a)0.05 gm b)0.1 gm c)0.2 gm of Copper in 10 gm of graphite respectively

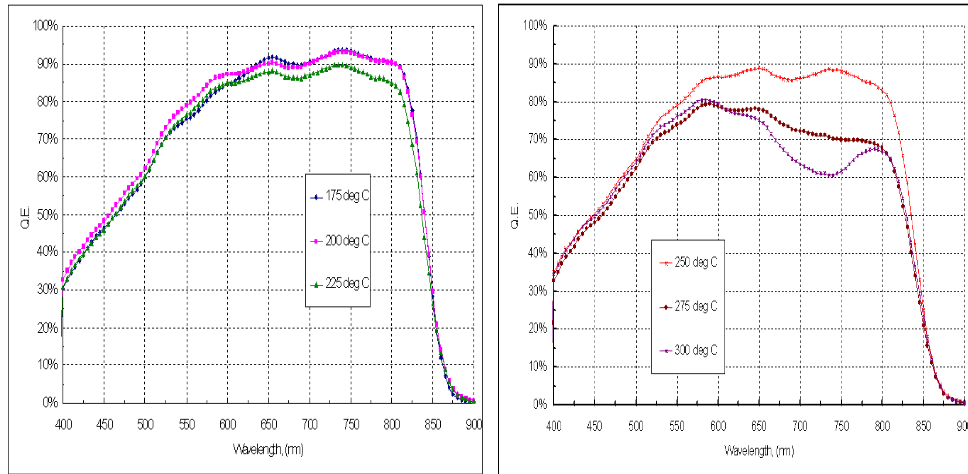


Figure C.2 Spectral Responses of Devices Made With Copper Concentration 0.2 gm in 10 gm of Graphite in Back Contact. Contact Annealing temperature in ^oC is given.

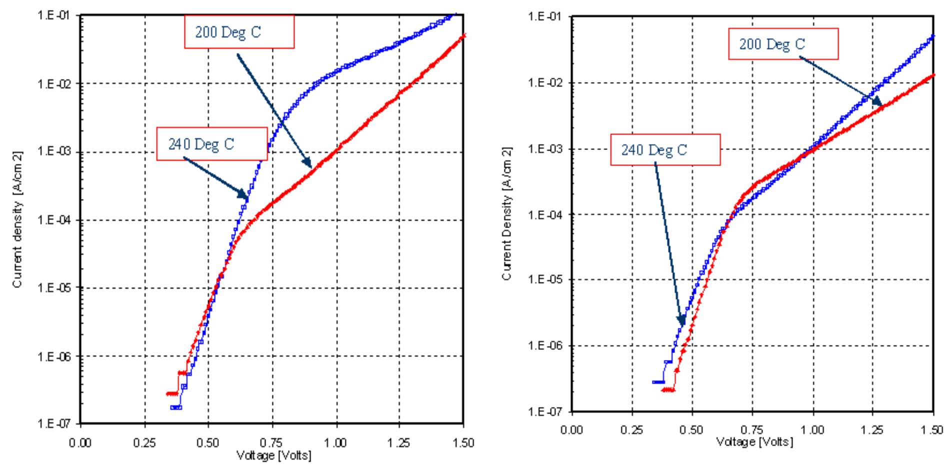
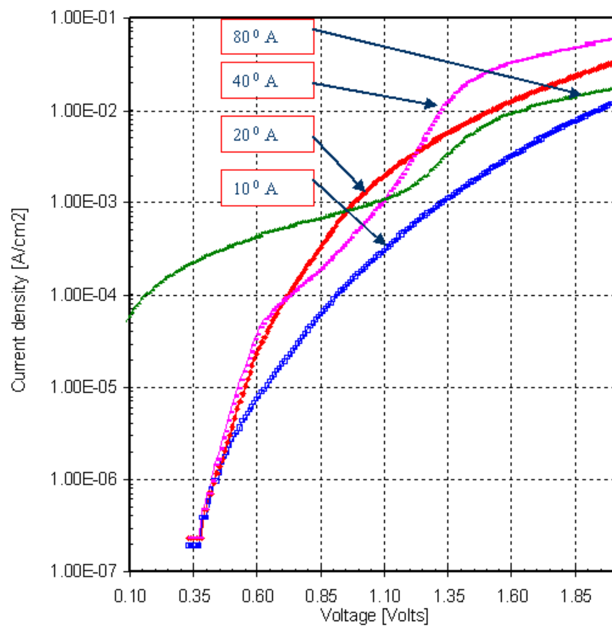


Figure C.3 Dark JV Curves of Devices with Copper Concentration : Left)0.05 gm and Right)0.2 gm in 10 gm of Graphite in Back Contact Respectively. Contact Annealing temperature in ^oC is also given.



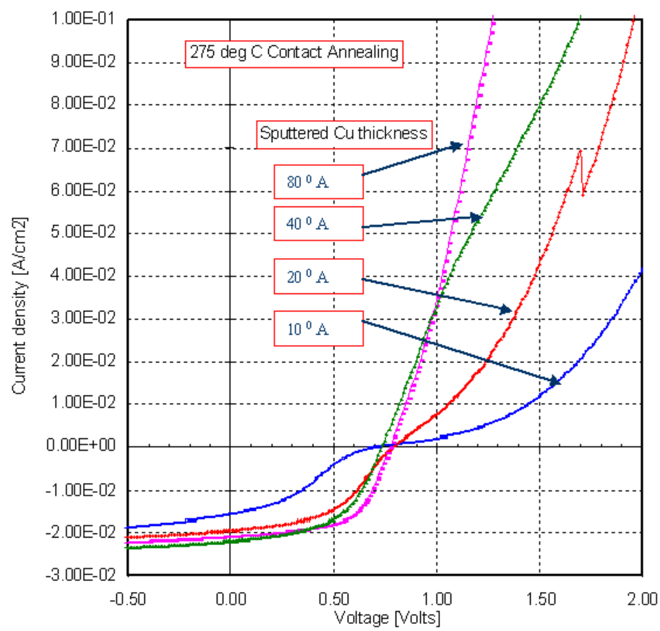
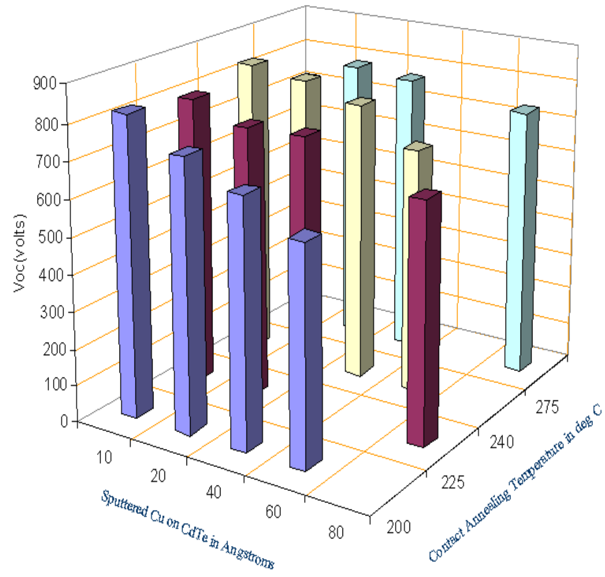


Figure C.4 Effect of Copper sputtered on CdTe layer : Top) Dark and Bottom) Light JVs.Sputtered Cu thickness is given in ^oA



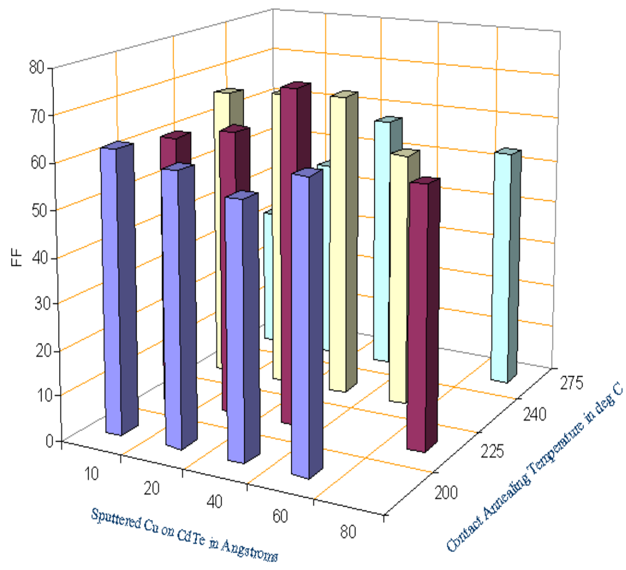


Figure C.5 Effect on Device Parameters (Average) due to Cu Sputtering on CdTe Layer for Different Contact Annealing Temperatures(^oC)

carrier concentration and profile in CdTe. Nearly flat doping profile in negative bias indicates the constant carrier concentration in the CdTe bulk region. The change in doping profile during stress period indicates the change in fermi level of CdTe, built in potential and even dominant carrier transport mechanism which in turn affects Voc, Jsc and Rsh.

Table C.1 Average Estimates of Depletion width (W_d) and doping level (N_a) changes after LS @ OC. Estimates are based on capacitance measurement at V=0V.Suffix b indicates before stress and a means after LS for 40 Hours

HT(^oC)	Cu Thickness(^oA)	$\frac{W_{d(a)}}{W_{d(b)}}$	$\frac{N_{a(a)}}{N_{a(b)}}$
175	5	1.07	2.49
240	10	1.11	1.15
240	40	0.76	0.82
275	40	0.31	3.75

Table C.2 Average Estimates of Depletion width (W_d) and doping level (N_a) changes after LS @ SC. Estimates are based on capacitance measurement at V=0V.Suffix b indicates before stress and a means after LS for 40 Hours

HT(^oC)	Cu Thickness(^oA)	$\frac{W_{d(a)}}{W_{d(b)}}$	$\frac{N_{a(a)}}{N_{a(b)}}$
175	5	1.05	1.48
240	10	0.89	1.09
240	40	0.86	0.76
275	40	0.32	4.05

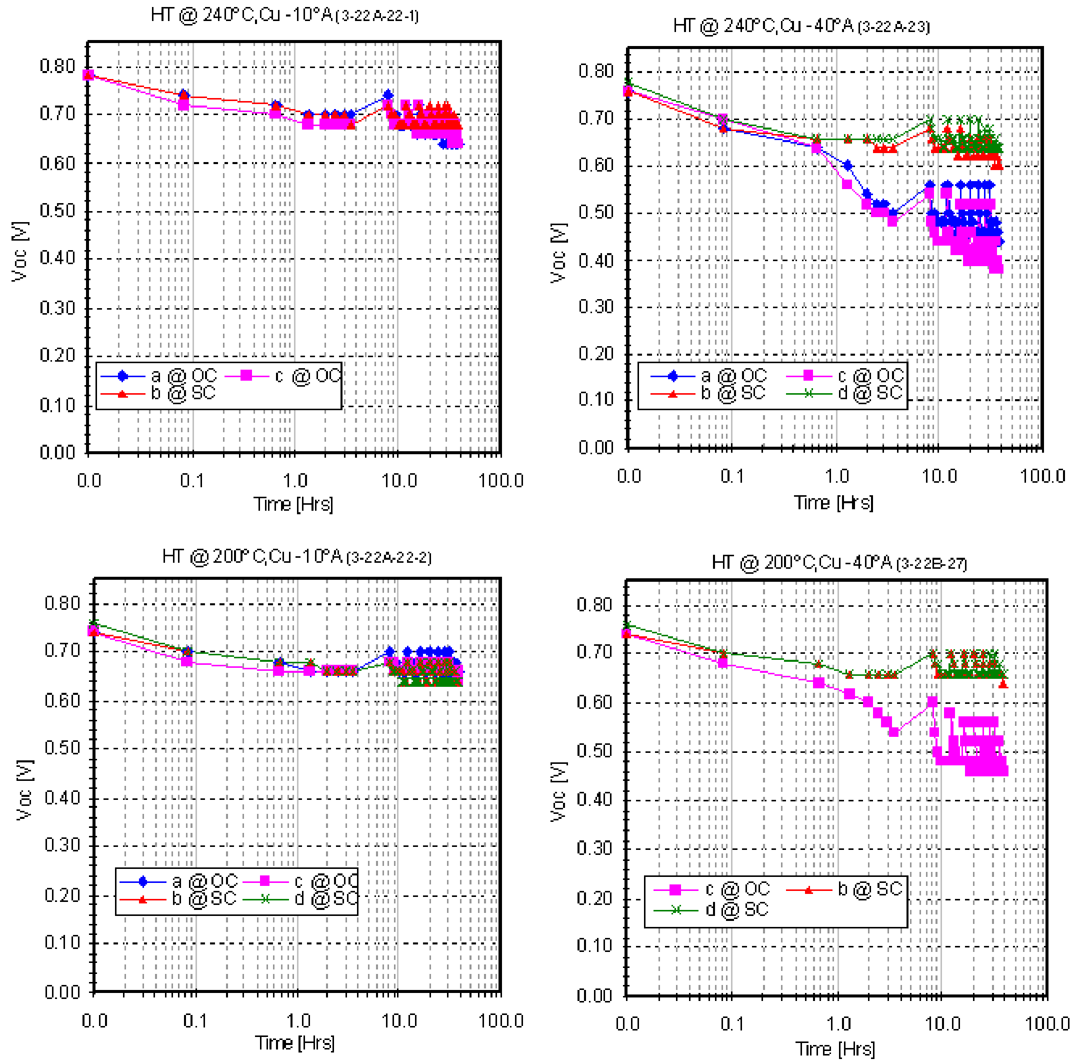


Figure C.6 Effect of Cu Thickness and Contact Annealing on Voc

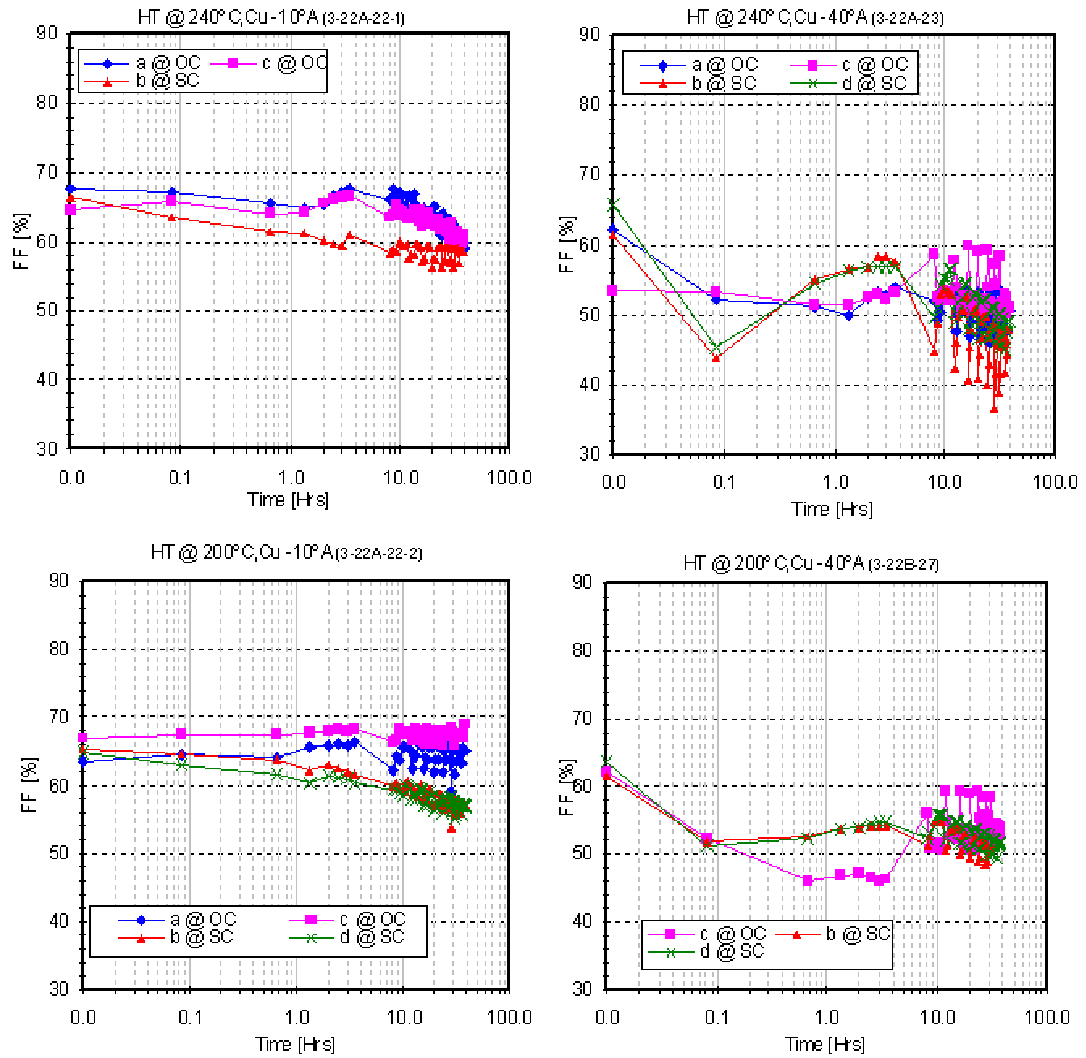


Figure C.7 Effect of Cu Thickness and Contact Annealing on FF

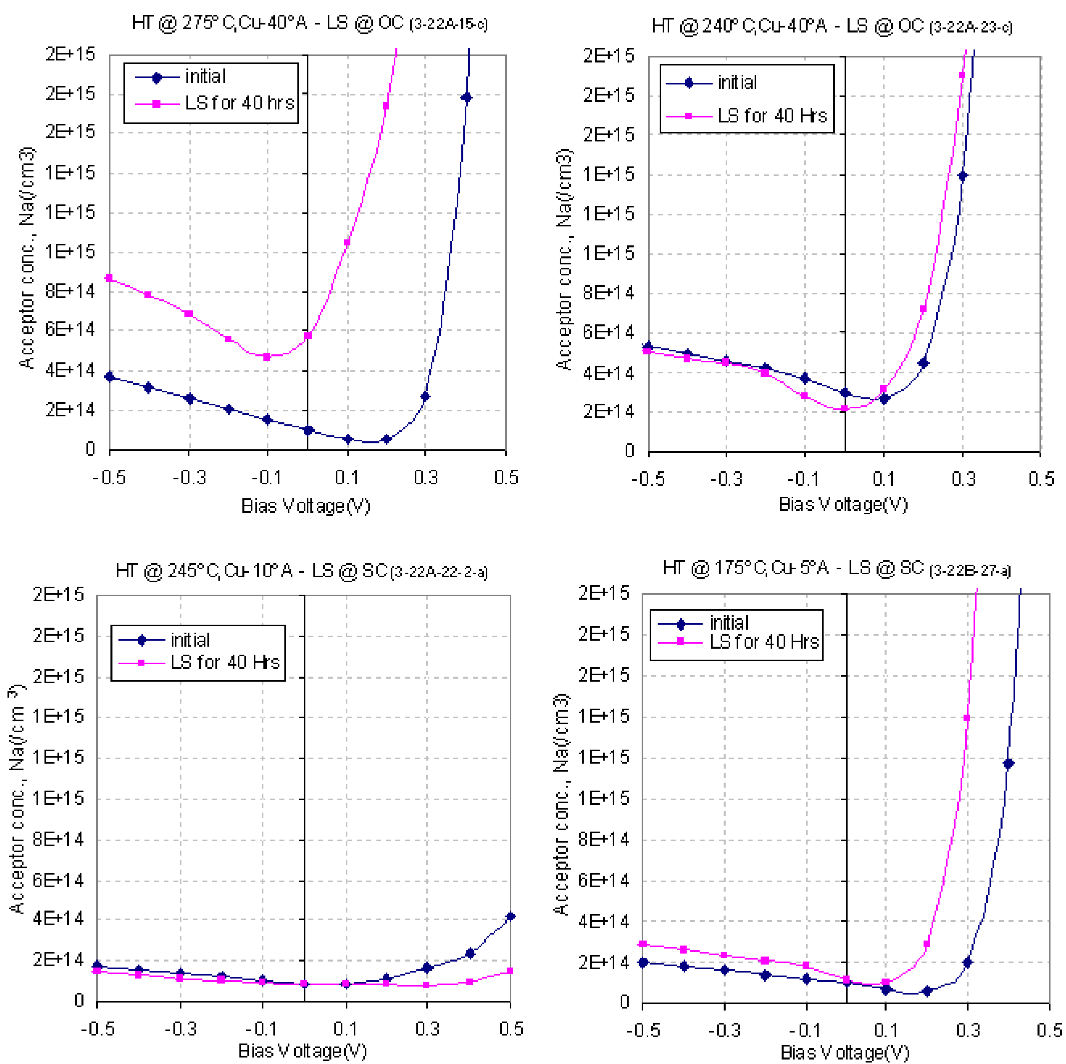


Figure C.8 Doping Profile for Samples LS @ OC

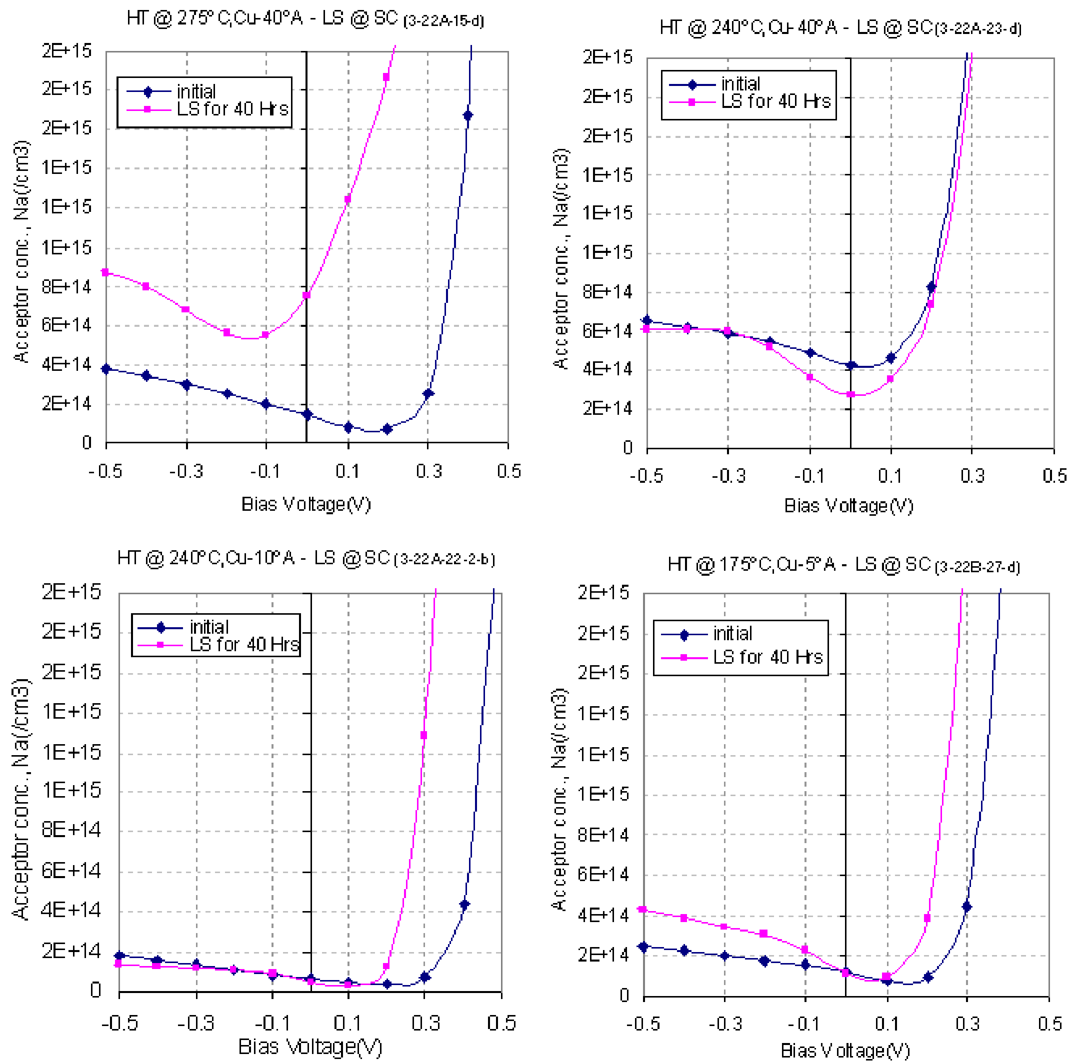


Figure C.9 Doping Profile for Samples LS @ SC