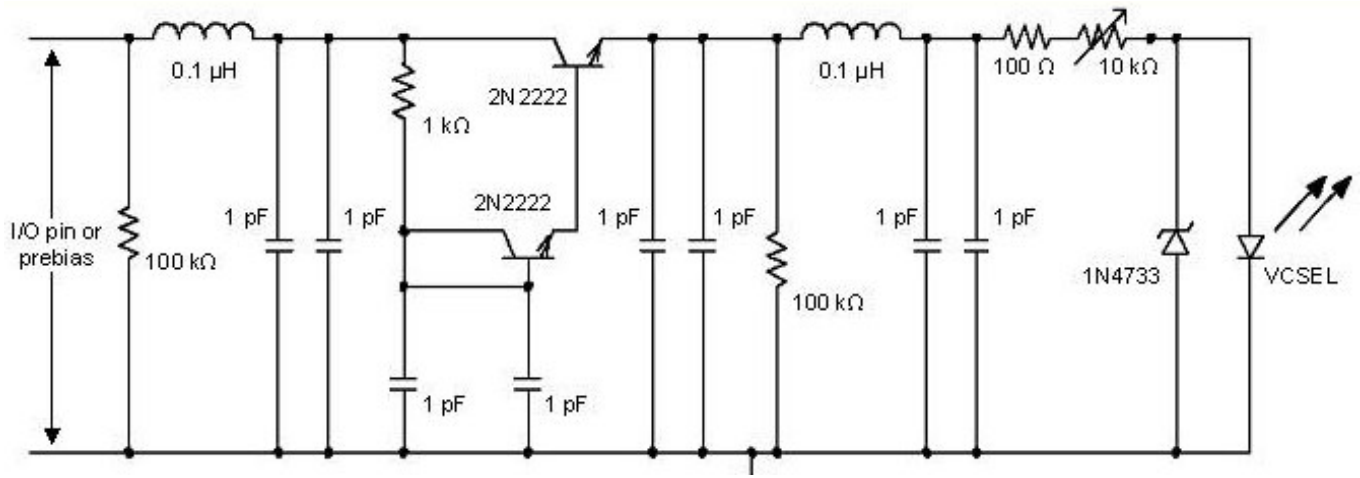
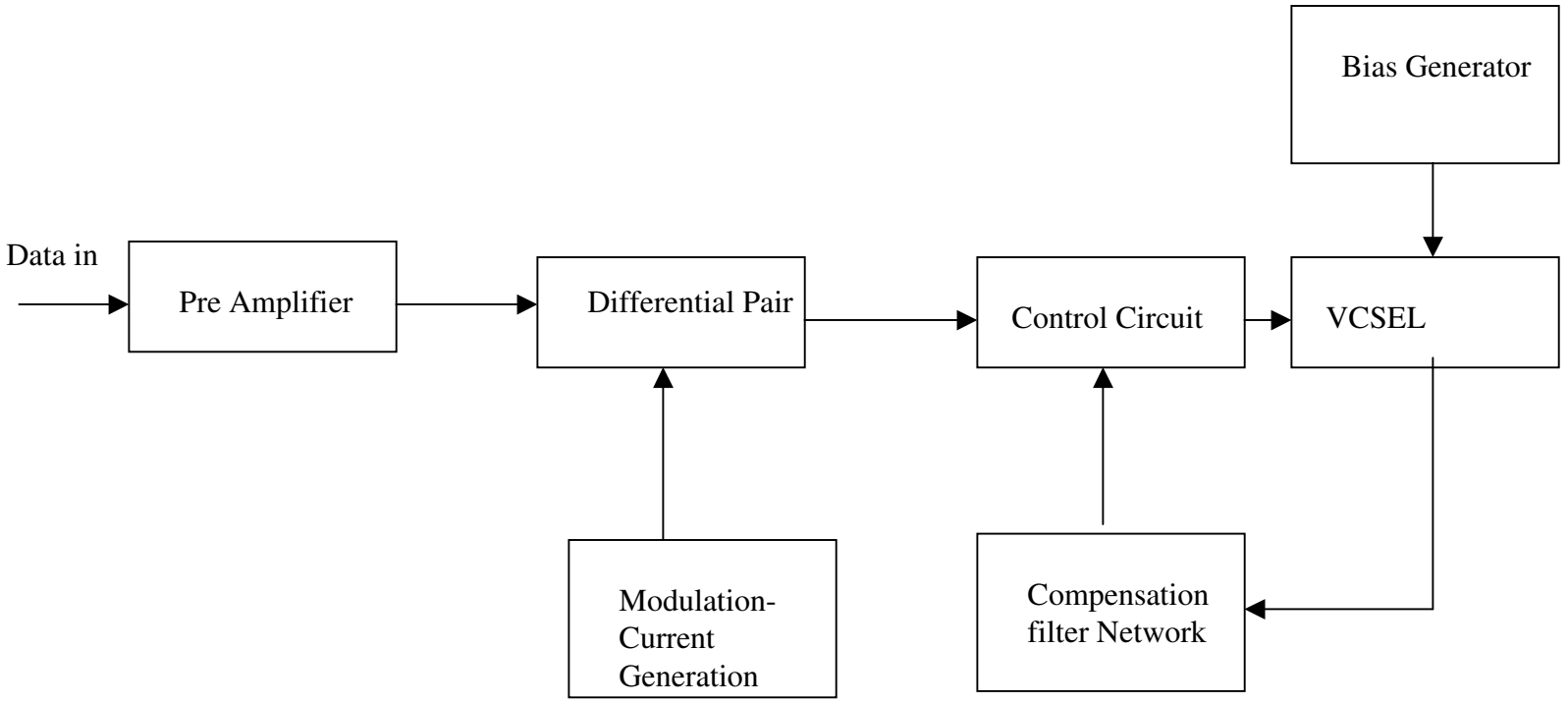
External Driver Circuit for VCSEL

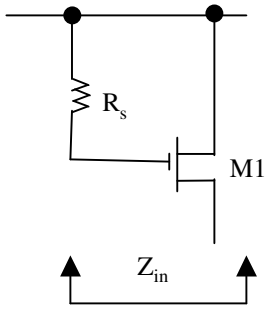


VCSEL Driver Architecture



Pre Amplifier

Active Inductor



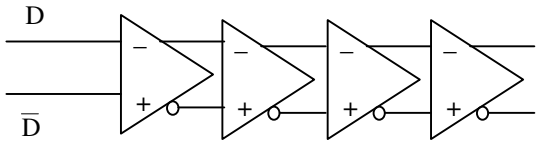
To behave as an inductor,

$$g_m > \frac{1}{R_s}$$

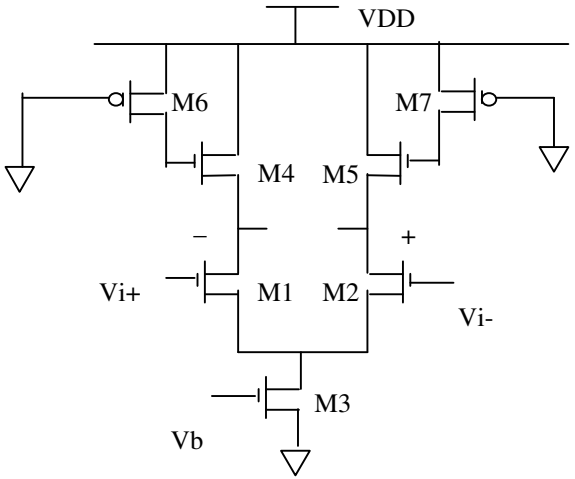
g_m is the transconductance of M1

Inductive Peaking - The inductive Load trim out the parasitic capacitance at the output node, thus high speed operation is achieved

4 Stage PreAmplifier



Structure of each stage



Conversion gain of each stage,

$$A_V = \sqrt{\frac{(W/L)_{M1}}{(W/L)_{M4}}}$$

Active Inductor is formed by nmos M4 and pmos M6 and M5, M7 pairs

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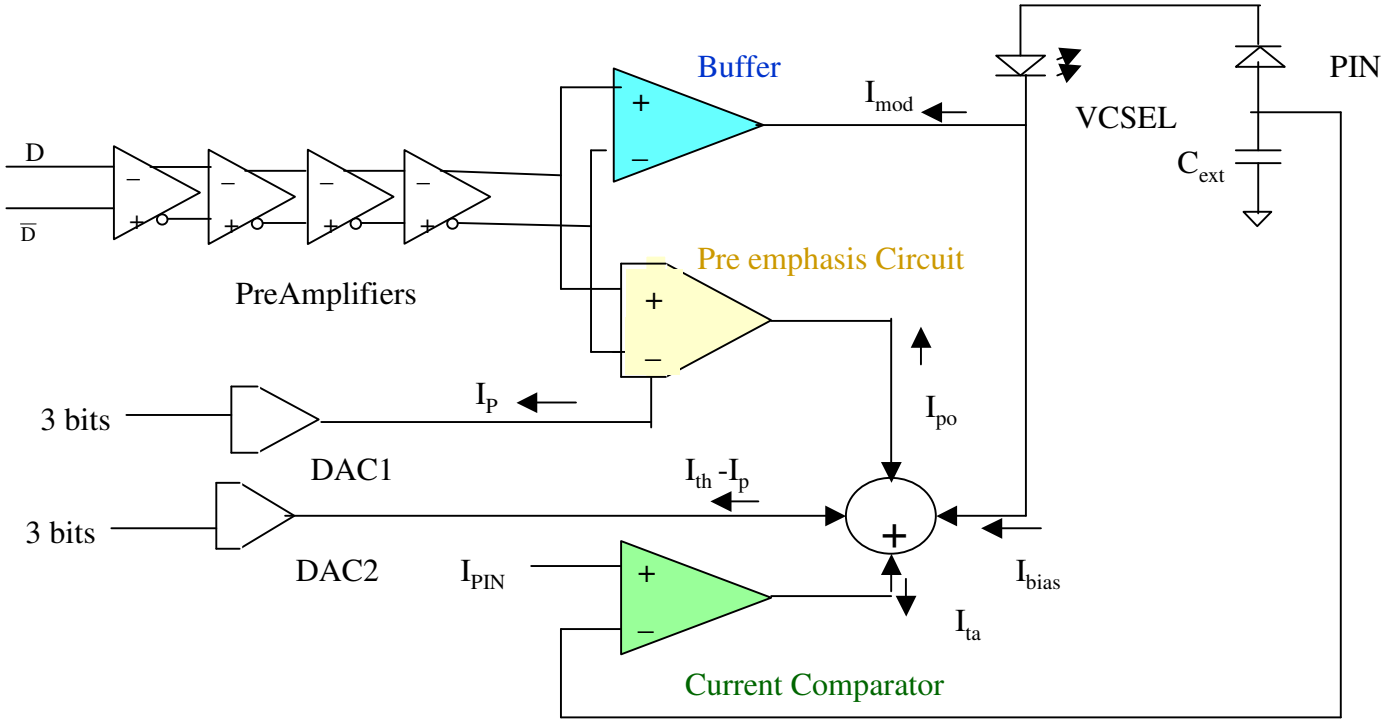
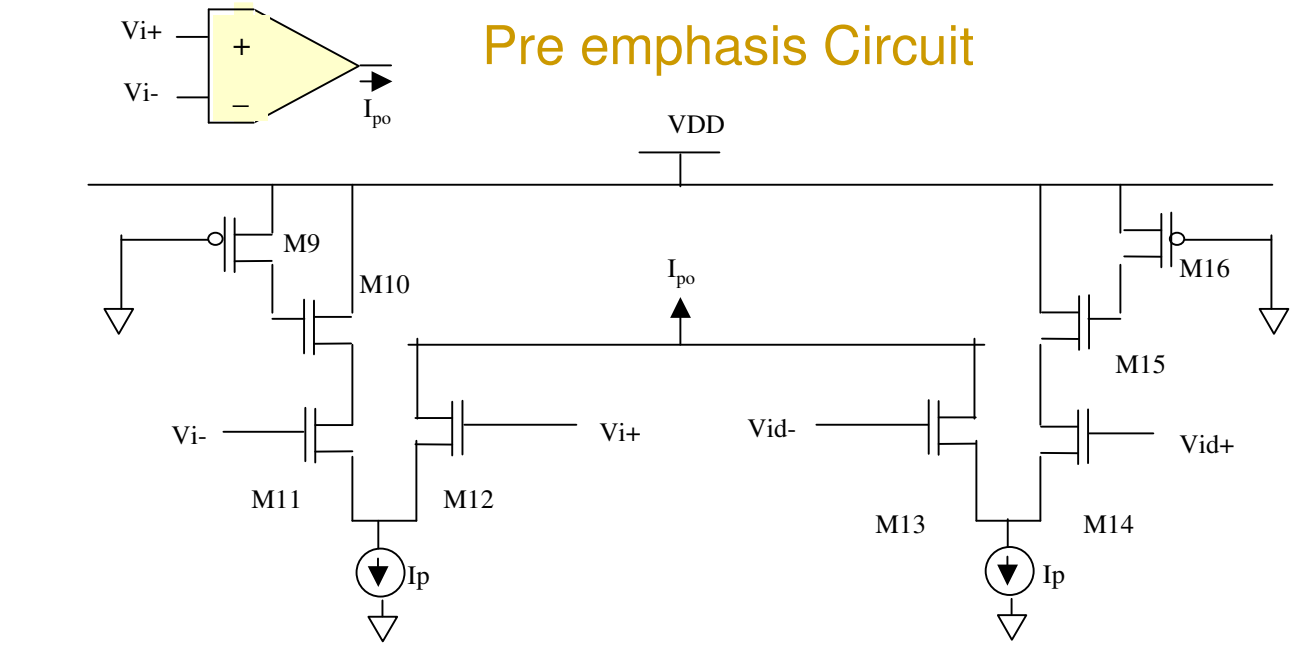
http://www.ap-asic.org/2002/proceedings/2A/2A-2.PDF

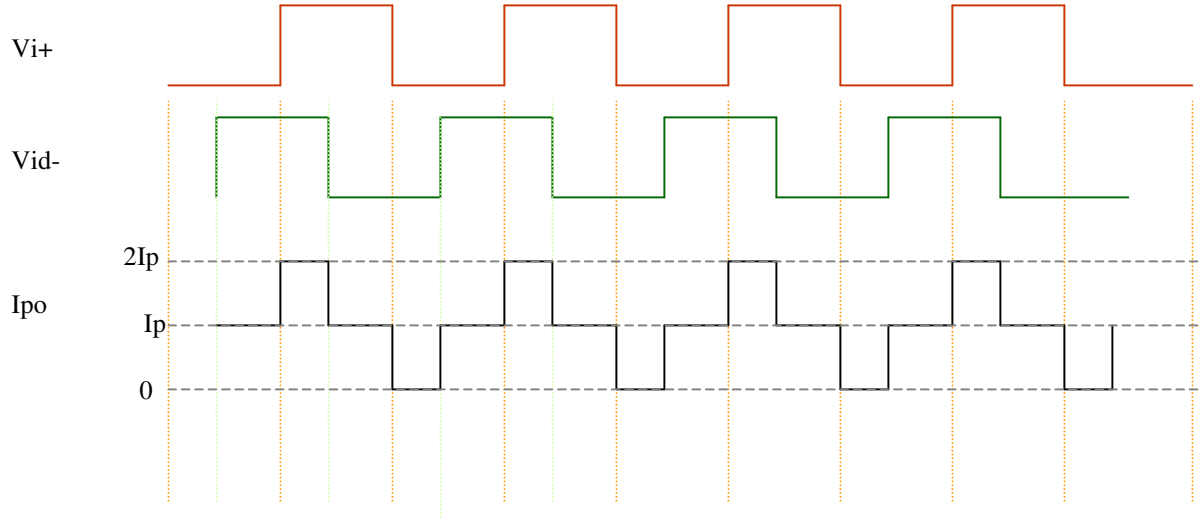
Laser Diode Driver Architecture



•Input signal is enlarged by preamplifier
•Drives Current Modulator (Buffer) which introduces large capacitive load
•Pre emphasis circuit detects transistion edge and generates Ipo to make DC biased current of Laser constant
•Current comparator generates Ita to compensate threshold current variation to make emitted output constant
•DACs act as reference current generators, DAC1 generates pre amphasis current and DAC2 generates DC biased current
•Thus bias current is programmable

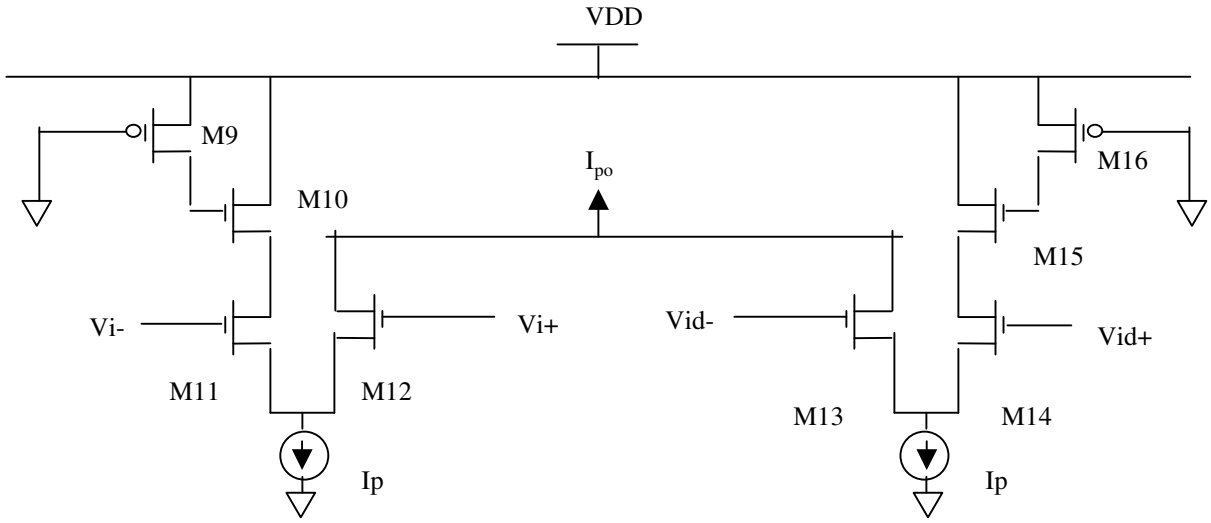
Pre emphasis Circuit



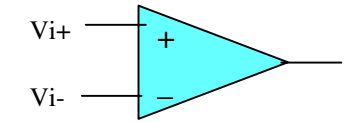


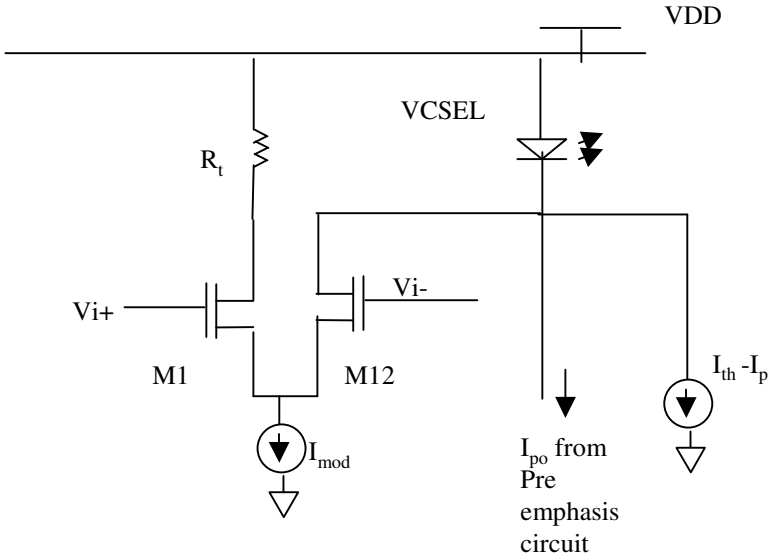
Vid is the delayed version of Vi
When input is unchanged, vi+ and Vd- are complementary, thus Ipo=Ip
On rising edge of Vi+, Ipo= 2Ip
On falling edge of Vi+, Ipo=0

Preamphasis Circuit



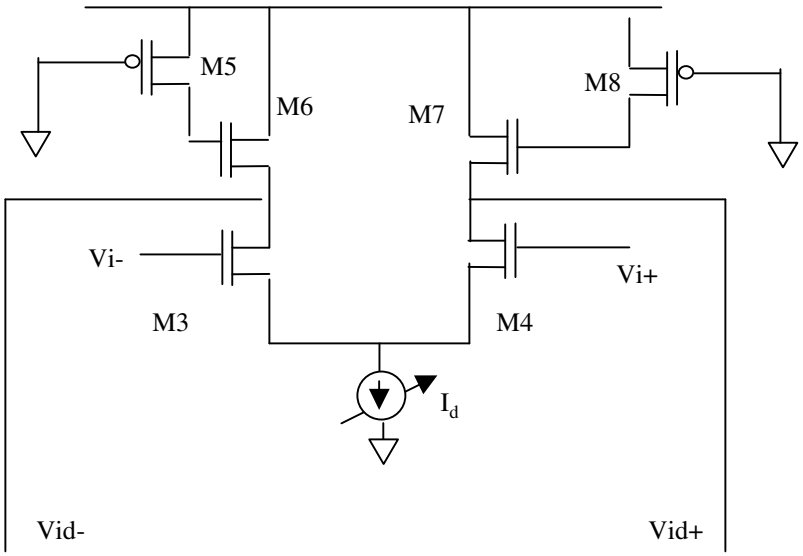
Buffer





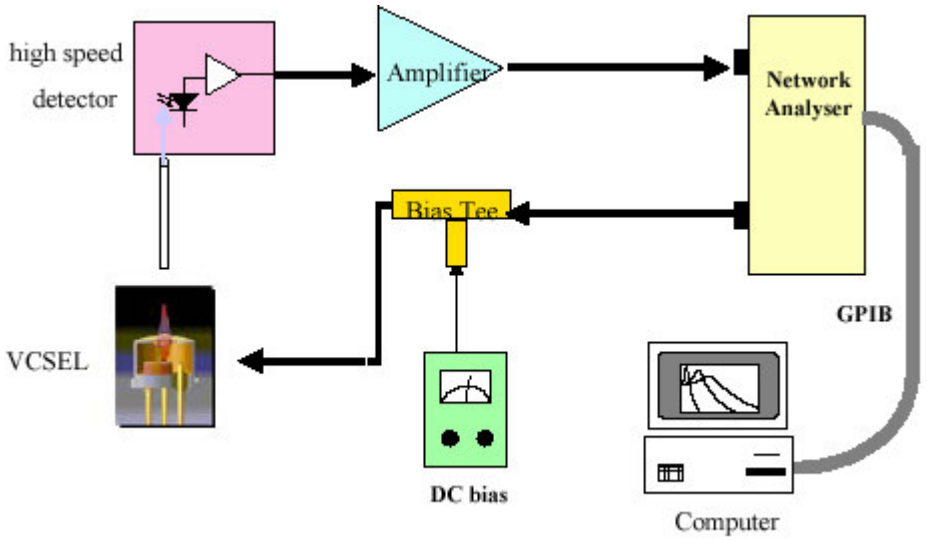
External Resistor Rt(50 ohms) is added to match the load(VCSEL)

Delayed input Vid to Pre emphasis Circuit



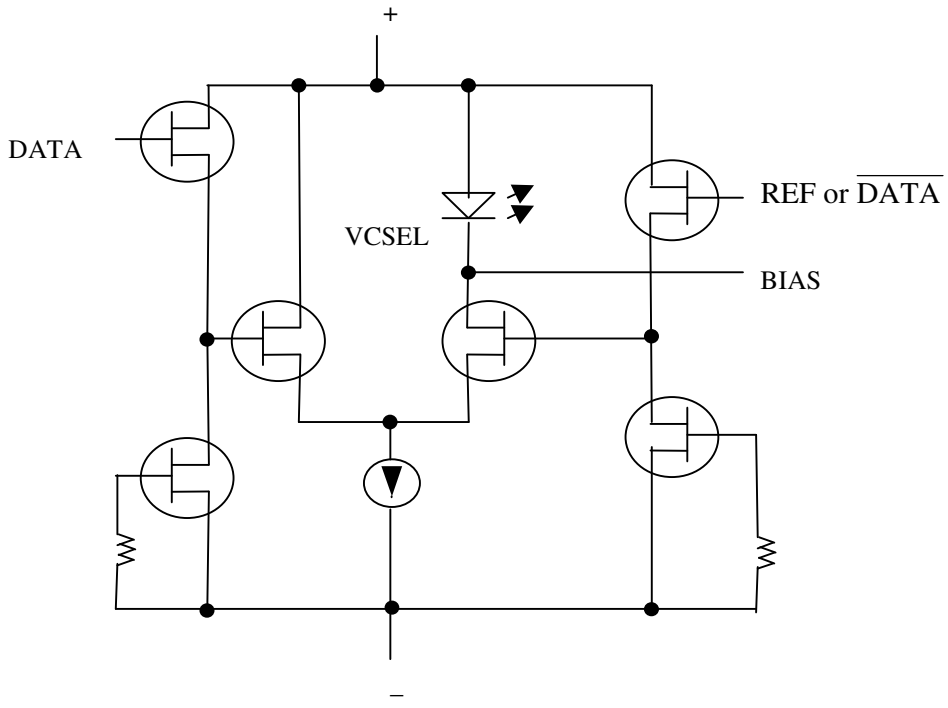
Id can changed to preset the delay difference between Vid and Vi

Setup for Modulation Response Measurement of VCSEL



Simplified Driver Circuit

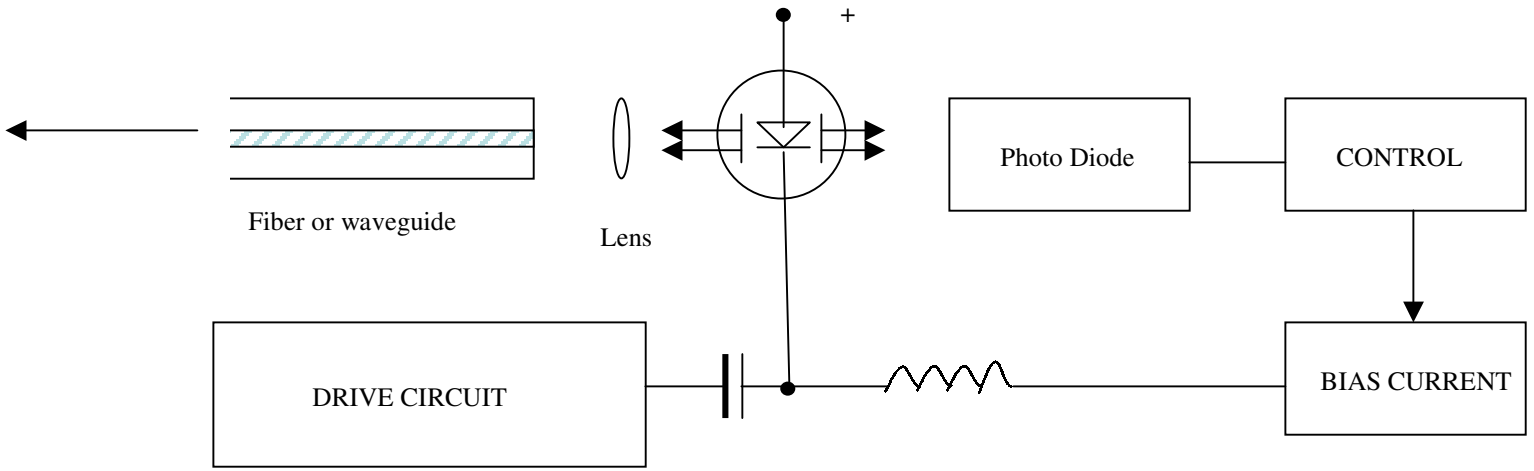
- Function of driver circuit is to convert an ECL level input voltage swing into a current swing to drive the VCSEL
- It generally has a laser dc bias control circuit and feedback circuit to keep the average power output constant
- Main component is the differential pair of transistors one of which has VCSEL
- The gate bias at the transistor connected in series with differential pair is used to control the total current



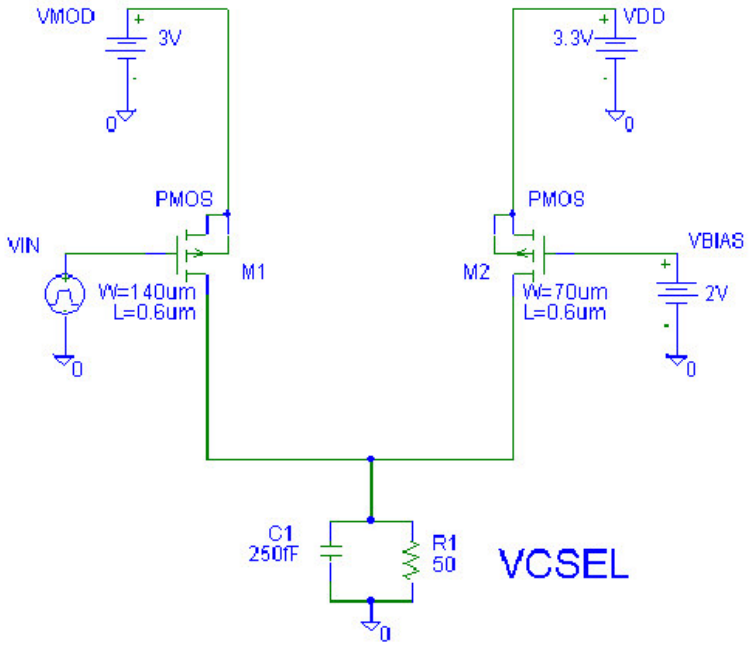
M.O. Manasreh, VCSELs: Technology and Applications, pp 163-167

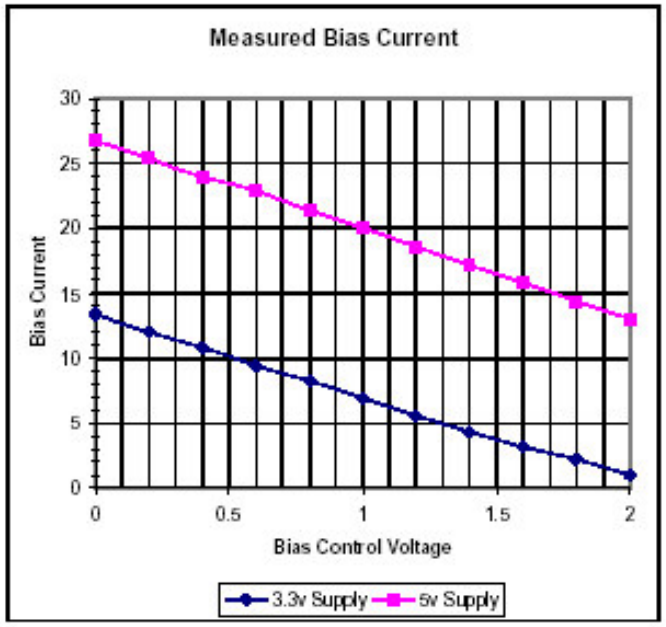
Transmitter Schematic

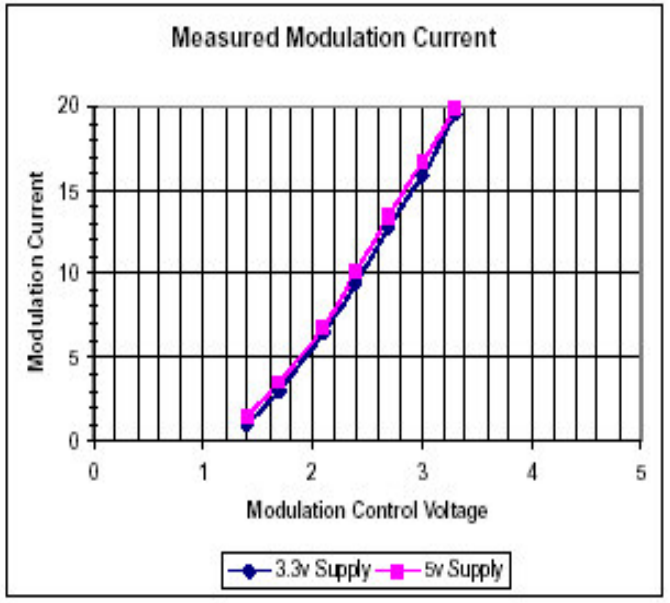
- For surface emitting laser array, two additional sets of similar lasers are fabricated on the array chip, the output of which is used to stabilize the output of elements of the array, if it varies with temperature or ageing



A 500MHz, 10-Channel CMOS VCSEL Driver IC with built-in self-test and on-chip clock generator circuitry



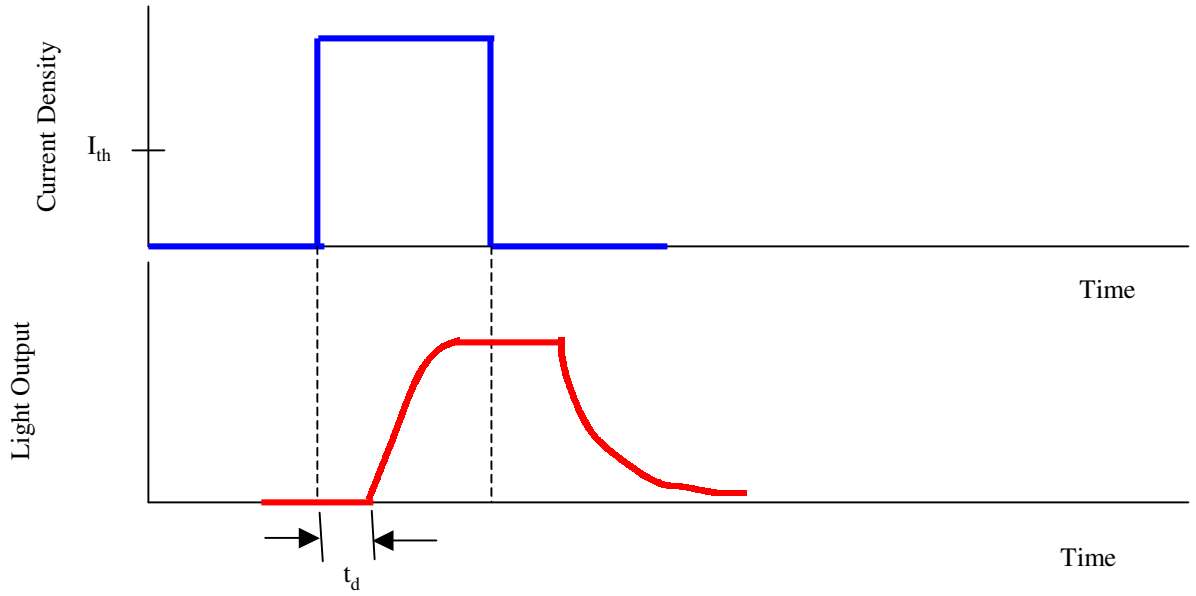




Power Supply	3.3 V Supply	5 V supply
Speed	400 MHz	500 MHz
Max Bias Current	10 mA	20 mA
Max Modulation Current	20 mA	40 mA

Optical Link 59
Ashok Rangawamy http://www.oida.org/JOP/us-new/interfaces/10drivers-spec.pdf
(Directed by: Dr. V. K. Jain)

Response to Current Density Step Excitation



With the application of current pulse, the carrier density increases from n_i to n_f in a time interval t_d

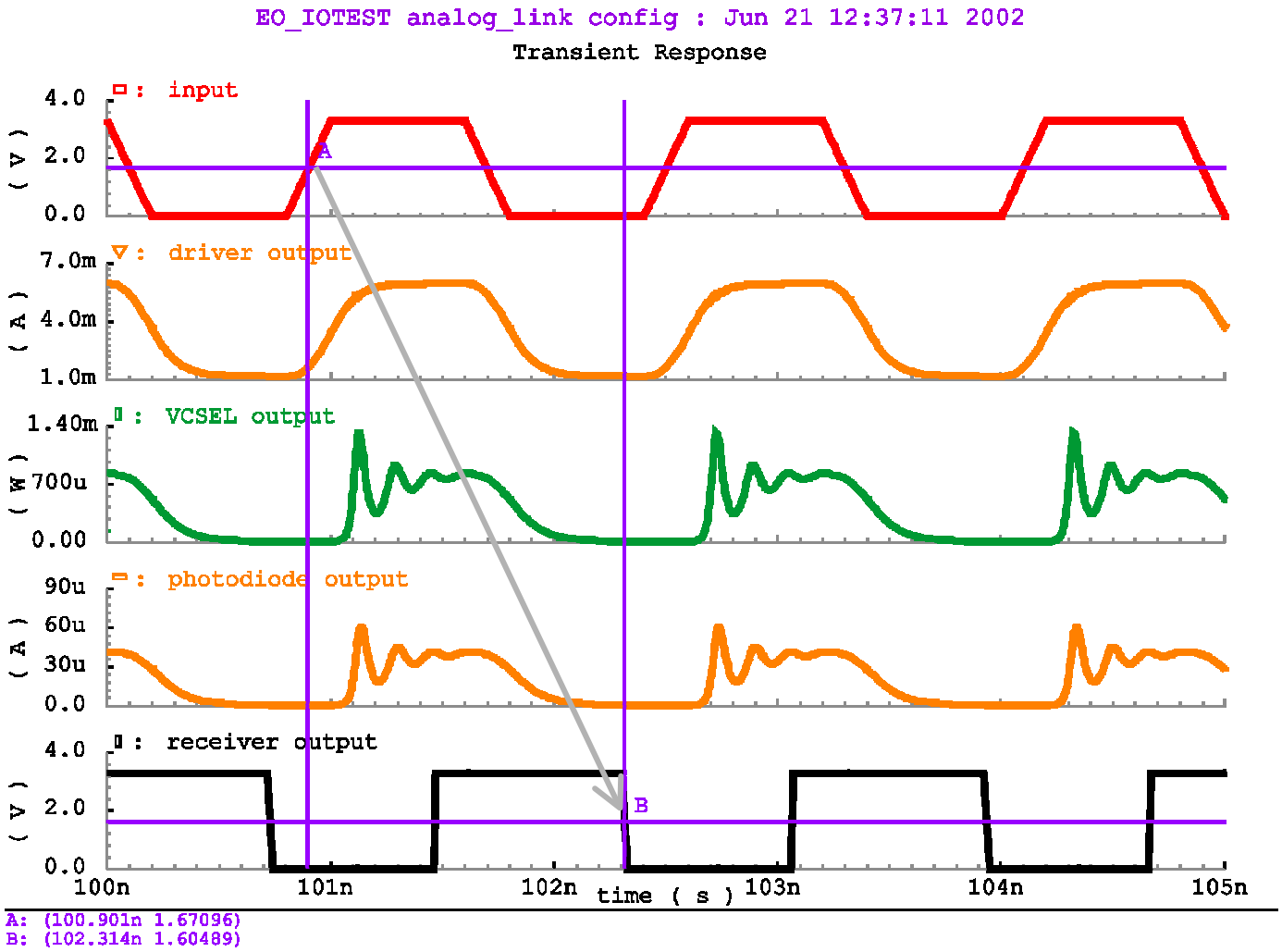
$$t_d = \tau \ln\left(\frac{I - \frac{qdn_i}{\tau}}{I - \frac{qdn_f}{\tau}}\right)$$

Which can be written as,

$$t_d \approx \tau \ln\left(\frac{I}{I - I_{th}}\right)$$

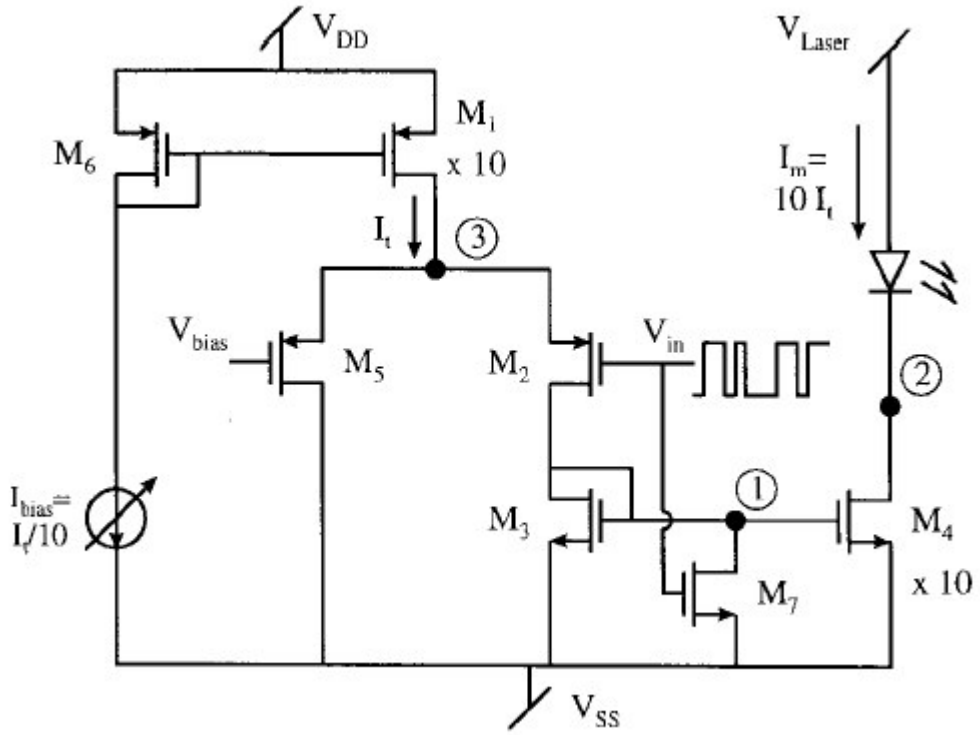
Simulation example: transient

1 link with 10dB attenuation in the optical path



Low Power 1 Gb/S CMOS Laser Driver for a zero bias modulated Optical Transmitter

- Differential pair and current mirror at output stage
- Low power achieved by zero bias modulation and additional current mirror
- It eliminates threshold-biasing DC circuitry
- Current mirror reduces static current of differential pair



Driver's Power Consumption is given by

$$P = I_t(V_{DD} - V_{ss}) + \frac{1}{2} I_m (V_{Laser} - V_{ss})$$

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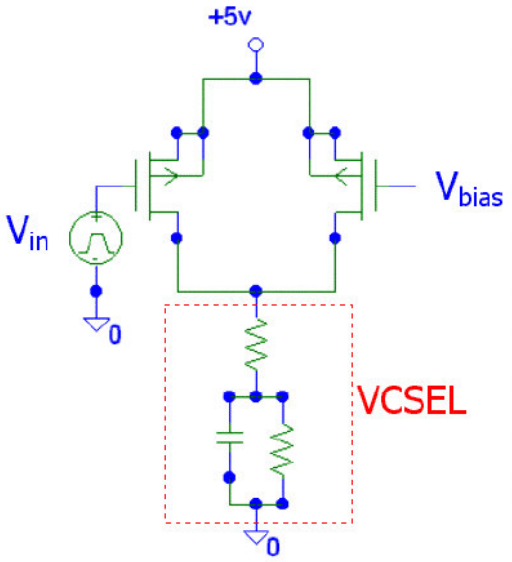
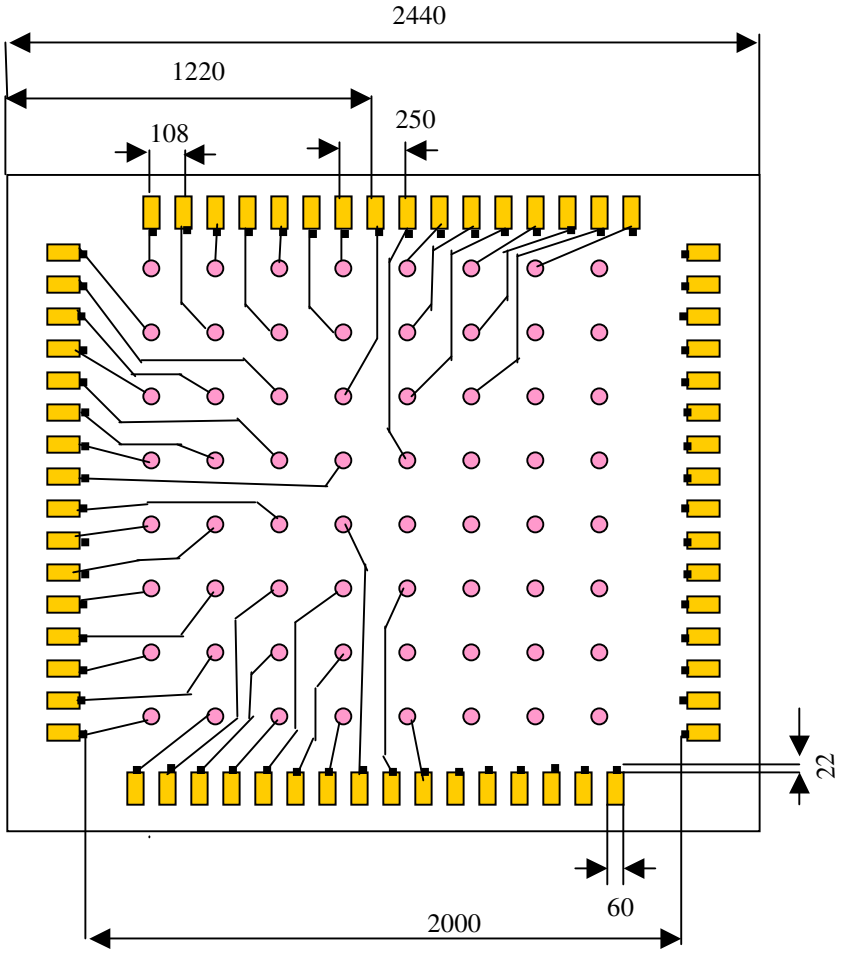
VCSEL Driver for 8X8 Array



- Two shunt-connected PMOS transistors have been used as switched current sources to drive the VCSEL.
- One of the PMOS transistors provides the quiescent current into the VCSEL.
- The quiescent current can be controlled by the voltage Vbias. The other PMOS provides the modulated drive current into the VCSEL.
- The drive PMOS is modulated by the input TTL signal Vin.
- The sizes of the two PMOS transistors have been optimized for speed and modulation current.
- The driver operates with a reverse logic. If the quiescent current is set to zero, a logic HIGH input to the driver completely switches OFF the corresponding VCSEL.
- A logic LOW input to the driver results in a drive current into the VCSEL of 3.5 mA.

FUJI Xerox 8X8 VCSEL Array



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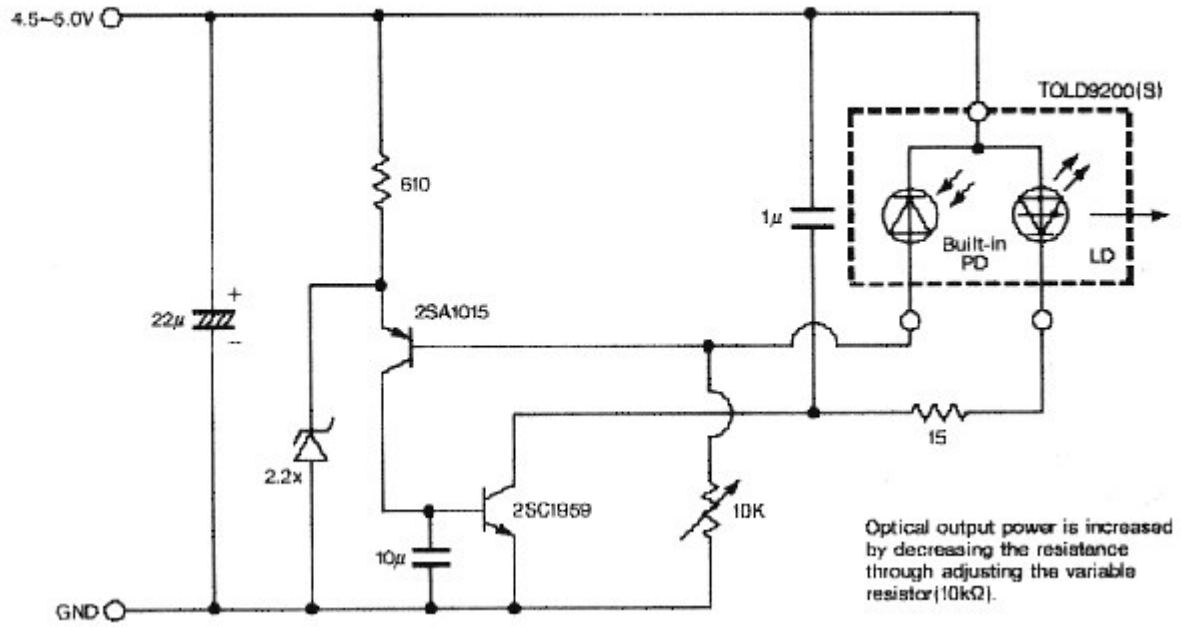
FUJI Xerox 8X8 VCSEL Array

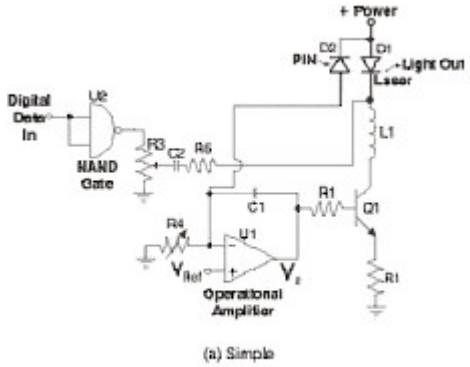
Parameter	Test Condition	Symbol	Value	Units
Optical Power Output	maximum	Po	4	mW
Threshold Current		I_{Th}	0.5(1-2)	mA
Non-Uniformity of Output Power	I_F=5 mA		10	%
Peak Wavelength	I_F=5 mA	ë	850(840-860)	nm
Series Resistance	I_F=5 mA	Rs	50-70	Ohms
Beam Divergence	Po=2 mW, Full width	è	20-30	deg

Simple Laser Diode Driver Circuit

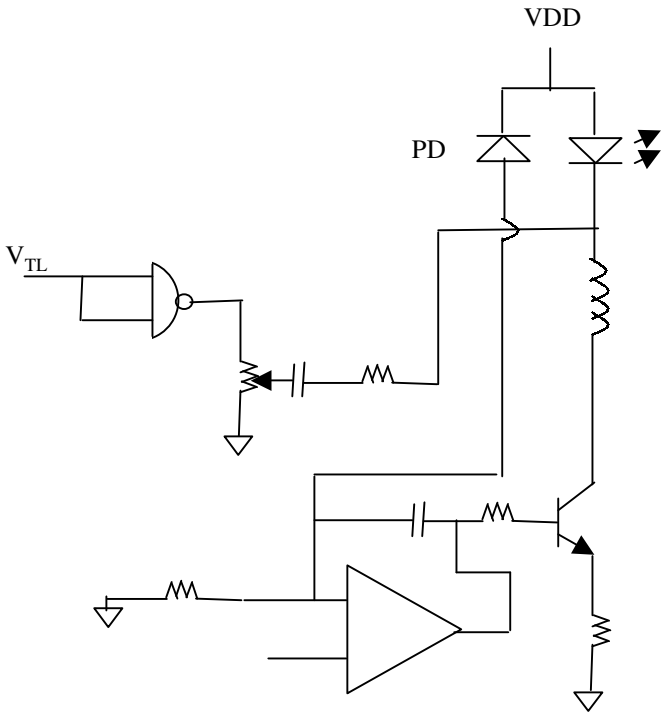


ftp://ftp.ee.ualberta.ca/pub/cookbook/optic/laser.gif

Simple Digital Laser Driver



(a) Simple



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Modulation Bandwidth

- The characteristic specification of a modulatable laser describing its pulse bandwidth is modulation Bandwidth.
- VCSELs are known to have intrinsic modulations bandwidth in excess of 25 GHz
- ULM Photonics – 850 nm VCSEL – 3 dB Modulation Bandwidth is 8 GHz at optical power output of 2 mW
- Maximum modulation Bandwidth per laser for an array of 12 VCSELs flip chip bonded,
  is 9.3 GHz at 0.6 mA drive current for 5.4µm diameter VCSEL at 77K.
- It decreases with increase in temperature (8.3 GHz at 300K).
- To obtain higher bandwidth, parasitic and internal capacitances should be reduced
- To reduce internal capacitance due to thin oxide aperture in the laser, tapered apertures are proposed[1]
- **3dB Modulation Bandwidth:**
  The Frequency at which the Modulating Frequency Deviation decreases to 0.707 of its DC value.

1. http://www.ucop.edu/research/micro/96_97/96_050.pdf

Differential Carrier Life Time

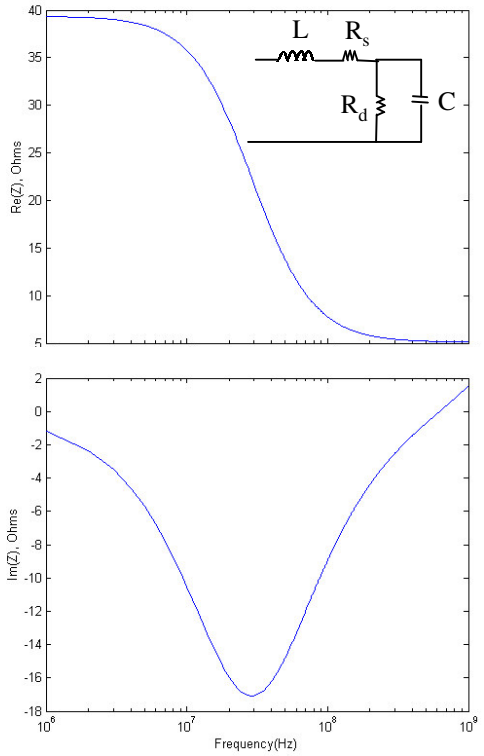
Example

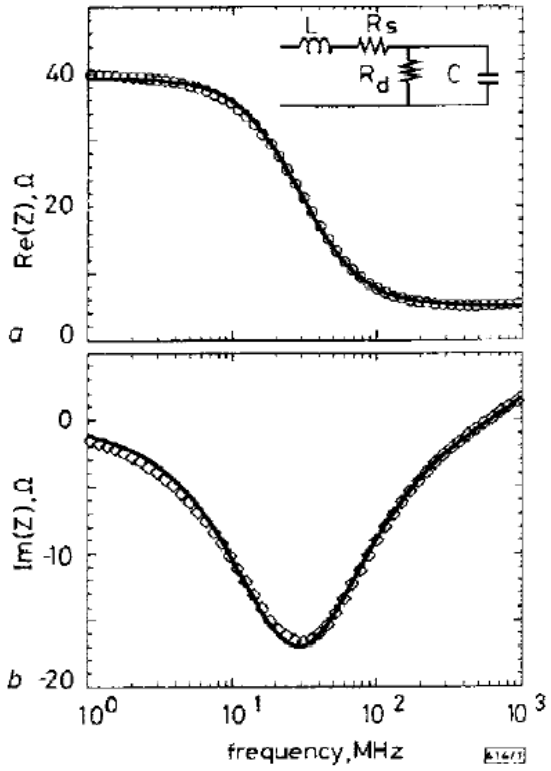
$L = 0.4\text{nH}$ $R_d = 5.1\Omega$

$R_s = 5.1\Omega$ $\tau_d = 5.4\text{ns}$

Total Impedence of LASER equivalent circuit

$$z(\omega) = j\omega L + R_s + \frac{R_d}{1 + j\omega\tau_d}$$





True carrier lifetime measurements of semiconductor lasers
Shtengel, G.E.; Ackerman, Elect. Letters.(1747-1748)

Laser Parameters

Photon group velocity v_g

$$v_g = cn_g$$

where n_g is a group refractive index of the quantum well material
c is the speed of the light

$$n_g = n - \lambda \frac{dn}{d\lambda}$$

n is the refractive index
ëis the wavelength

Cavity Loss ã

cavity loss is defined as total internal loss of a laser due to absorption and scattering

$$\gamma = \frac{1}{L_{eff}} \ln R$$

R is the reflectivity of DBR mirror, assuming Top and bottom mirrors have same reflectivity

Example

Photon group velocity v_g

For GaAs, $n_g = 3.6$

$$v_g = 3\times10^8 \times 3.6 = 10.8\times10^8 \; m/\sec$$

Cavity Loss ã

$$\gamma = \frac{1}{380\times10^{-4}} \ln(0.32)$$
$$= 30/cm$$

$R = 0.32$
$L_{eff} = 380$ ì m