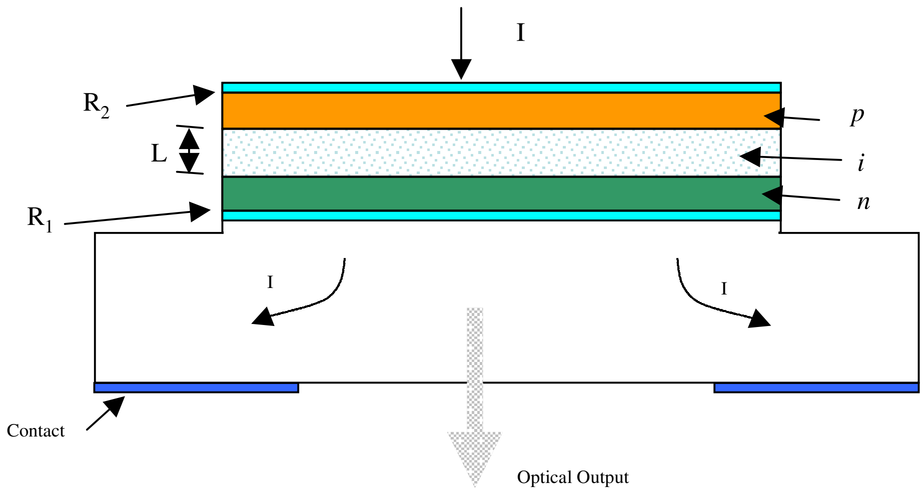
Operating Principle

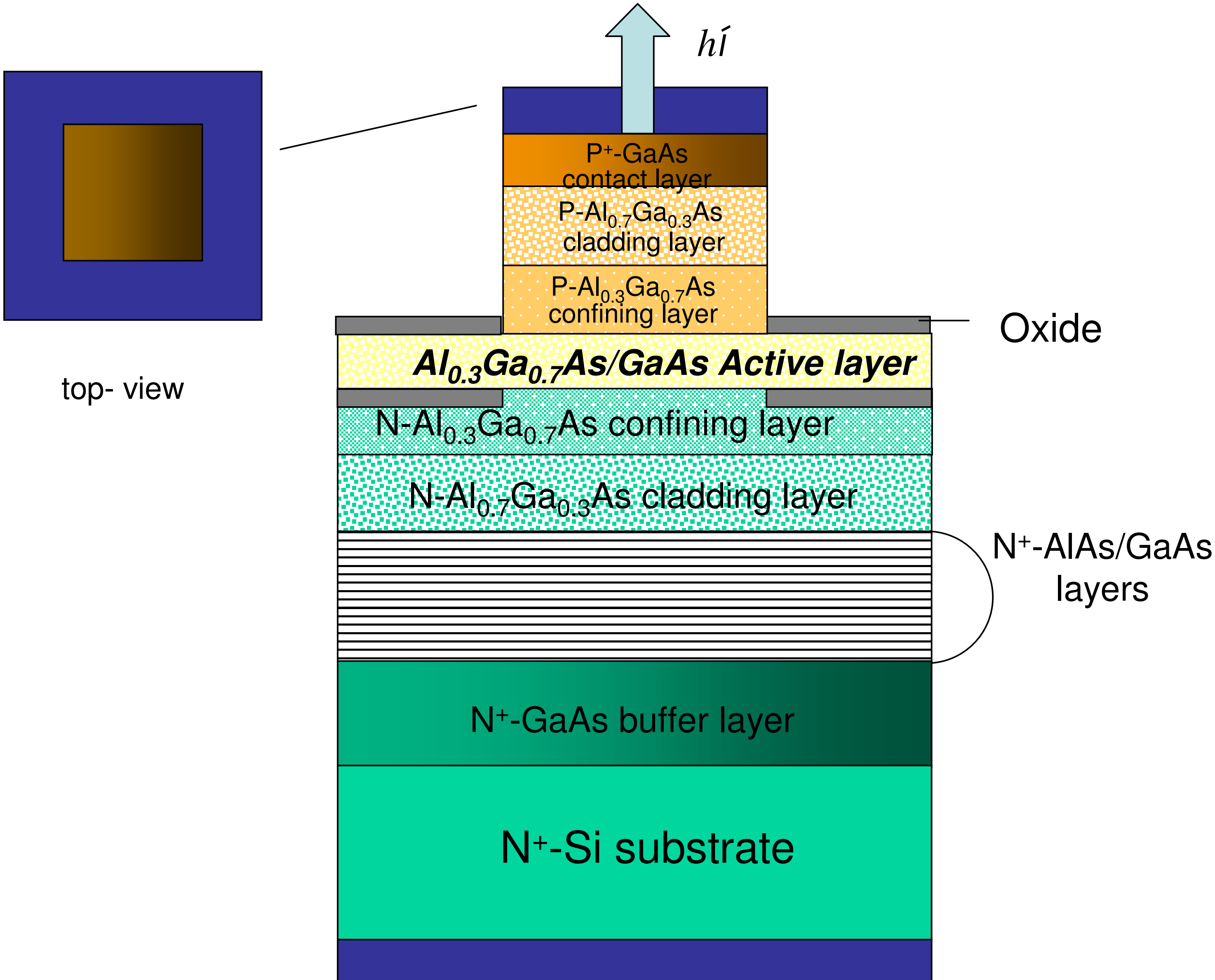


- Current is injected vertically into p-i-n active layer of length L, Cavity mirrors with reflectivities R1 and R2
- For an electromagnetic wave travelling in through a region with gain g, the photon density grows with distance as,

$$\rho(\mathrm{x}) = \rho_0 e^{(g-\alpha)x}$$

where α is absorption coefficient (due to optical loss)

Schematic Cross section of an AlGaAs/GaAs VCSEL grown on a Si substrate



Threshold Gain

Threshold gain, where losses due to absorption and the mirrors are just overcome,

$$g_{th} = \alpha + \frac{1}{2L\Gamma} \ln \frac{1}{R_1 R_2}$$

Let

$$\text{L} = 5\ \mu\text{m (maximum limit due to cost and time)}$$

$$\text{g}_{\text{th}} - \alpha = 1000\ cm^{-1} (Maximum\ \text{ when } \alpha = 0)$$

Confinemen t Factor, $\Gamma = 1.0$

Assume

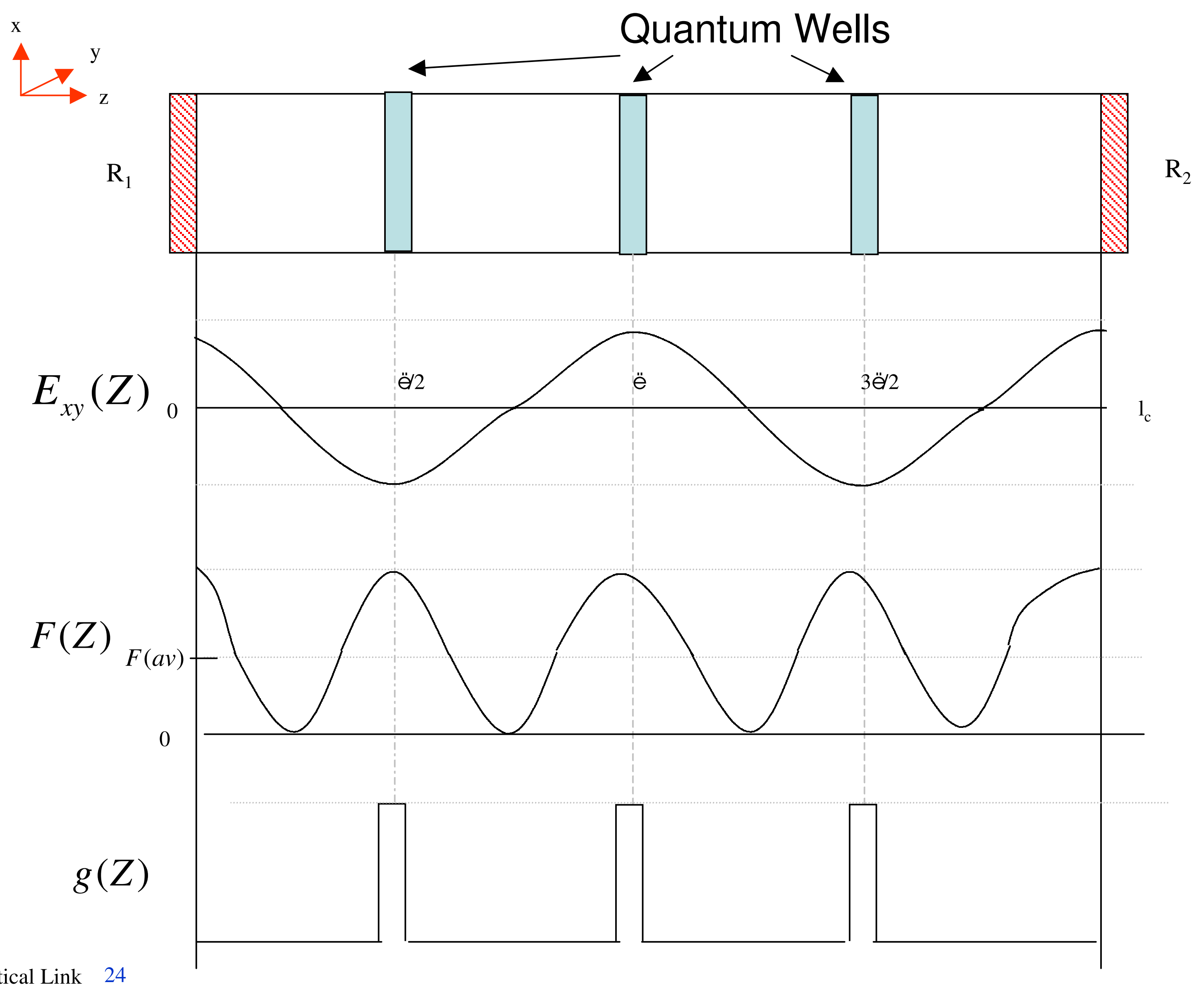
$$\text{R}_1 = \text{R}_2 = R$$

Then

$$\text{R} = 0.61$$

This can be provided by metallic reflectors

Standing Wave in the Active Region



Ashok Rangawamy
(Directed by: Dr. V. K. Jain)

Simplified Threshold Condition

Time averaged Field Intensity of a standing wave,

$$F(Z) = \frac{2c}{\eta\omega} n_r \sqrt{\varepsilon_0} E_0^2 \cos^2(\beta z)$$

$$F(av) = \frac{c n_r \sqrt{\varepsilon_0}}{\eta\omega} E_0^2$$

The nodes occur at $\lambda/4, 3\lambda/4, ...$ and antinodes at $\lambda/2, 3\lambda/2...$

Normalized magnitude of optical Standing wave,

$$F_n(Z) = \frac{1_c \left|E_{xy}(Z)\right|^2}{\int \left|E_{xy}(Z)\right|^2 .dz}$$

If the gain regions are split and placed at the antinodes of the standing wave, the spatial variation of gain,

$$g(Z) = \sum_{i=1}^{N} L.g'.\delta\left(Z - \frac{\lambda}{2}\right)$$

Where L is the extent of the gain region at each antinode and N number of quantum wells in active region

Threshold condition for a VCSEL along Z direction,

$$\int F_n(Z) g_{th}(z) dz = \frac{1}{2\Gamma} \ln\left(\frac{1}{R_1 R_2}\right)$$

Example

The gain has a value g_t in the wells and α, the cavity loss, exists elsewhere
If there are N quantum wells, each of width d, and Γ_1 is the longitudin al confinemen t factor, which depends on placement of the wells with respect to standing wave pattern,
then thres hold Condition becomes,

$$\Gamma_1 g_{th} Nd = \alpha l_\alpha + \frac{1}{2\Gamma}(1 - R_1 R_2)$$

Let $\Gamma = 1$

$\Gamma_l = 2$

Losses are minimal. ie, αl_α is neglected.

$g_{th} = 1000\, cm^{-1}$

$d = 100\ \overset{0}{\mathrm{A}}$

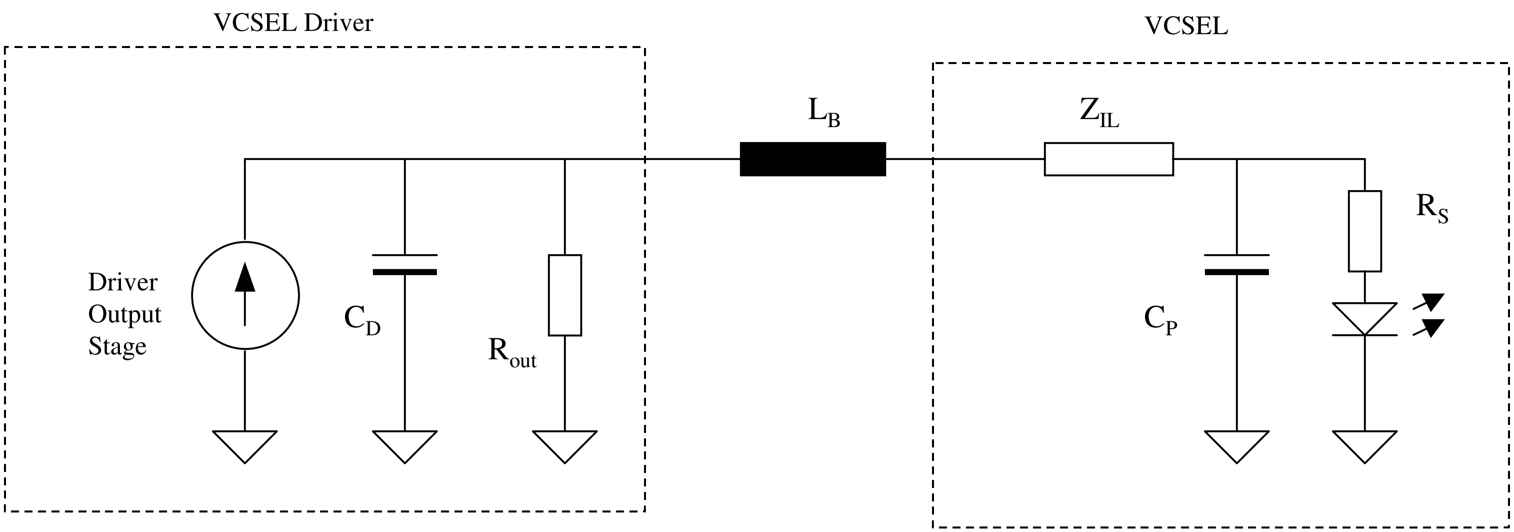
$N = 1$

Then $R_1 R_2 = 0.996$

If $R_1 = R_2 = R$,

$R = 0.998$

Equivalent Circuit

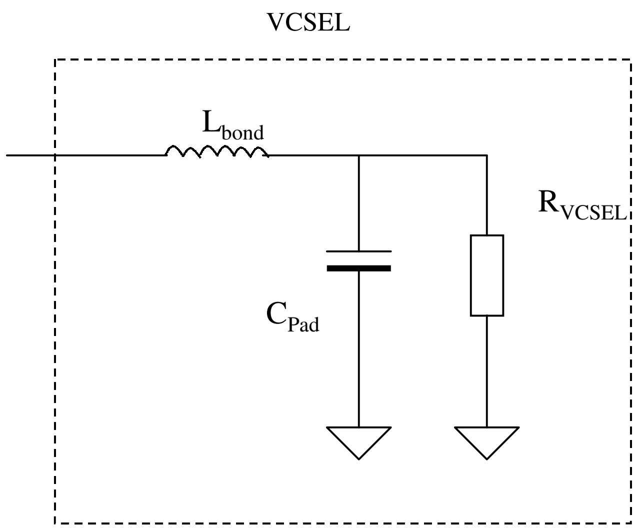


$$C_{tot} = C_D + C_p$$

$$R_{tot} = \frac{R_s R_{out}}{R_s + R_{out}}$$

$$\text{Parasitic Response } B_{3dB} = \frac{1}{2\pi R_{tot} C_{tot}}$$

Above Threshold die-level Model

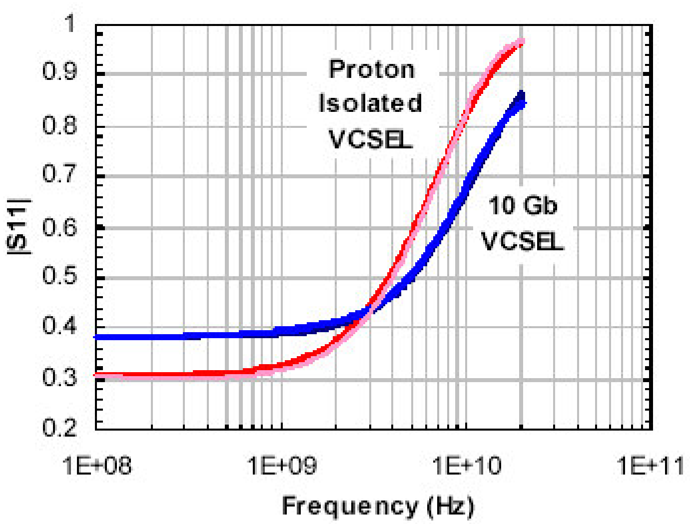


For Standard proton implanted device,

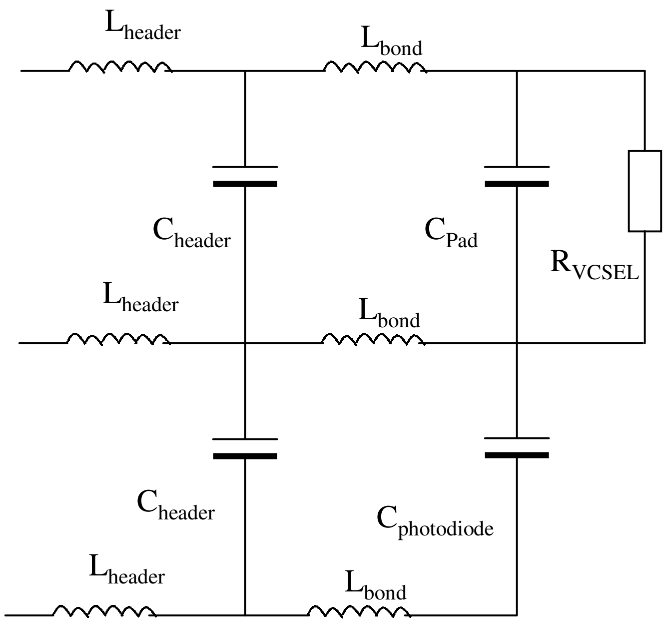
$$L_{bond} = 100\ pH$$
$$R_{VCSEL} = 29\,\Omega$$
$$C_{pad} = 0.8\,pF$$

For small diameter oxide VCSEL optimized for 10 GB,

$$L_{bond} = 100\ pH$$
$$R_{VCSEL} = 120\,\Omega$$
$$C_{pad} = 0.8\,pF$$



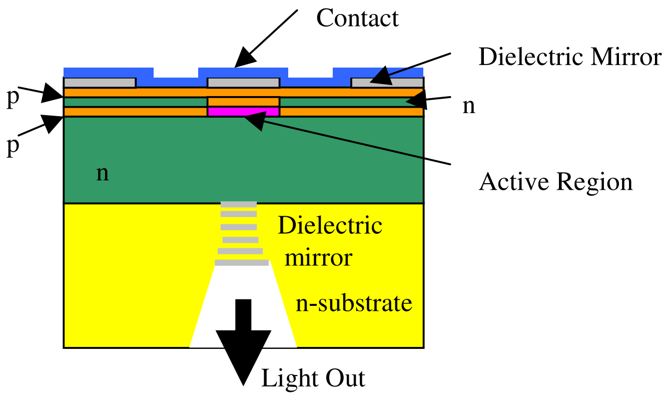
Package VCSEL Interactions



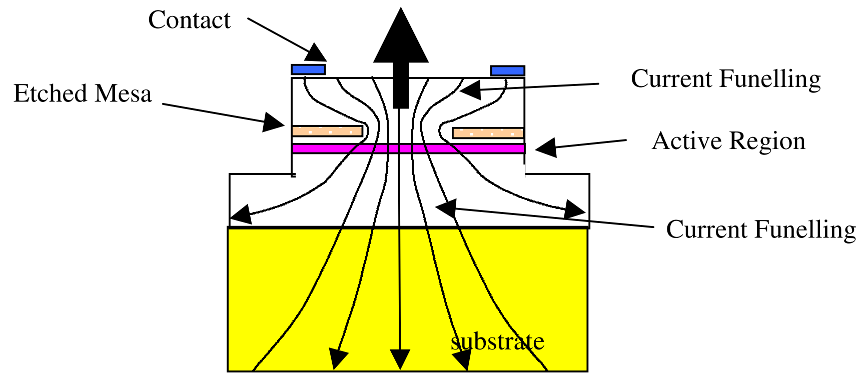
$$L_{bond} = 1nH$$
$$L_{header} = 0.5nH\ /mm$$
$$R_{VCSEL} = 29\,\Omega$$
$$C_{pad} = 0.8\,pF$$
$$C_{header} = 0.5\,pF$$
$$C_{photodiode} = 1\,pF$$

Small Signal Equivalent circuit of a VCSEL packaged with a photodiode on a HoneyWell TO46 header in a common cathode configuration

Device Geometries for VCSEL Devices



a) Etched Well

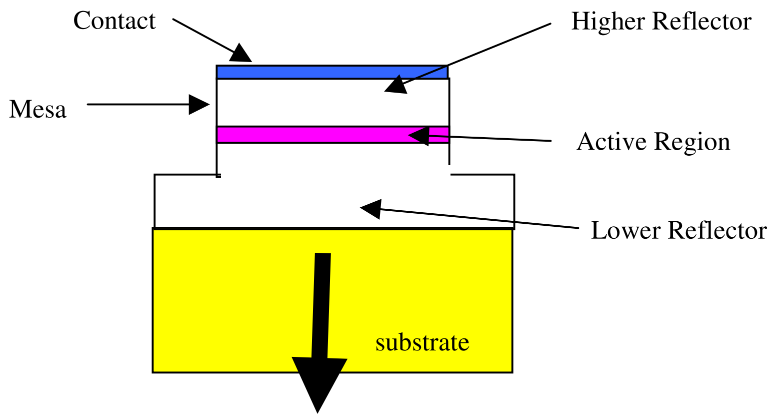


b) Implant Defined Device

- Upper p-type hole injection layer is etched (active Layer)
- Upper mirror is SiO2 / TiO2
- Lower Reflector is quarter wave reflector Stack
- This Epitaxial Bragg relector type is not attractive since refractive index step is small and etched well

- Protons or Oxygen ions used to selectively produce buried current blocking layer to funnel current through small area of active layer
- Neighbouring devices may be isolated by mesa etching or by further implantation

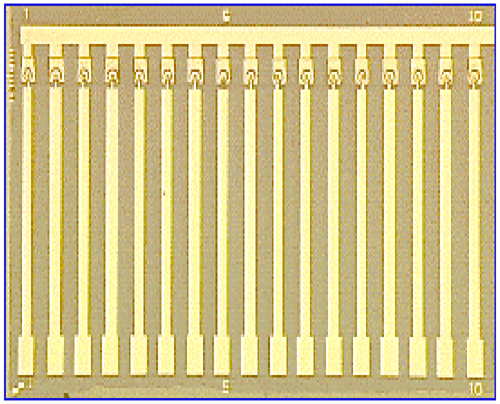
Device Geometries for VCSEL Devices - Continued

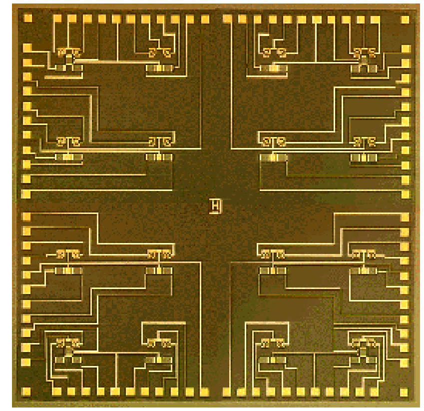


c) Bottom Emitting Mesa

- Substrate is transparent
- Passivated with polyimide, oxides, nitrides, or by Semiconductor Overgrowth

VCSEL Monolithic Array

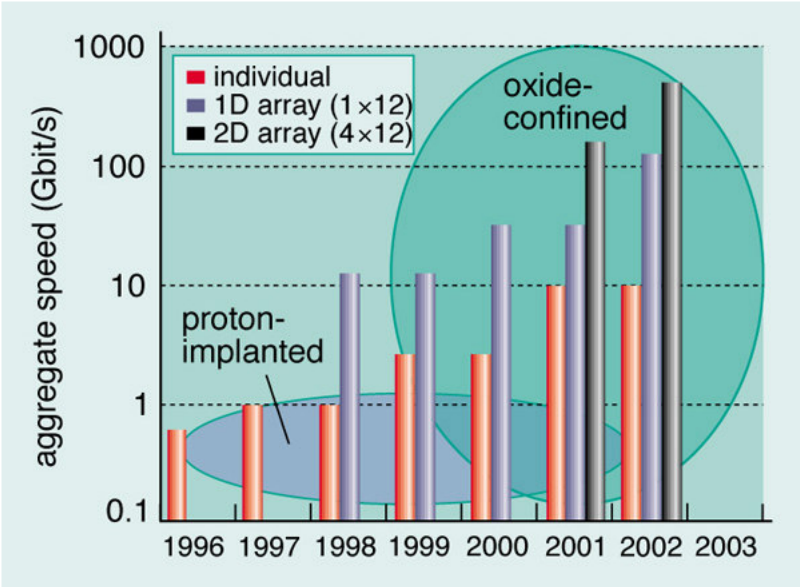




- Two or more emitting areas (or elements) on a single chip makes a "monolithic array"
- The elements may be arranged in a single line (1D), a square array (2D), or in any arbitrary pattern
- If each element can be turned on or off independently, the array can be strobed in sensor applications or can carry multiple high-speed data streams in data communications applications.
- If all elements are always turned on simultaneously, then a precise fixed pattern of emitting spots is generated with a single electrical connection.

VCSEL Arrays

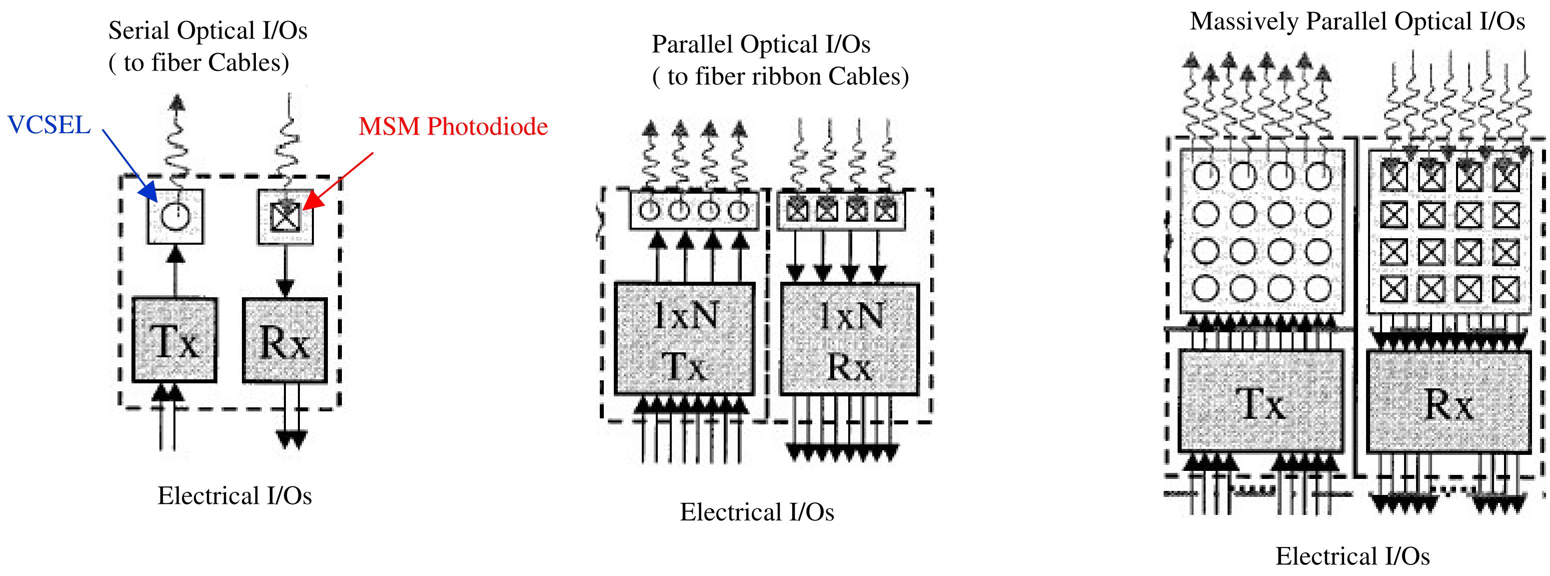
- VCSEL Array Manufacturers – FUJI Xerox Inc, Agilent, Emcore, Cielo, Avalon Photonics, Zarlink and ULM Photonics
- FUJI Xerox – 8 X 8 multimode VCSEL arrays – AM 0808
    - Maximum Modulation speed 2.5 Gbps
    - 850 nm
    - Threshold Current – 1 (0.5-2) mA
    - Max Optical output power – 4 mW
    - Max driving current – 15 mA
- . Avalon Photonics – VCSEL Arrays
    - 3 dB Modulation – 3 GHz
    - Aggregate speed – 3 X N for N VCSELS in a array
- Looking at the maximum 3 dB bandwidth for a single channel, the highest value reported is 21.5 GHz (Lear *et al.),* but typically bandwidths are around 10 GHz[1].



Aggregate Speed for VCSEL Arrays[1]

1.http://www.compoundsemiconductor.net/magazine/article/8/3/4/1

VCSEL Array Configurations

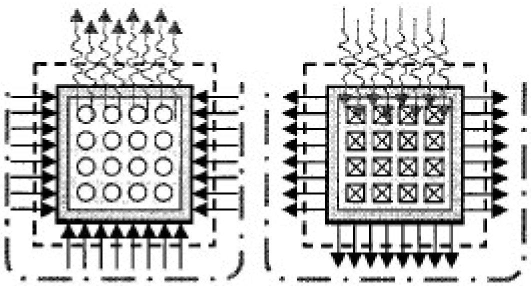


a) Serial Link Module b) 1D Array c) 2D Array

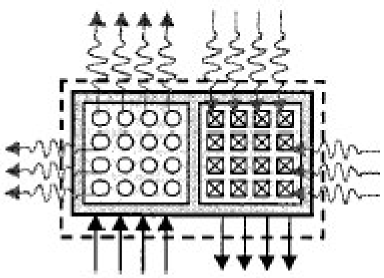
Liu, Honeywell, Heterogeneous Integration of OE Arrays

2D Array Configurations

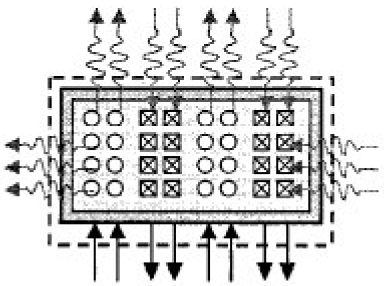
Flip Chip Bonding



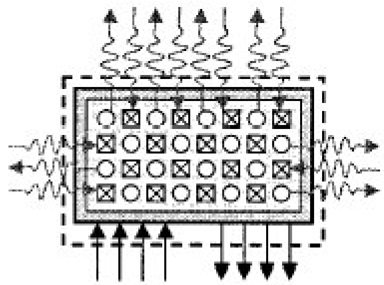
- OE integrated directly on the top of the ASIC
- Mixed signal ASIC
- Free Space Optical Interconnect



a) Separate VCSEL and PD Array

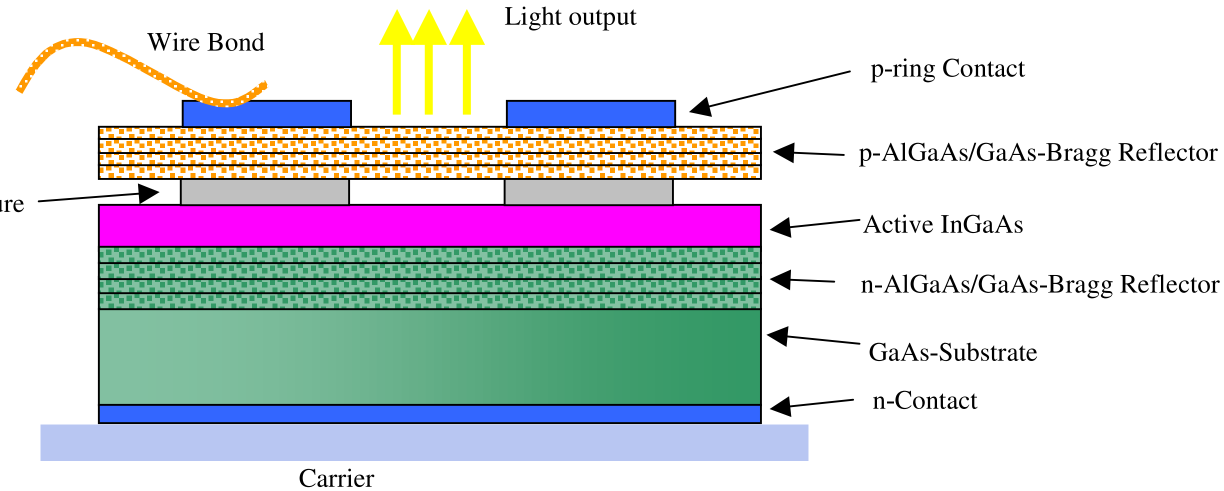


b) Clustered Pixel Layout



c) Interlaced Pixel Layout

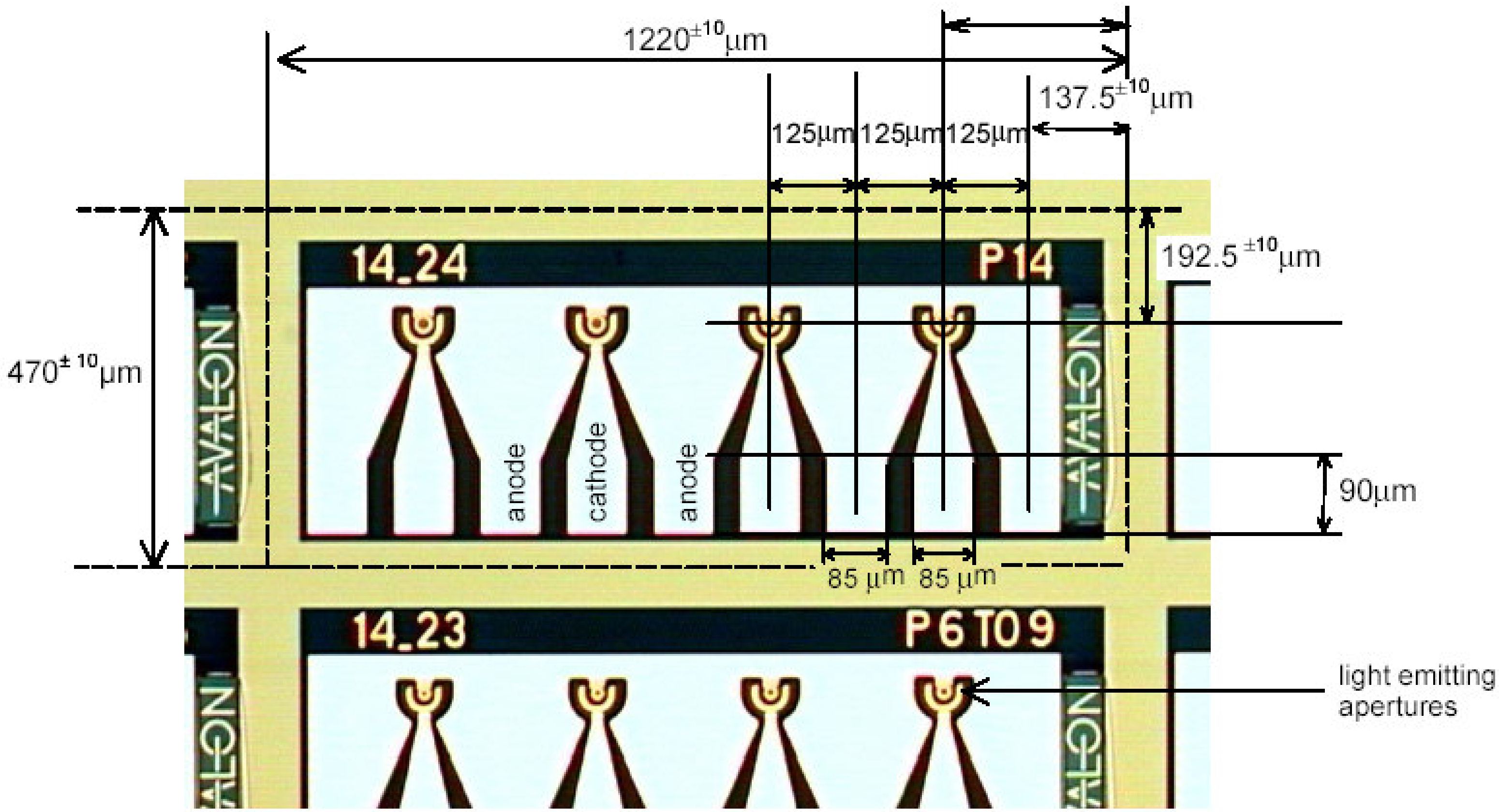
ULM Photonics Array Configuration



Structure

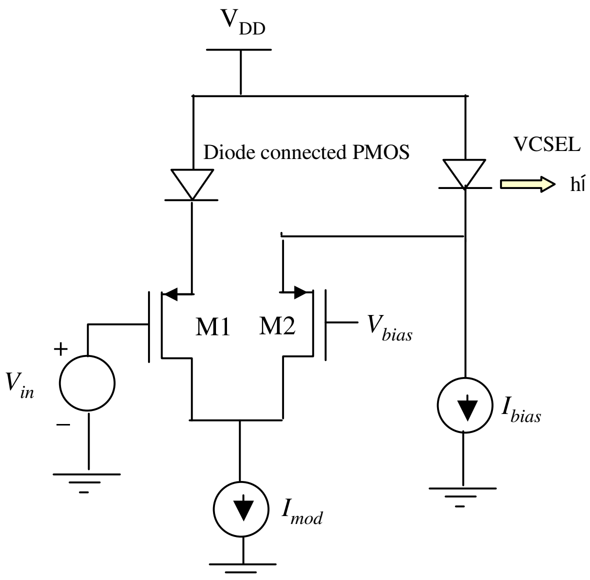
- VCSEL Bond wired and glued to submount
- 850 nm optical output
- Top Emitter

10 Gbit/s VCSEL Array

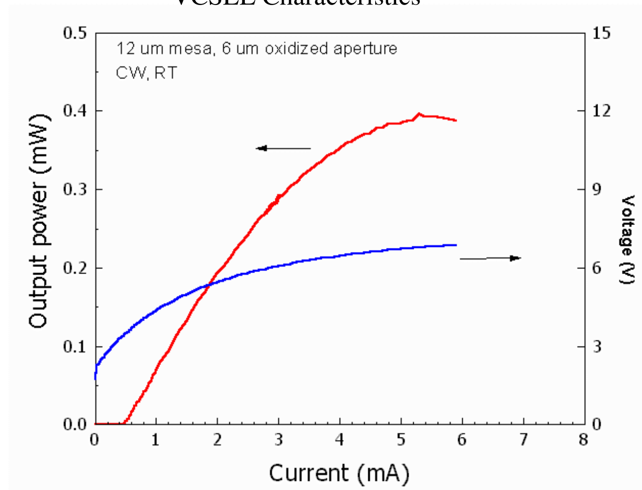


Driver Circuit for VCSEL Array[1]

Each Pixel



VCSEL Characteristics[2]



Operation

M2 provides the bias current into the VCSEL where I_{bias} is just above thershold current

M1 provides the modulated drive current into the VCSEL. (modulated by V_{in})

I_{mod} is steered either through dummy diode load D1 (diode connected PMOS) or VCSEL

It is achieved by complementary V_{in} and V_{bias}

When Vin is low and Vbias is high, VCSEL is driven by $I_{bias} + I_{mod}$, producing logical high optical output

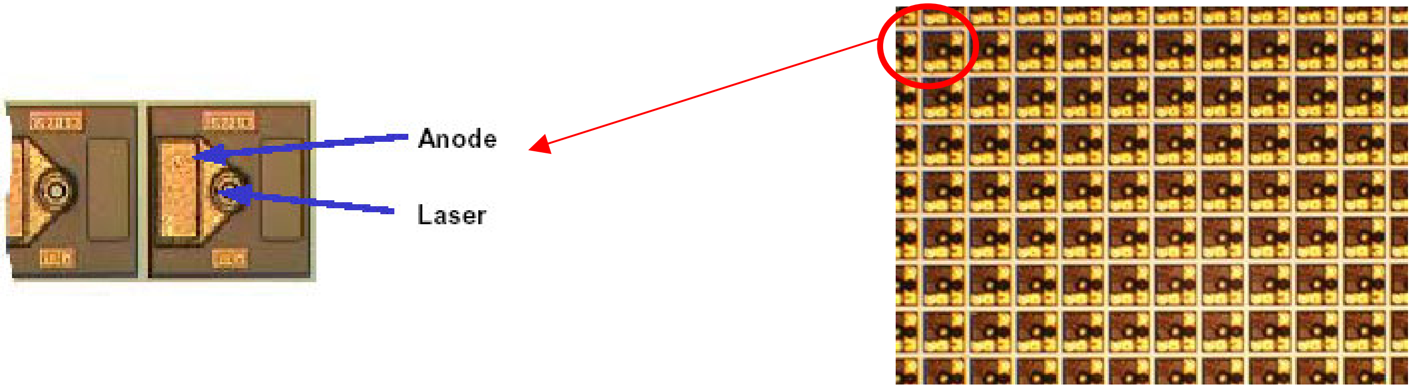
When inputs are reversed, VCSEL is biased only to I_{bias} and produce logical low output

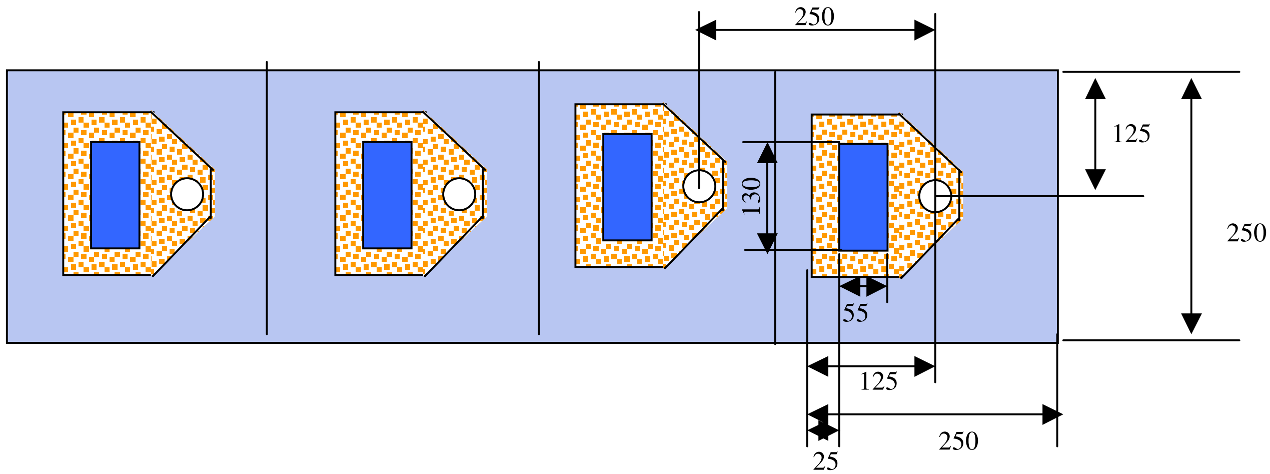
Specification

VCSEL bias current - Tunable from 0 mA to 2.5 mA
Maximum drive current - 3.5 mA + bias current
Maximum operating voltage - 3.5 Volts at the VCSEL anode
Fabrication Technology Hewlett Packard (HP) 0.8 mm
CMOS26G Process (through MOSIS)

1. D.V. Plant, "*256-Channel Bidirectional optical interconnect using VCSELs and Photodiodes on CMOS*", IEEE J. Lightwave Technologies, Vol.19, No. 8, August 2001
2. http://www.ee.umd.edu/photonics/papers/oida/driver.htm

ULM Photonics Array Configuration





Size : 1000 X 250 X 150 μm
1 X 4 Array

Tunable VCSEL Structure

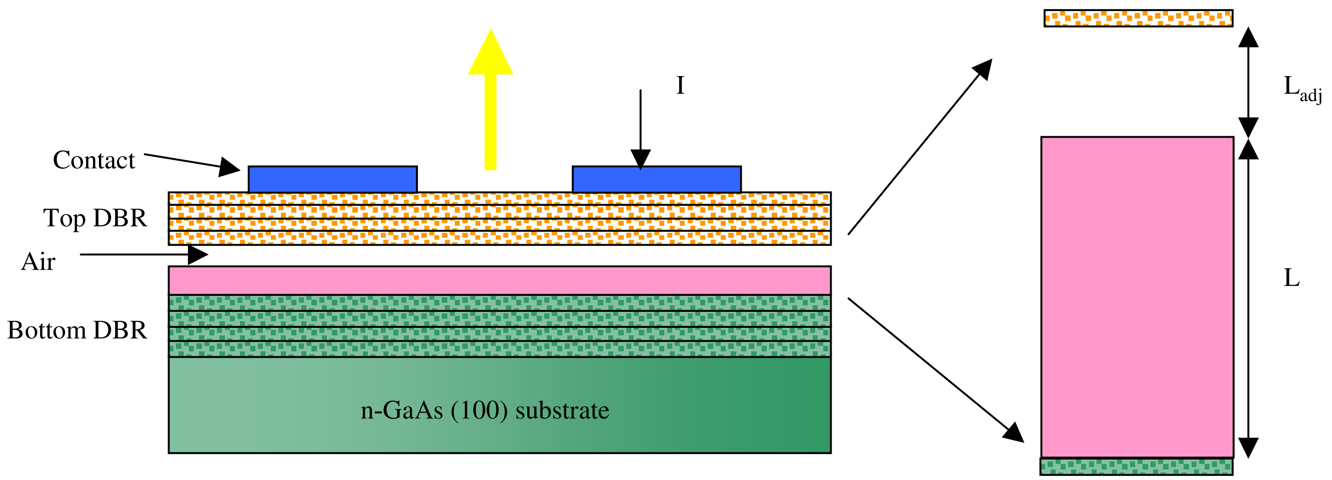
- The ability to tune laser frequency relaxes the fabrication tolerances which makes suitable for long distance optical communication
- Cavity Resonace can be written as,

$$\text{nL} = m\frac{\lambda}{2}$$

- Where n is refractive index, L is the length of the cavity, ë is the wavelength and m is the constant
- Wavelength can be tuned by either changing L or n
- n can be changed by heating or cooling
- But not suitable due to low tuning speed, small change and excessive loss at high temperatures
- Hence change in L

http://snowmass.stanford.edu/~fred/Papers/JMEMS.pdf

Wavelength Tuning in VCSEL



$$nL + L_{adj} = m\frac{\lambda}{2}$$

Ashok Rangawamy
(Directed by: Dr. V. K. Jain)

http://snowmass.stanford.edu/~fred/Papers/JMEMS.pdf

Honeywell VCSEL Array

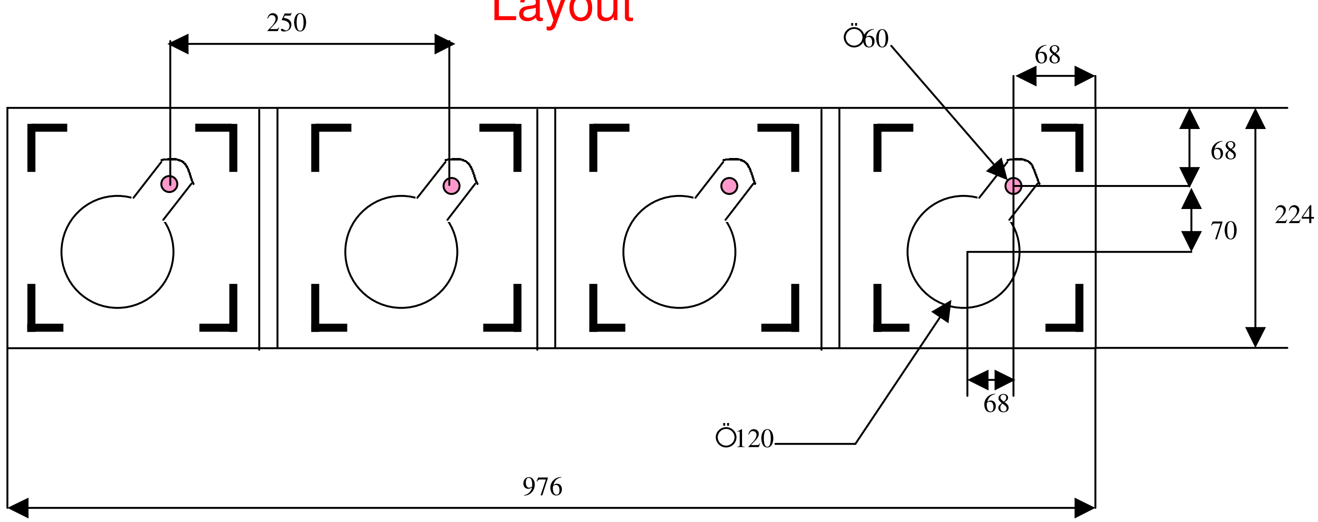
- The HFE80xx-101 is a high-performance 850 nm VCSEL (Vertical Cavity Surface-Emitting Laser) array die optimized for high-speed data communications. The HFE80xx-101 is a fully *stabilized* and tested VCSEL array die, ideal for use in manufacturing transceivers for parallel optical interconnects. The die is available in either 4 or 12 channel configurations.
- The HFE80xx-101 is designed to be used with inexpensive silicon or gallium arsenide detectors, but excellent performance can also be achieved with some indium gallium arsenide detectors. The Honeywell companion array detector is the HFD80xx-101.

Parameter	Test Condition	Symbol	Typ Value	Units
Optical Power Output	I_F=6mA	Po	2	mW
Threshold Current		I_{Th}	2	mA
Threshold current temperature variation	0-70 deg C	ÄI_{Th}	1	mA
Peak Wavelength	I_F=6mA	ë	850	nm
Series Resistance	I_F=6mA	Rs	35-60	Ohms
Beam Divergence		è	17-30	deg

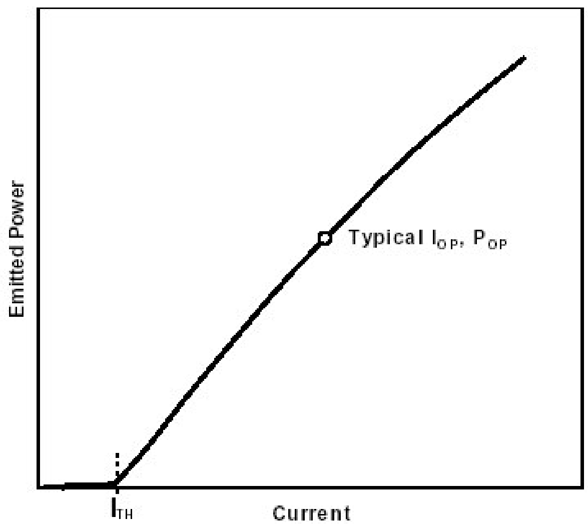
http://content.honeywell.com/vcsel/pdf/HFE80xx-101.pdf

Honeywell VCSEL 1X4 Array

Layout



Lasing Characteristics



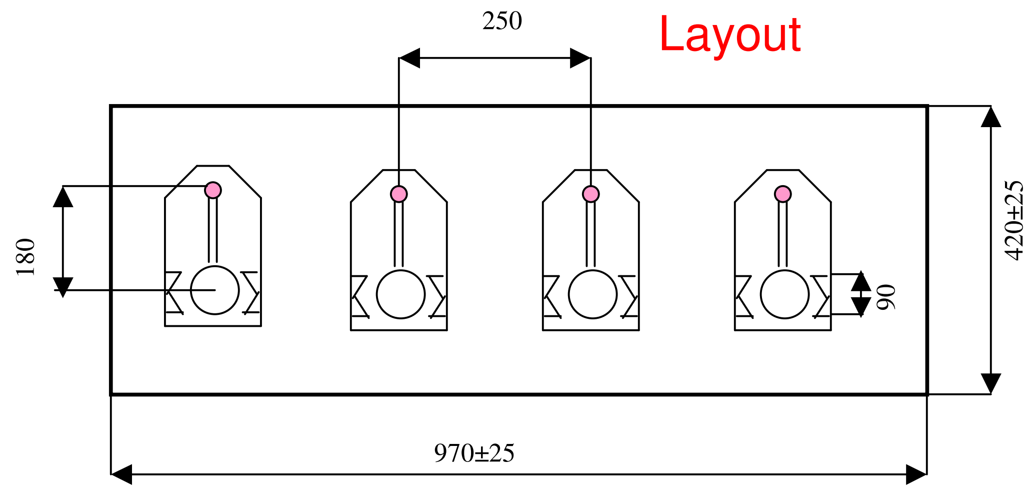
http://content.honeywell.com/vcsel/pdf/HFE80xx-101.pdf

OptoWell 1X4 VCSEL Array

Parameter	Test Condition	Symbol	Value	Units
Optical Power Output	I_F=5 mA	Po	2	mW
Threshold Current		I_{Th}	1.5	mA
Threshold current temperature variation	0-70 deg C	ÄI_{Th}	1	mA
Peak Wavelength	I_F=5 mA	ë	850	nm
Series Resistance	I_F=5 mA	Rs	25-55	Ohms
Beam Divergence	Po=2 mW, Full width	è	14-30	deg

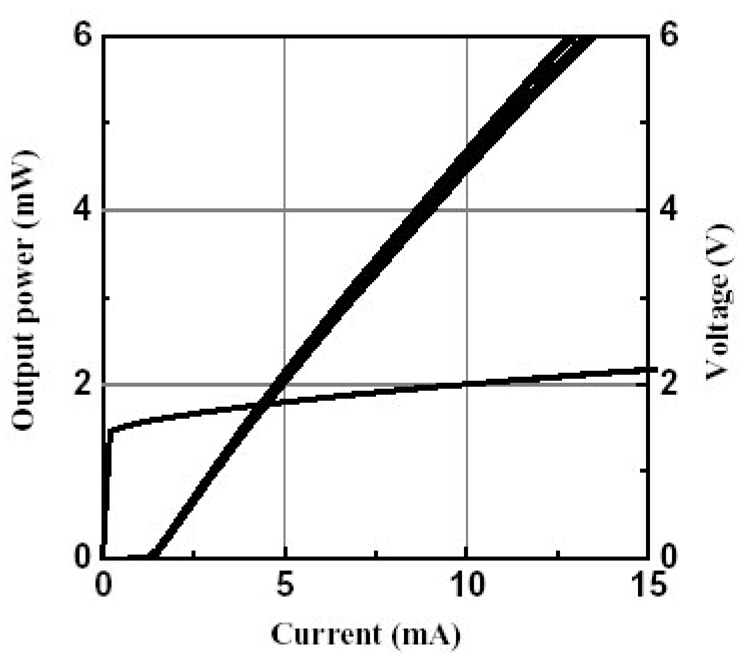
http://www.optowell.com/homepage2/VCSEL/AM85-1N104.pdf

Layout



Lasing Characteristics

OptoWell 1X4 VCSEL Array



Ashok Rangawamy
(Directed by: Dr. V. K. Jain)

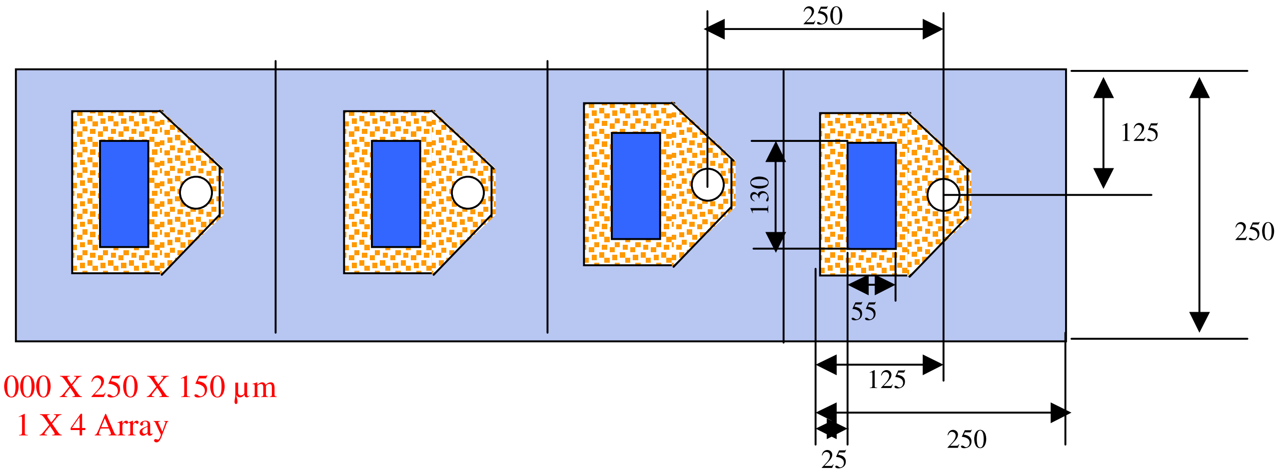
ULM Photonics

Parameter	Test Condition	Symbol	Value	Units
Optical Power Output	I_F=5 mA	Po	2	mW
Threshold Current		I_{Th}	1.5	mA
Threshold current temperature variation	0-70 deg C	ÄI_{Th}	1	mA
Peak Wavelength	I_F=5 mA	ë	850	nm
Series Resistance	Po = 2 mW	Rs	30-100	Ohms
Beam Divergence	Po=2 mW, Full width	è	6-20	deg

http://www.ulm-photonics.de/docs/pdfs/ULM850-05TN-Unxmm.pdf

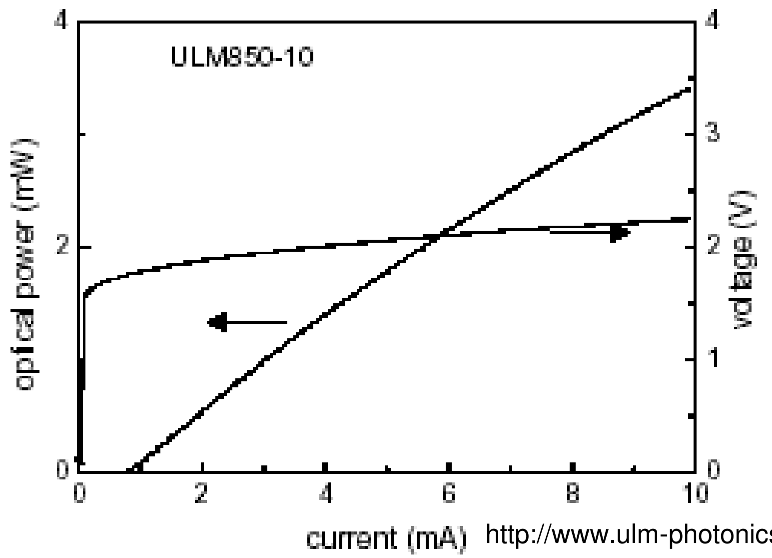
ULM Photonics

Layout



Size : 1000 X 250 X 150 µm
1 X 4 Array

Lasing Characteristics



http://www.ulm-photonics.de/docs/pdfs/ULM850-05TN-Unxmm.pdf

Hikari- 8X8 VCSEL Array

Parameter for Individual Laser	Test Condition	Symbol	Value	Units
Optical Power Output	I_F=10 mA	Po	2 (1-5)	mW
Threshold Current		I_{Th}	0.6 (0.3-1)	mA
Slope Efficiency			0.4	mW/mA
Peak Wavelength		ë	960 (940-970)	nm
Threshold Voltage			1.5	Volts
Beam Divergence	Full width Half Maximum (FWHM)	è	16	deg

http://www.hikari-trading.com/avap/8x8.html