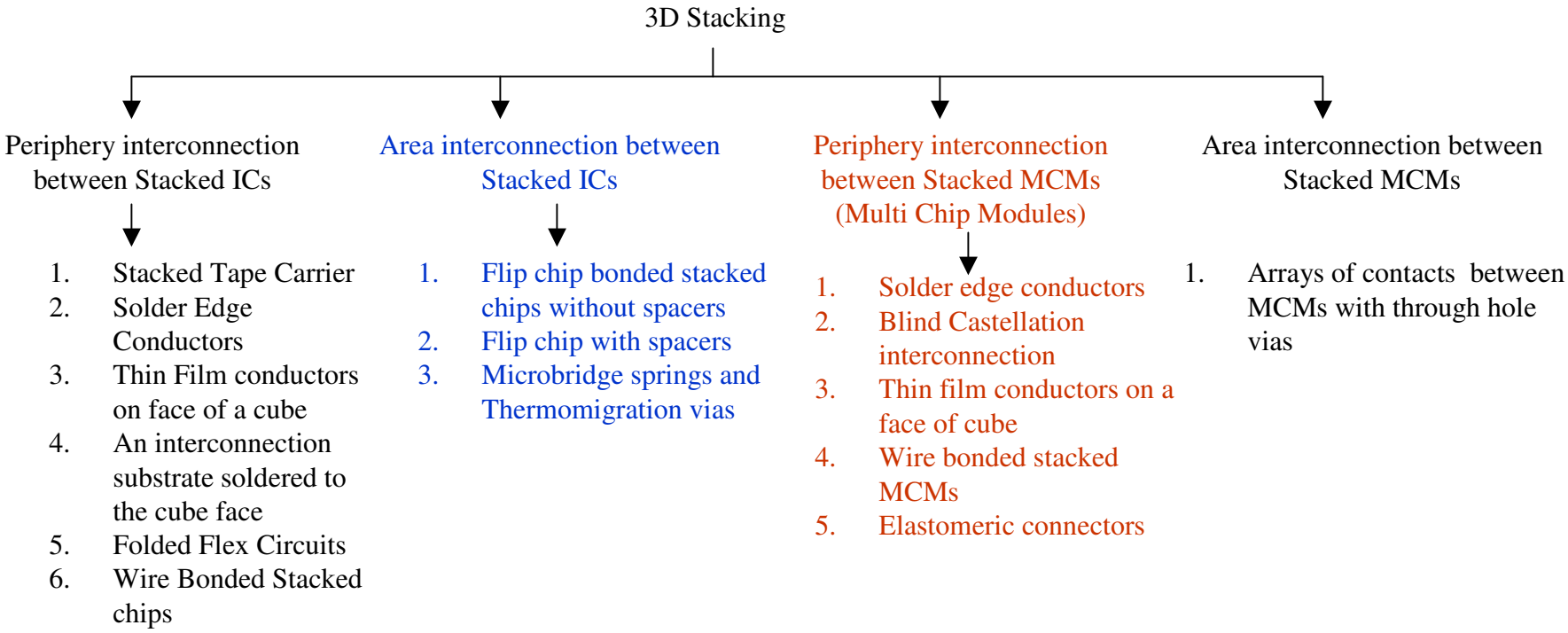
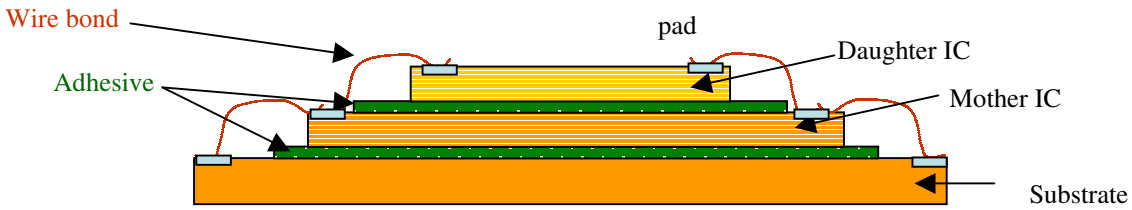
Methods for 3D Stacking



Technologies for Area interconnection between Stacked ICs

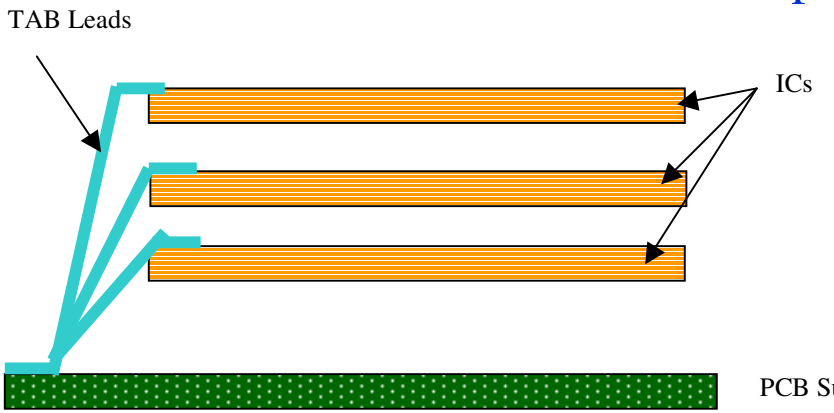
Company	Application	Technique
Fujitsu	ASIC	Flip Chip stacked chips without spacers
University of Colorado & UCSD	Optoelectronic	Flip Chip stacked chips with spacers
Huges	ASIC	Microbridge springs and thermomigration vias

Wire Bonded Stacked Chips



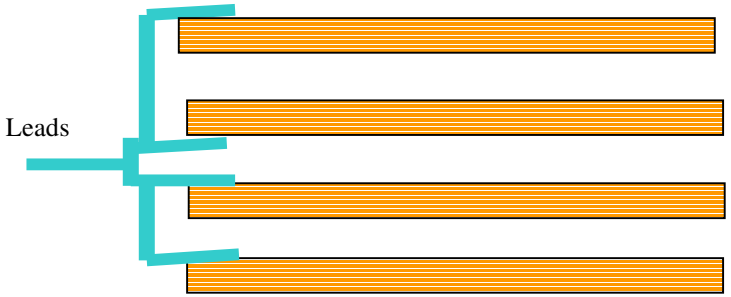
- Mother chip acts as substrate for daughter chip

Stacked Tape Carriers



Stacked TAB on PCB

TAB-Tape Automated Bonding

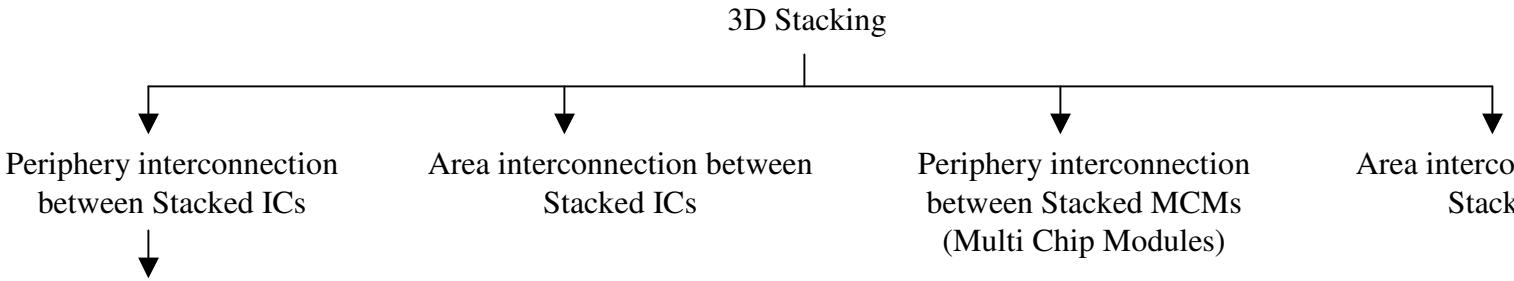


Stacked TAB on Lead Frame

TAB- driver or controller is placed in a thin, hard-bubble package; which the leads extend from the bubble package on a thin substrate. The TAB attaches to the PCB or display glass by the adhesives along the edge

Review of 3D Packaging, Said Al Sarawi, IEEE,Components packging, Vol 21, Feb 1998

Methods for 3D Stacking

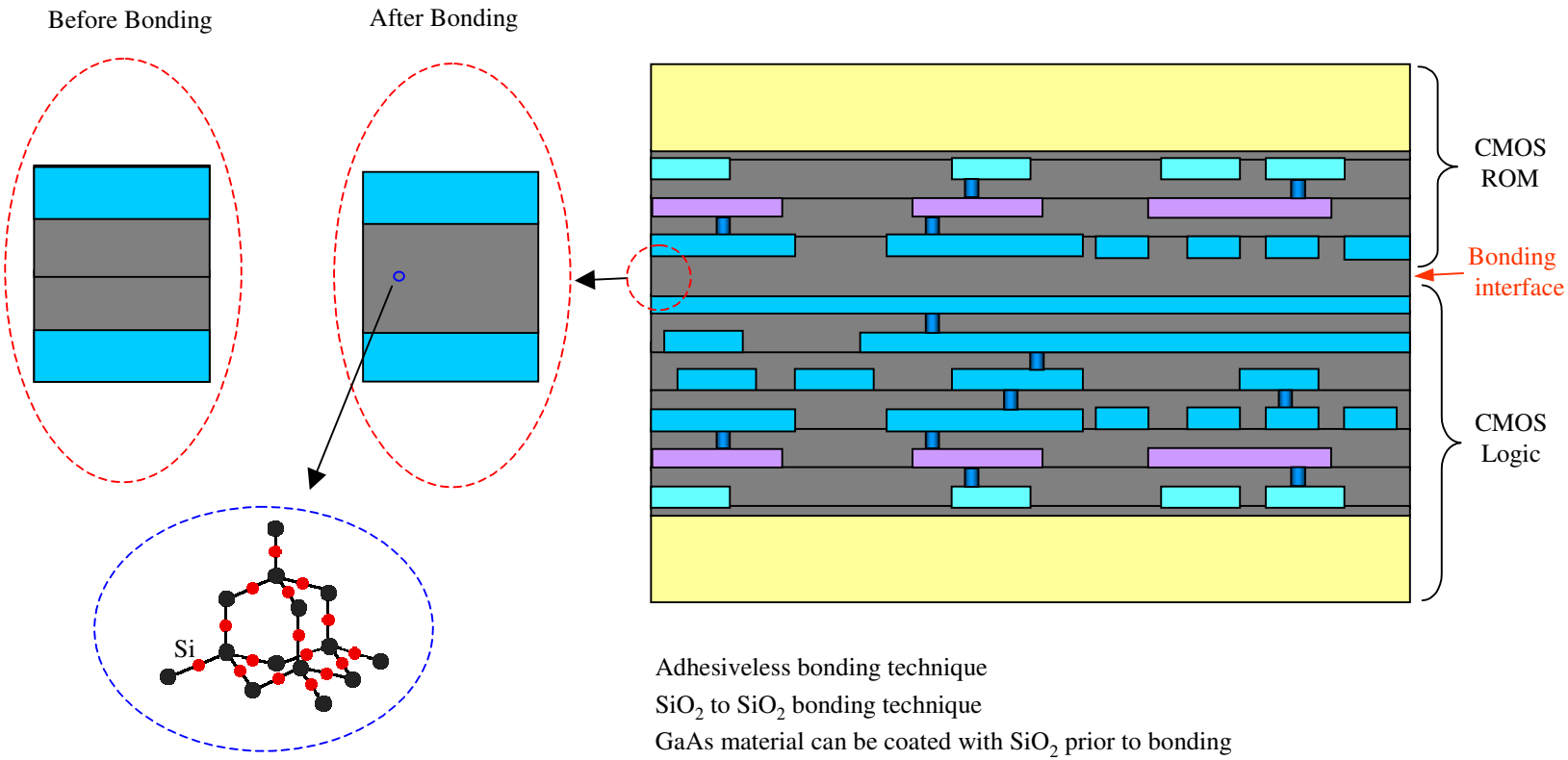


1. Stacked Tape Carrier
2. Solder Edge Conductors
   a. Solder dipped stacks to create vertical conductor on top
   b. Solder filled holes in chip carriers and spacers
   c. Solder connections between plated through- hole
   d. Edge array solder balls
3. Thin Film conductors on face of a cube
   a. Thin film “T-Connects” and sputtered metal conductors
   b. Direct Laser write traces on epoxy cube face
4. An interconnection substrate soldered to the cube face
   a. Array of TAB leads soldered to bumps on Si Substrate
   b. A flip chip bonded to face of the stack
   c. PC Boards soldered on two sides of TSOP Packages
5. Folded Flex Circuits
6. Wire Bonded Stacked chips

1. Arrays of contacts between MCMs with through hole vias
2. Elastomeric connectors with electrical feedthroughs
3. Compliant anisotropic conductive material
4. Microbridge spring

Review of 3D Packaging, Said Al Sarawi, IEEE,Components packging, Vol 21, Feb 1998

Adhesiveless 3D Integration



Covalent Bonding of SiO_2

Adhesiveless bonding technique

SiO_2 to SiO_2 bonding technique

GaAs material can be coated with SiO_2 prior to bonding

Prior to bonding surfaces must be planarized using CMP

Then Ziptronix's proprietary process(Ziroc) is used to activate one or both of the bonding surfaces

Ziroc technology provides covalent bonding between surfaces at room temperature

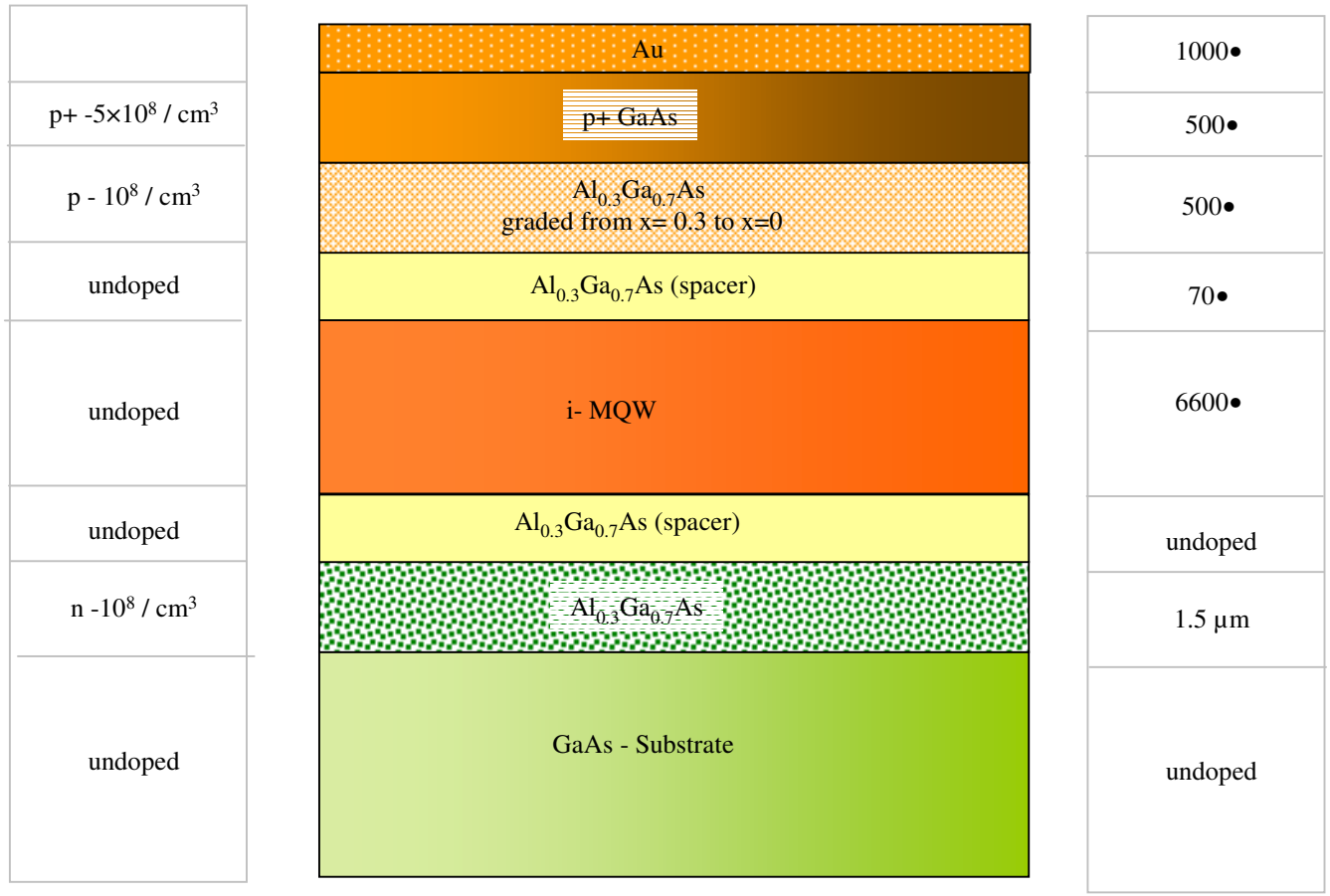
Many varieties of materials can be bonded directly or depositing a thin layer of oxide over them

Bonding process is carried out in normal foundry ambient

http://www.ziptronix.com

Flip Chip Bonding

Step 1: GaAs MQW Modulator Formation

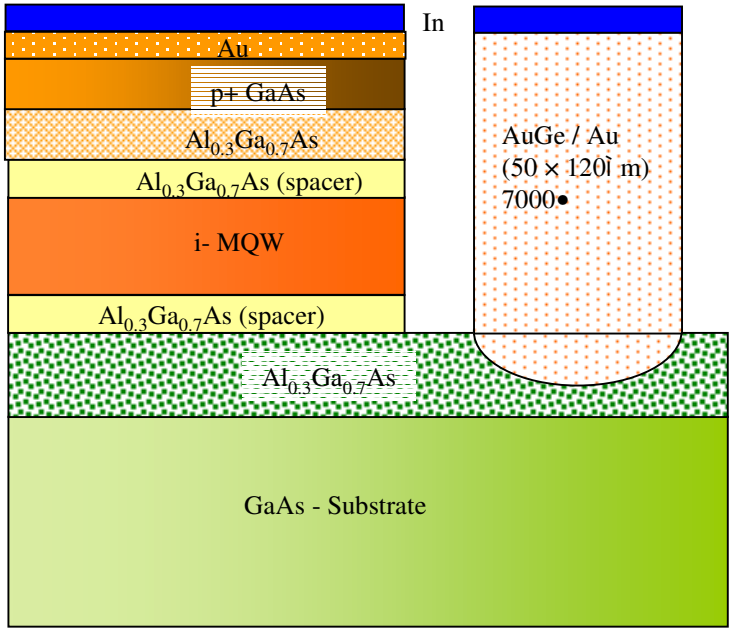


MQW consists of 55 periods of 90• GaAs wells and 90• $Al_{0.3}Ga_{0.7}As$ barriers

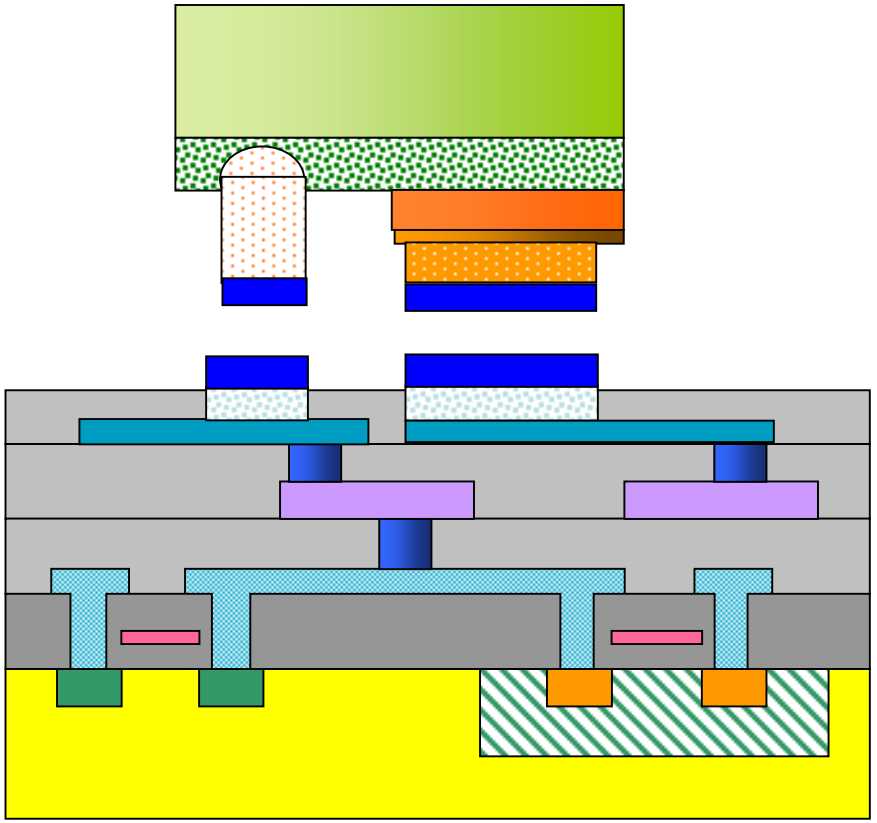
GaAs 850 nm Modulators solder bonded to Silicon, K.W. Goossen et al, IEEE photonics Tech. Letters, Vol 5, No. 7, July 1993

Flip Chip Bonding – Contd…

Step 2: Contact Formation



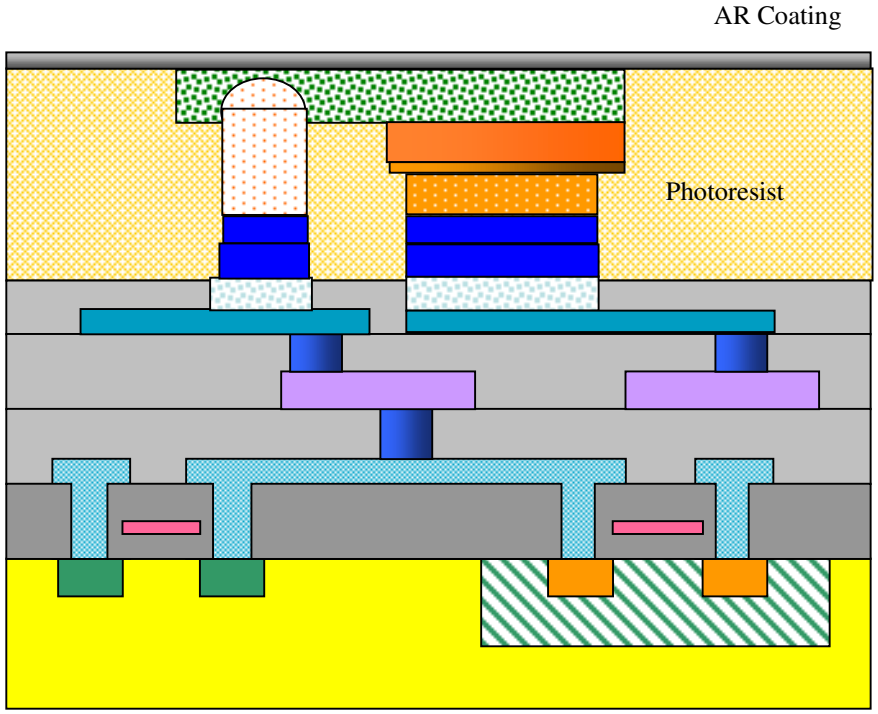
Step 3: Flip Chip integration



1. GaAs 850 nm Modulators solder bonded to Silicon, K.W. Goossen et al, IEEE photonics Tech. Letters, Vol 5, No. 7, July 1993
2. GaAs MQW Modulators Integrated wth Si CMOS, K.W. Goosen, IEEE Photonics Letters Vol.7 No. 4 April 1995

Flip Chip Bonding – Contd…

Step 4: GaAs substrate Removal and Anti reflection Coating Formation

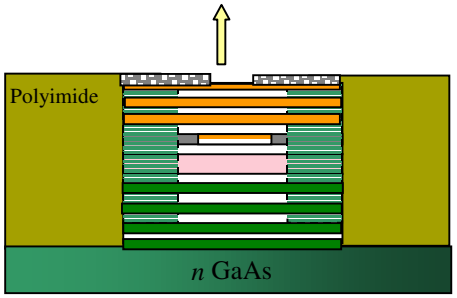


In contacts are bonded when the aligned chips are heated to 200°C for 15 min..
AZ4210 photoresist was flowed between chips and air dried for 12 hrs.
It protects sample during etching for GaAs subtstrate removal and gives additional mechanical support.
GaAs substrate was then etched away using H_20_2:NH_4OH, which stops on $Al_{0.3}Ga_{0.7}As$
Before etching KoH etching was donebriefly to remove GaAs oxide layer.

GaAs 850 nm Modulators solder bonded to Silicon, K.W. Goossen et al, IEEE photonics Tech. Letters, Vol 5, No. 7, July 1993

Integration of InGaAs VCSEL (Applique Method)[1]

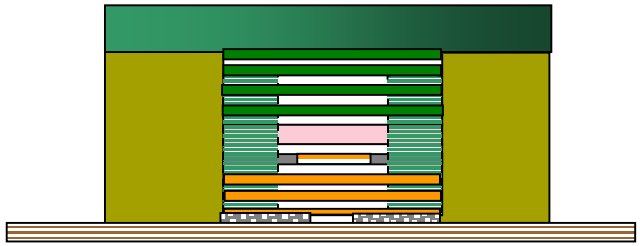
1. VCSEL fabrication



VCSEL[1,2]

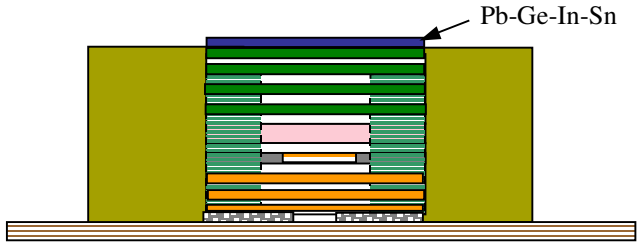
1000 Å AlAs etch layer on (100) n-GaAs substrate
3 pairs of $Al_{0.5}Ga_{0.5}As$/GaAs smoothing layer
22 ½ pairs of the AlAs/GaAs n-bragg reflectors
3 $In_{0.2}Ga_{0.8}As$ QW active region
18 pairs of p-doped top reflectors
180 Å superlattice linear grading at the GaAs/ AlAs interface for the reflectors
Proton implantation for lateral current confinement into 10 ì m diameter.
A solution of H_2SO_4:H_2O_2: H_2O is used to form 20 ì m mesa till etch stop layer is reached
Top ring Contacts (Cr/Au) are formed with apertures of 20 ì m
Polyimide isthen deposited around mesa.

2. Mounted on Glass substrate



VCSEL array is attached to the glass substrate, facing down, using black wax

3. GaAs Substrate removal n- Contact metal Formation

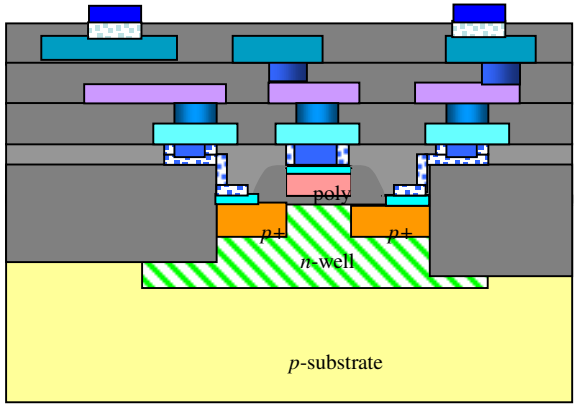


GaAs is first removed by mechanical grinding and polishing within 100ì m of the laser
Then wet etching using NH_3OH:H_2O_2 solution till AlAs etch stop layer is reached
Then AlAs and smoothing layers are etched in dilute HF
Now optically smooth surfaces are obtained
Pd/ Ge/ InSn (1000 Å/ 1000 Å/ 1.5 ì m) back conact is then formed (e beam evaporation) after photoresist patterning
This contact has little stress on epi layer compared to AuGe contact, as a high stress will induce film curvature which can inhibit uniform contacting
InSn is used for bonding with Si

1. D.L Mathine, "The integration of III-V Optoelectronics with silicon circuitry", *IEEE J. Quantum Electronics*, Vol. 3, No. 3, June 1997, pp. 952-959
2. H.Fathollahnejad, "The integration of GaAs VCSEl onto silicon circuitry", IEEE

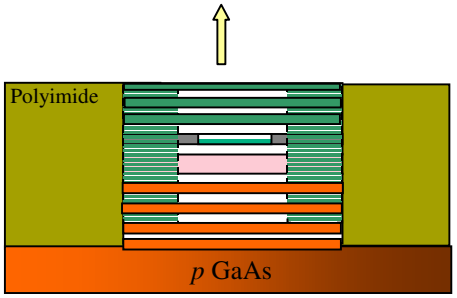
Integration of GaAs VCSEL (Applique Method)[1]

1.CMOS wafer fabrication



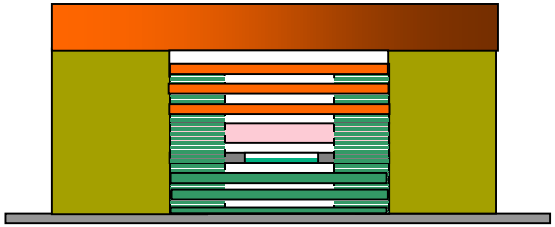
M2

2. VCSEL fabrication

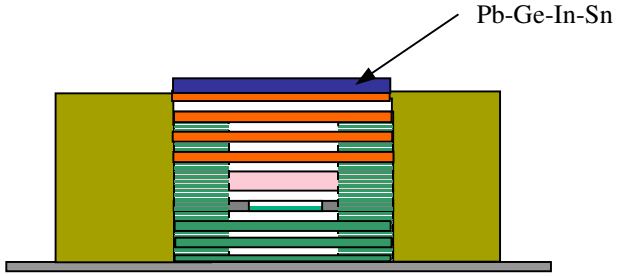


VCSEL[1]

3. Mounted on Glass substrate



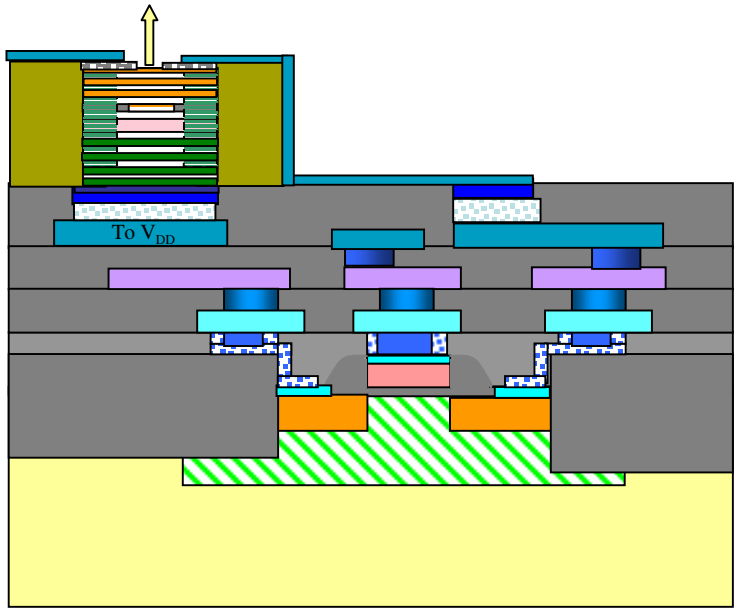
4. GaAs Substrate removal n- Contact metal Formation



1. D.L Mathine, "The integration of III-V Optoelectronics with silicon circuitry", *IEEE J. Quantum Electronics*, Vol. 3, No. 3, June 1997, pp. 952-959

Integration of InGaAs VCSEL (Applique Method)[1] Contd…

5. Integration with CMOS and Contact Formation



The array is removed from glass slide and bonded to pondbad (In) on the CMOS
VCSEL was then coated with polyimide
Polyimide was exposed, developed and patterened to provide insulation
Al was then evaporated to form top contact to V_{DD} continuity.

1. D.L Mathine, "The integration of III-V Optoelectronics with silicon circuitry", *IEEE J. Quantum Electronics*, Vol. 3, No. 3, June 1997, pp. 952-959