

Stability Analysis of CdS/CdTe Solar Cells under illumination

Objective:

- To study and analysis of CdS/CdTe Solar cells for their stability performance under light soaking
- Standardize the stability testing procedure
- To investigate degradation mechanisms involved in the cell performance.

Experimental

Device Measurement

- λ One Half of Sample substrate is mounted inside the oven and stressed under one sun intensity simulated using Halogen lamps and other half remain unstressed.
- λ Day and Night cycle is done by turning on and off the lights at 4 Hour interval.
- λ The samples are maintained at desired temperature zone using water cooling technique.(Now it is maintained below 45 deg C)
- λ Characterization techniques such as IV, CV, Color IV and CF Measurements are used to analyze the degradation mechanisms involved.
- λ Light and Dark IV Measurements are made frequent intervals, keeping samples stressed inside the oven.
- λ The samples are maintained at UHP N₂ ambient.

Set III Samples under light soaking

- Annealing Temperature after CdCl₂ treatment

360,370,380,390 and 400 deg C

- Various CBD CdS Deposition Time

60,70,80 minutes

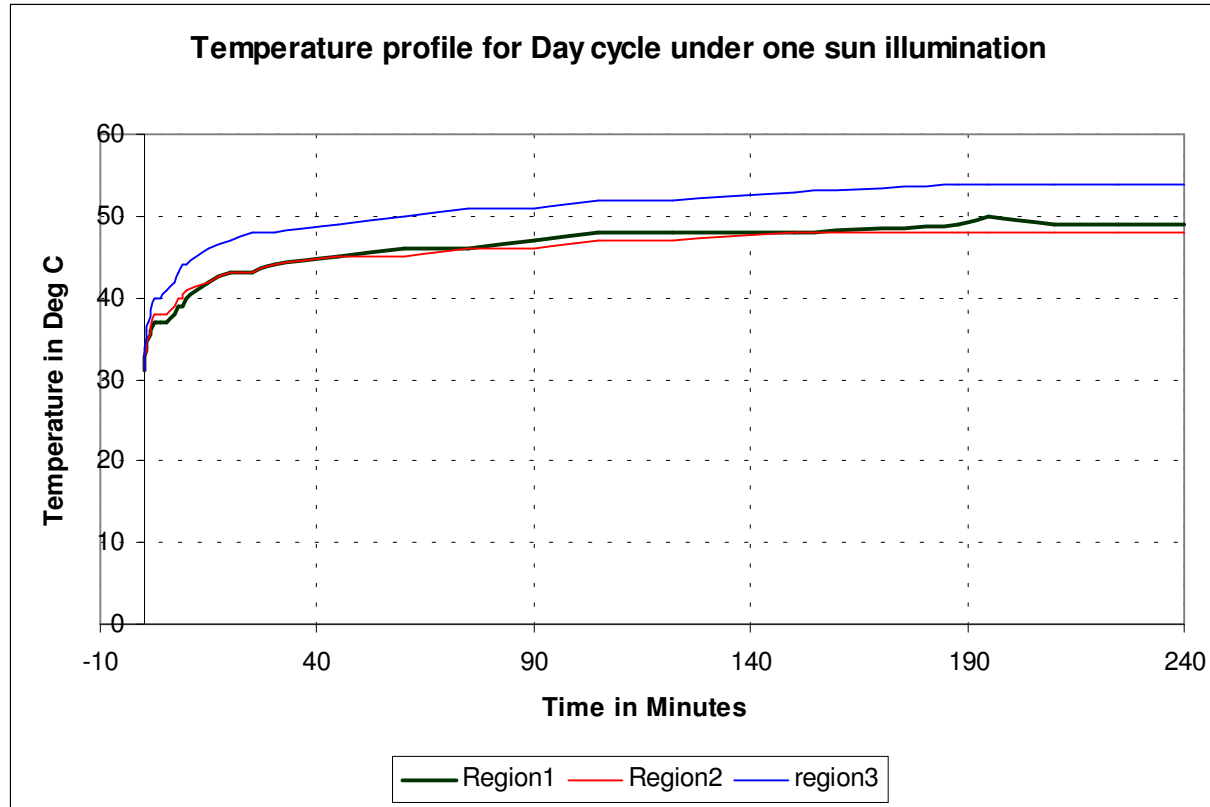
- CdTe only samples without Back contacts to see the effect of back contacts in degradation process

- Samples with CuCl₂ treatment on CdS.

Note:

Samples are tested under Open Circuit and Short Circuit Condition.

Temperature Profile inside the oven



Set point for water flow control 35 deg C

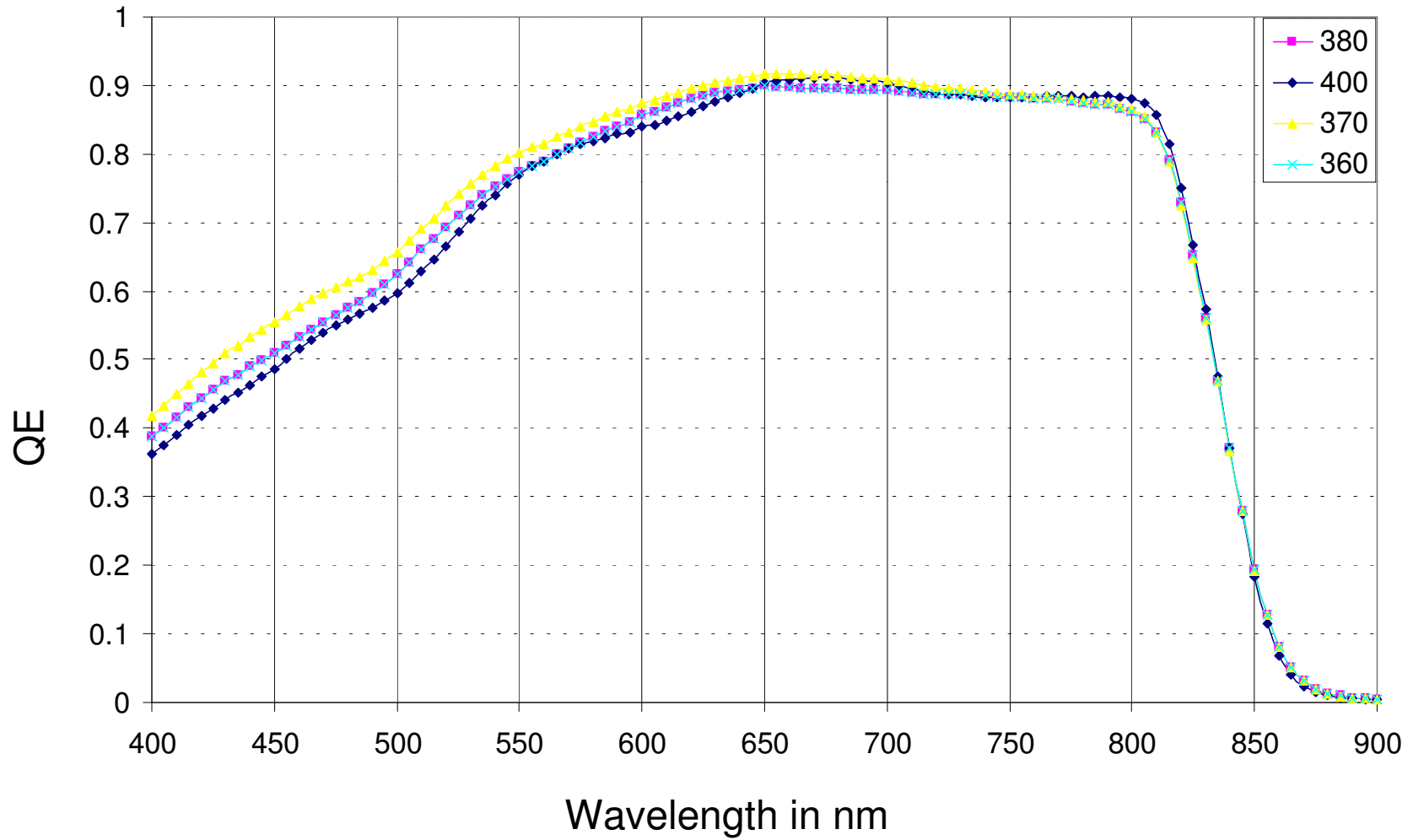
1 2 3

sub Region

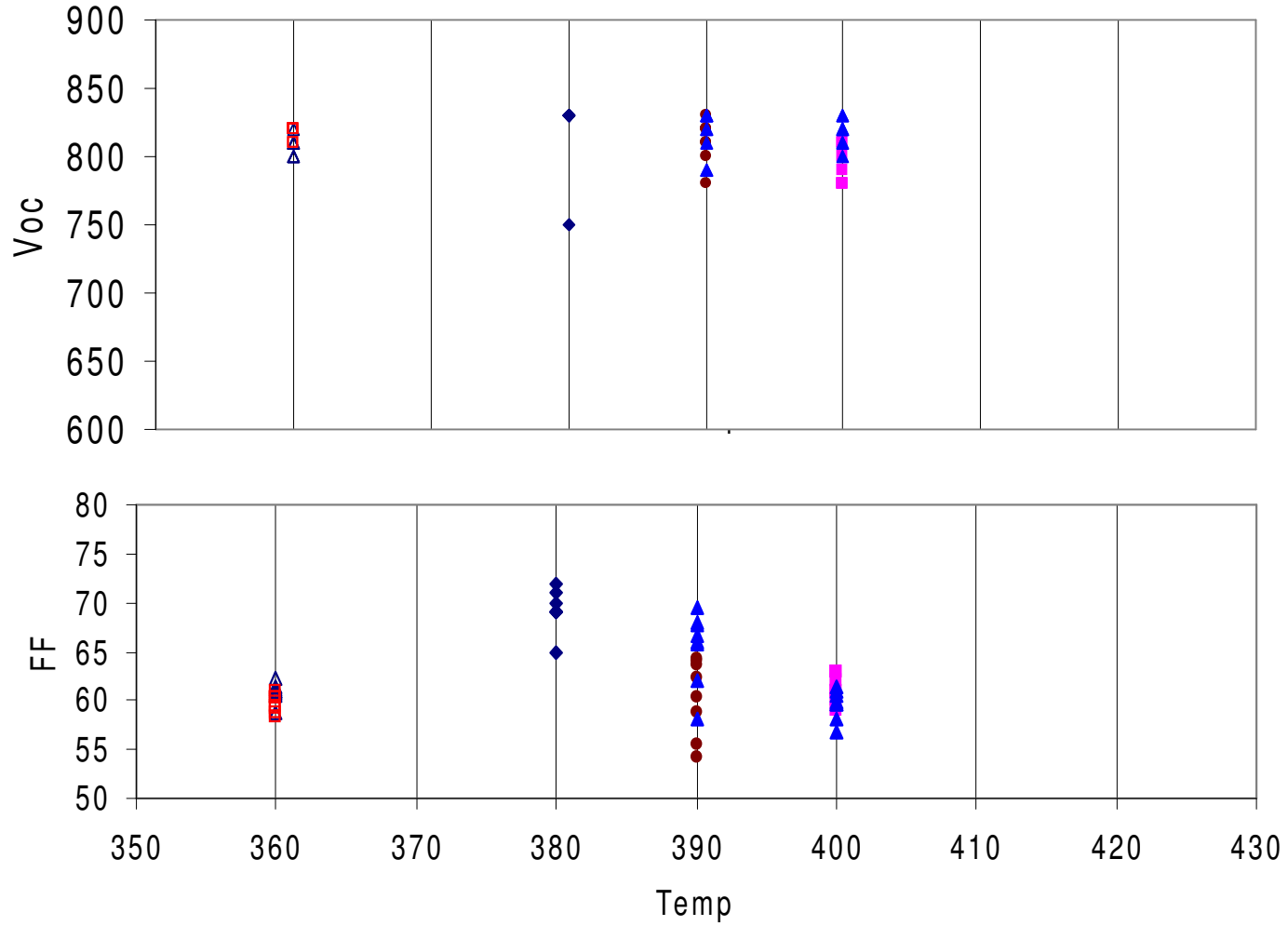
Front
Row

SR Measurement

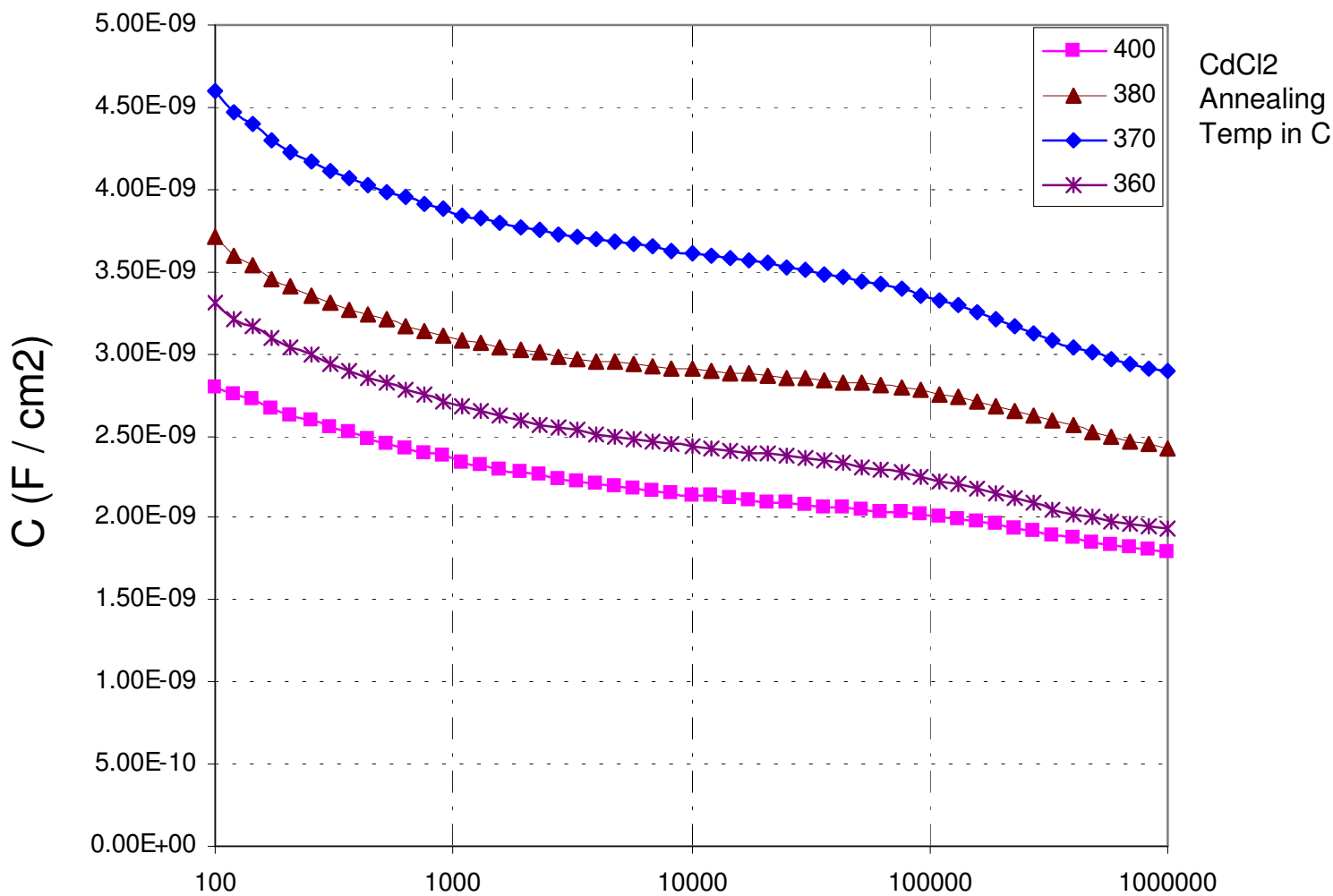
CdCl₂
Annealing
Temp in C



Effect of CdCl₂ Annealing Temperature



CF Measurement at Room Temperature



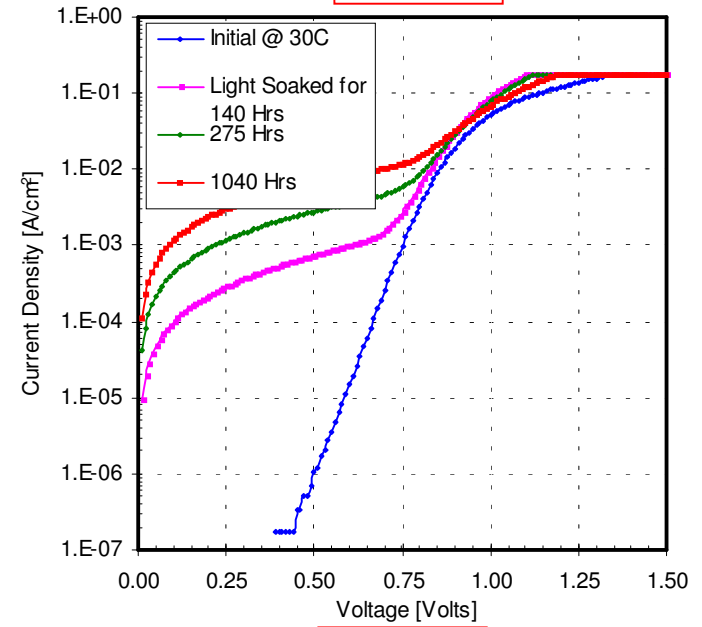
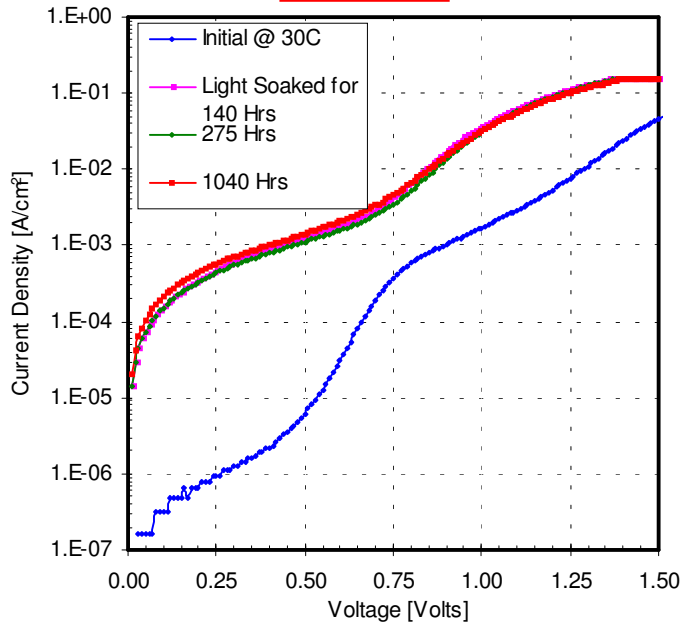
Stability Analysis of CdS/CdTe Solar cells
Ashok Rangaswamy

Frequency in Hz

360⁰ C

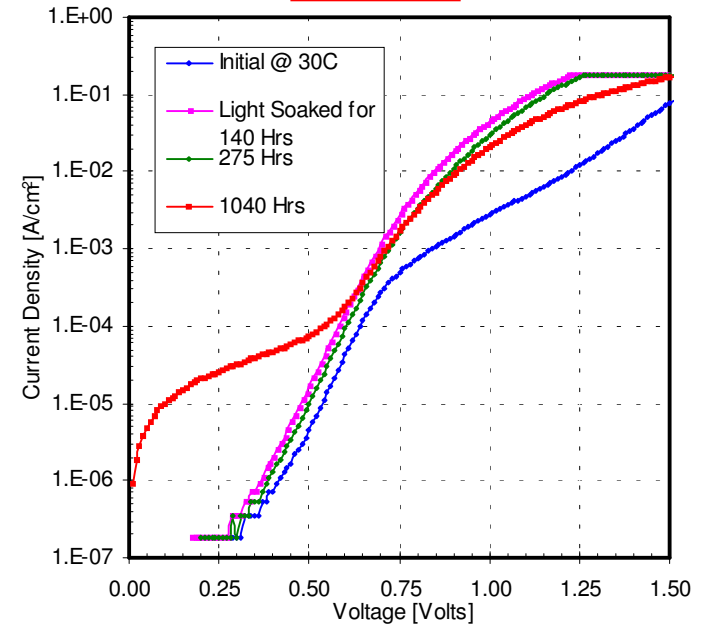
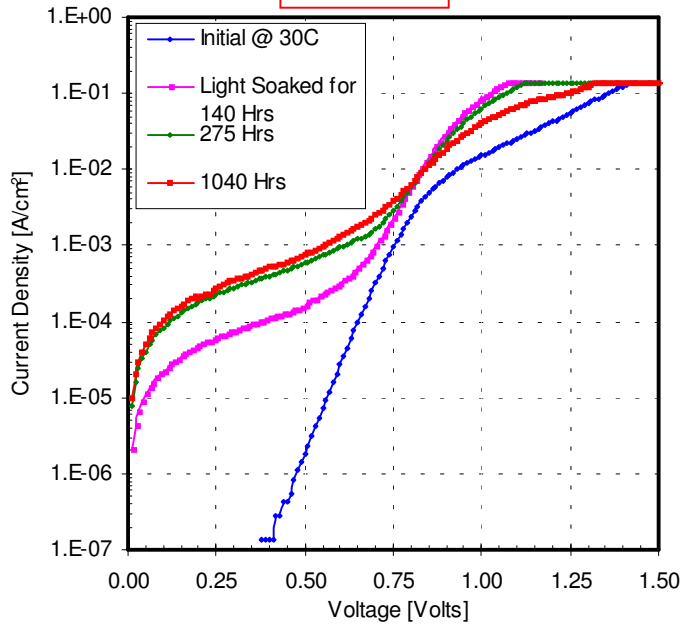
Post Annealing Effect on device stability

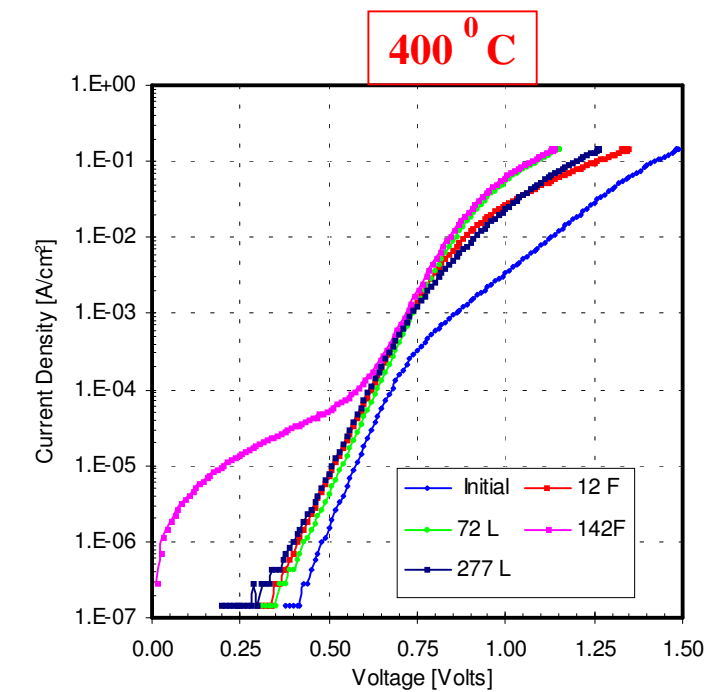
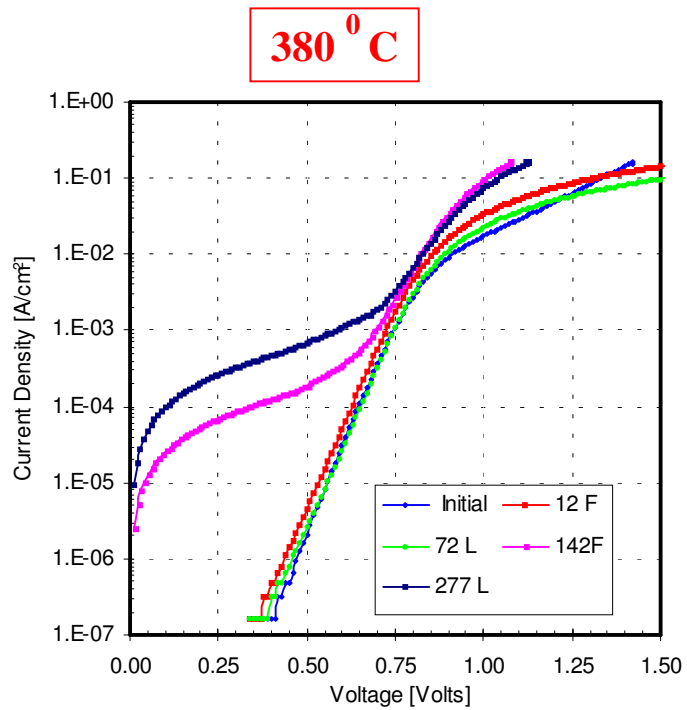
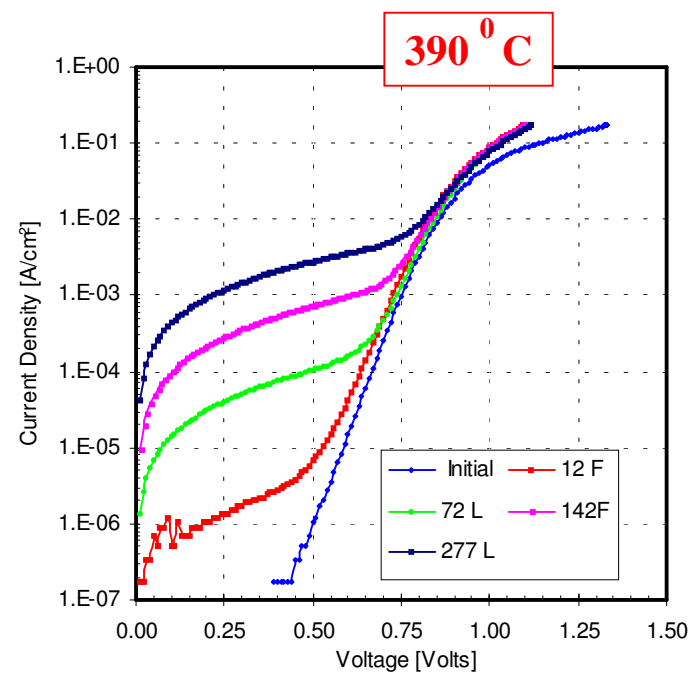
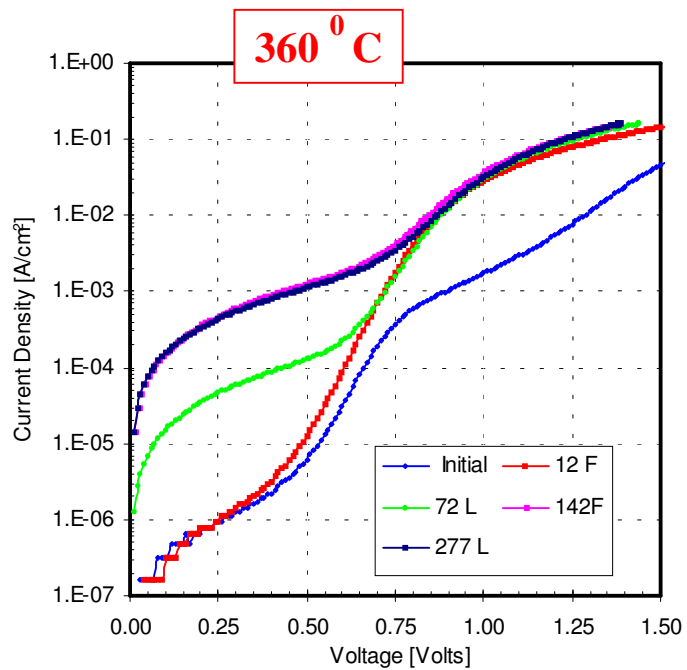
390⁰ C



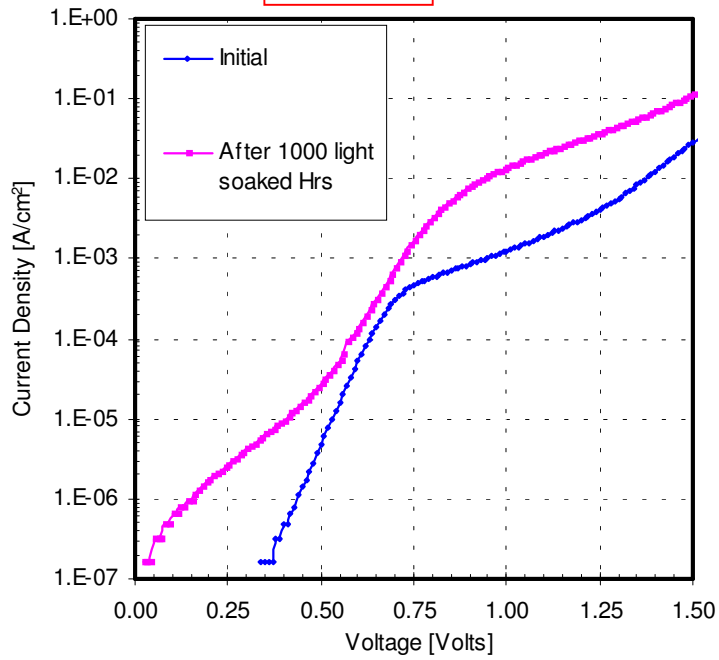
380⁰ C

400⁰ C

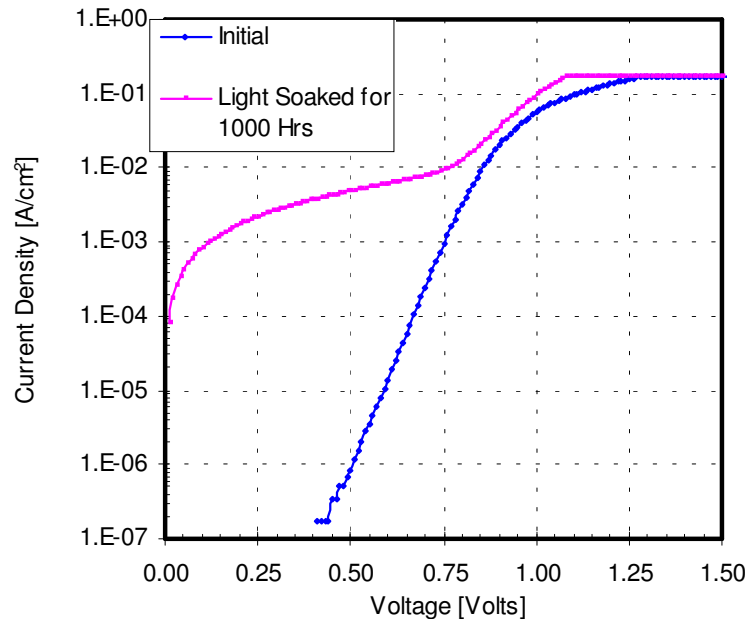




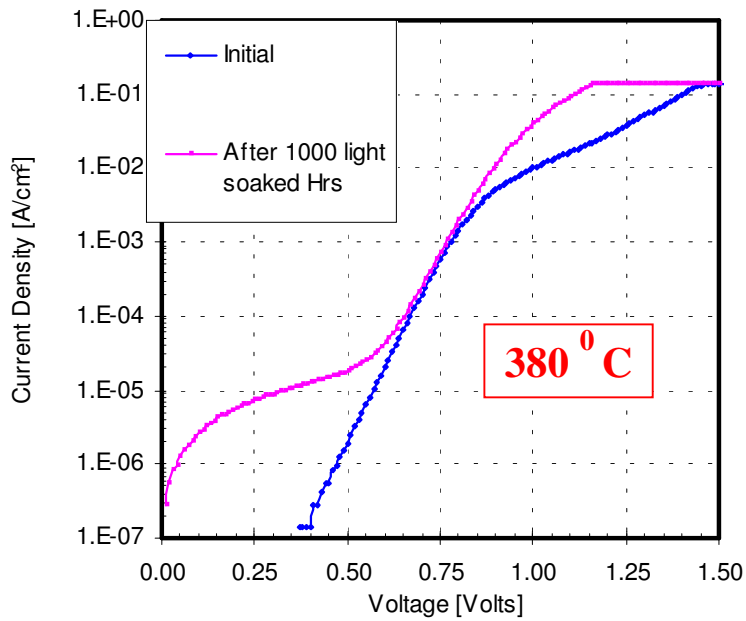
360⁰ C



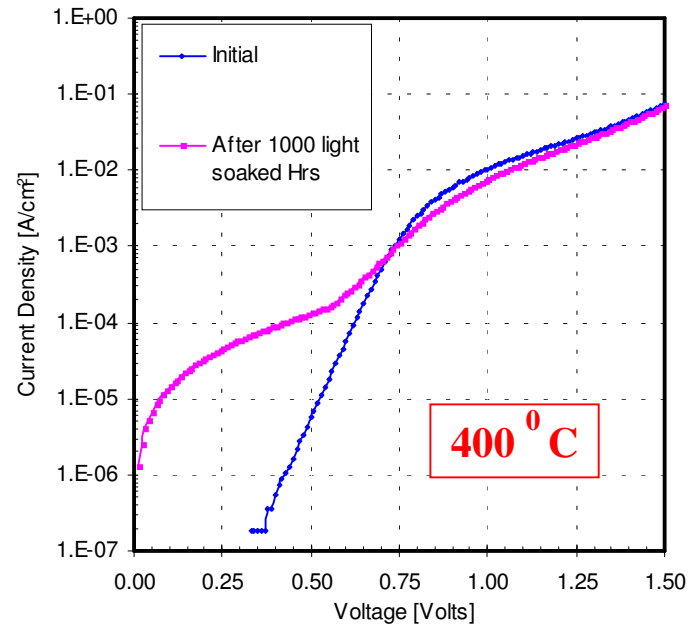
390⁰ C



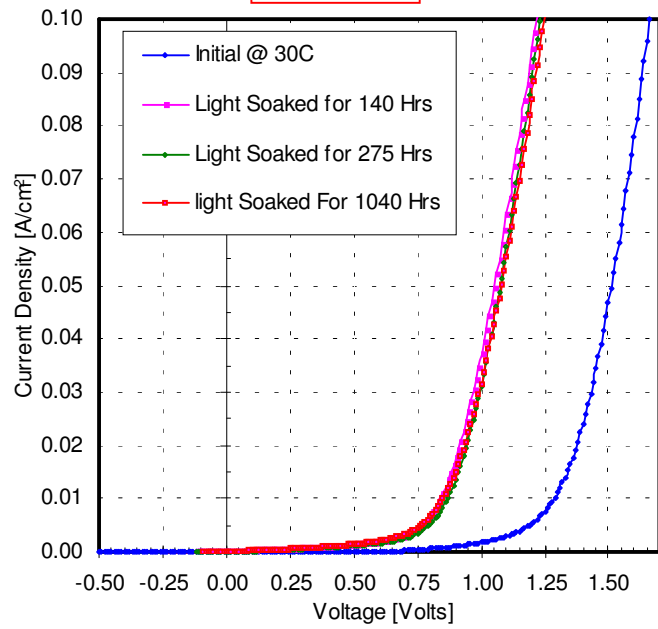
380⁰ C



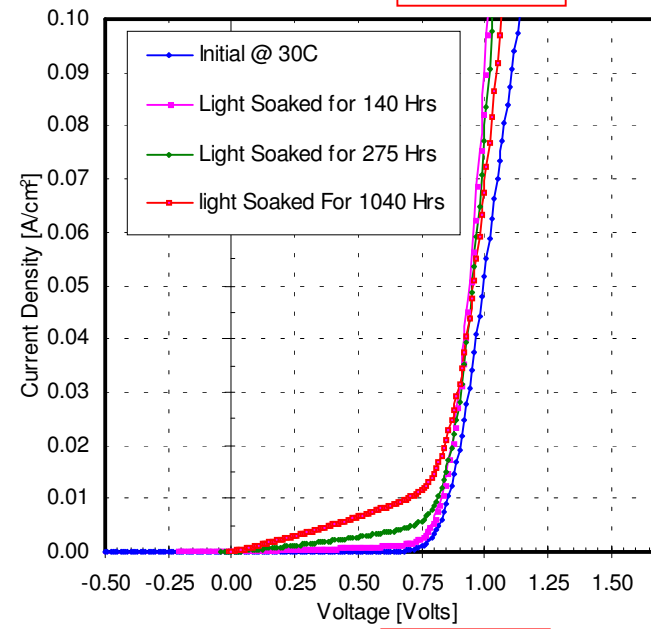
400⁰ C



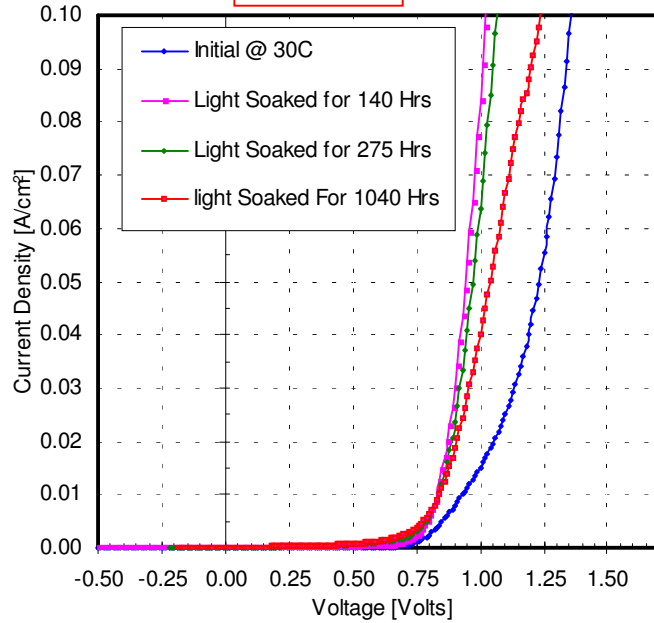
360⁰ C



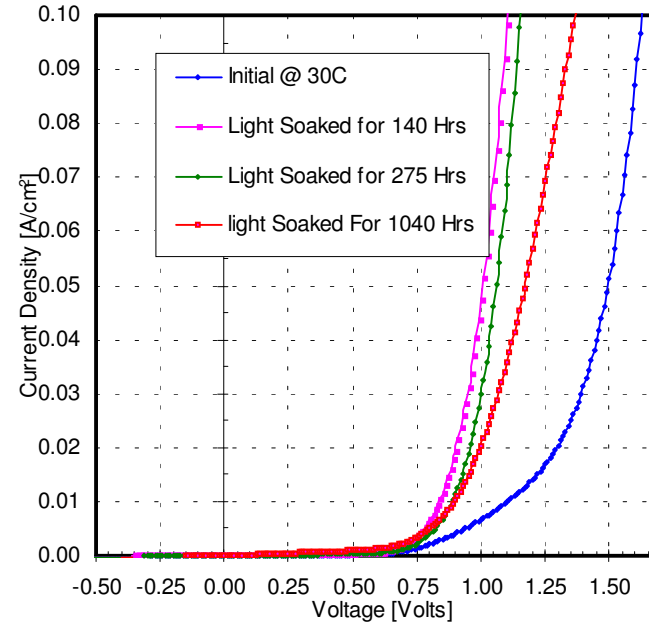
390⁰ C



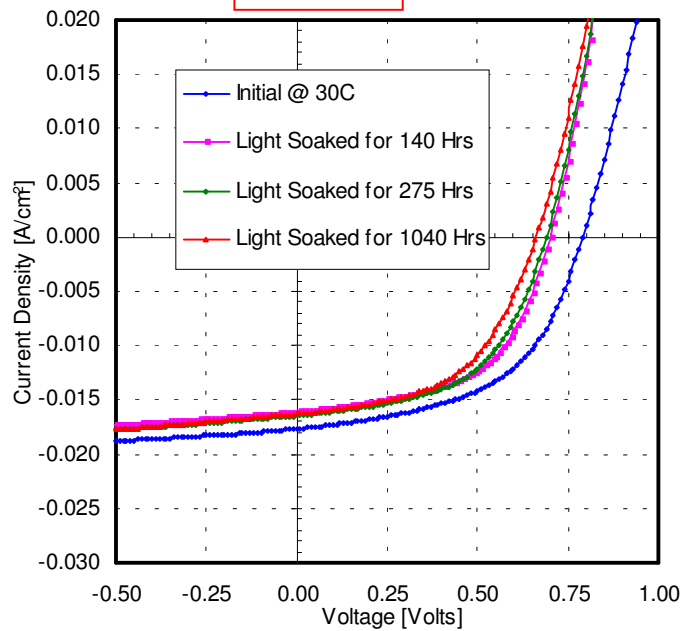
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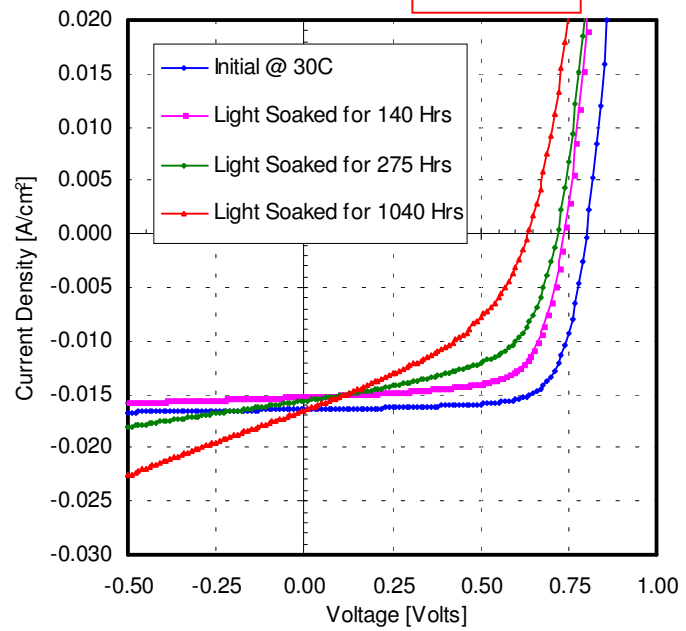
400⁰ C



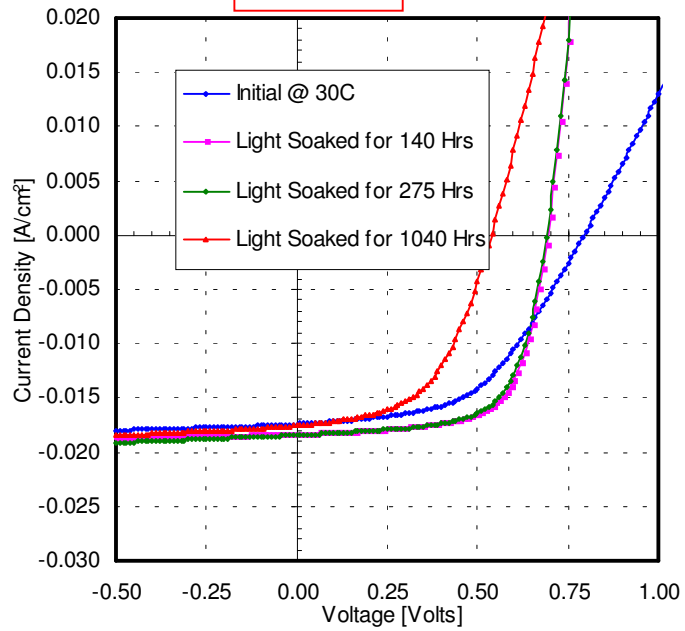
360 ° C



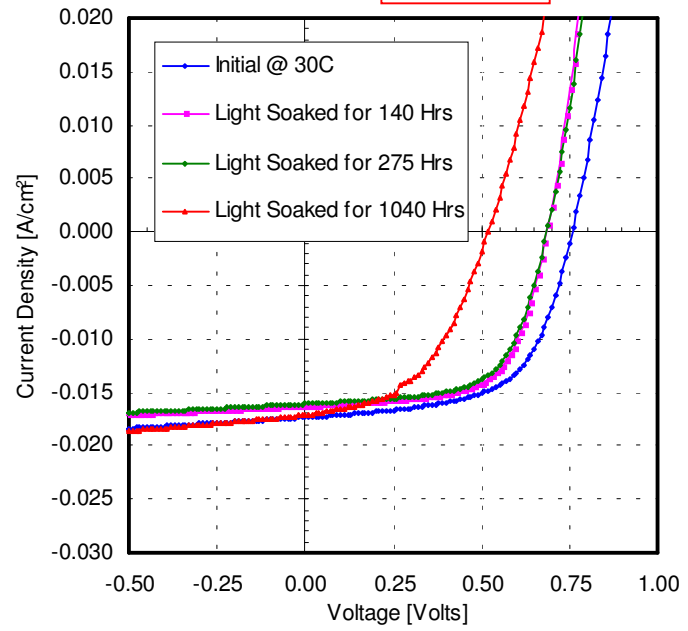
390 ° C

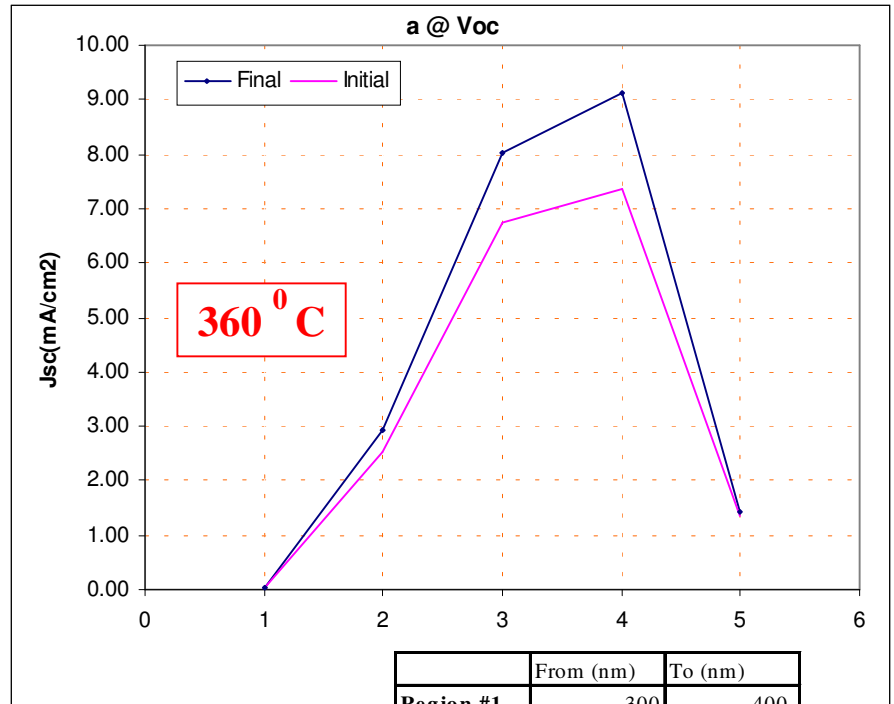
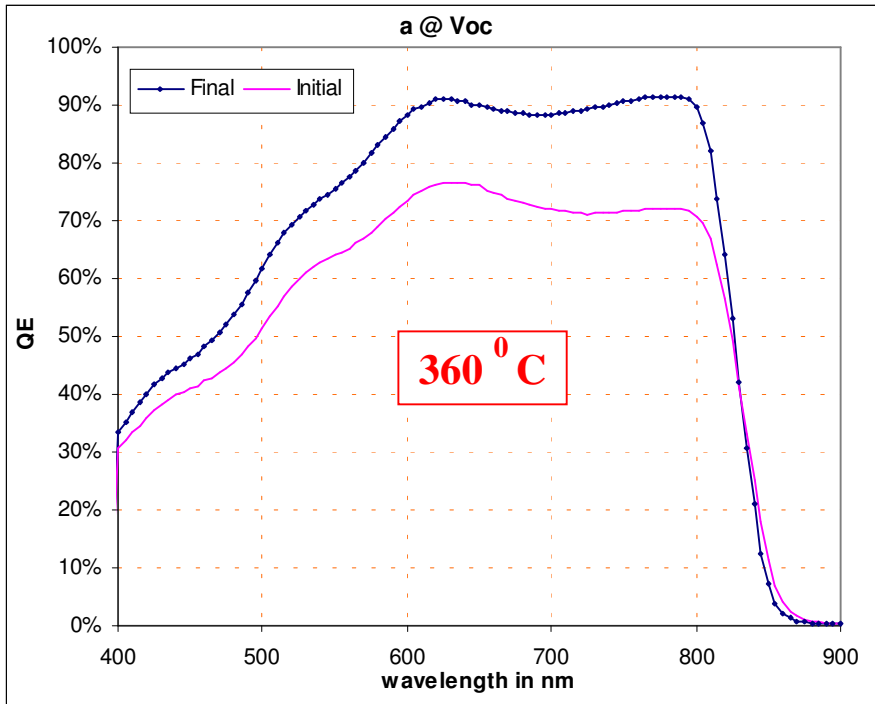


380 ° C

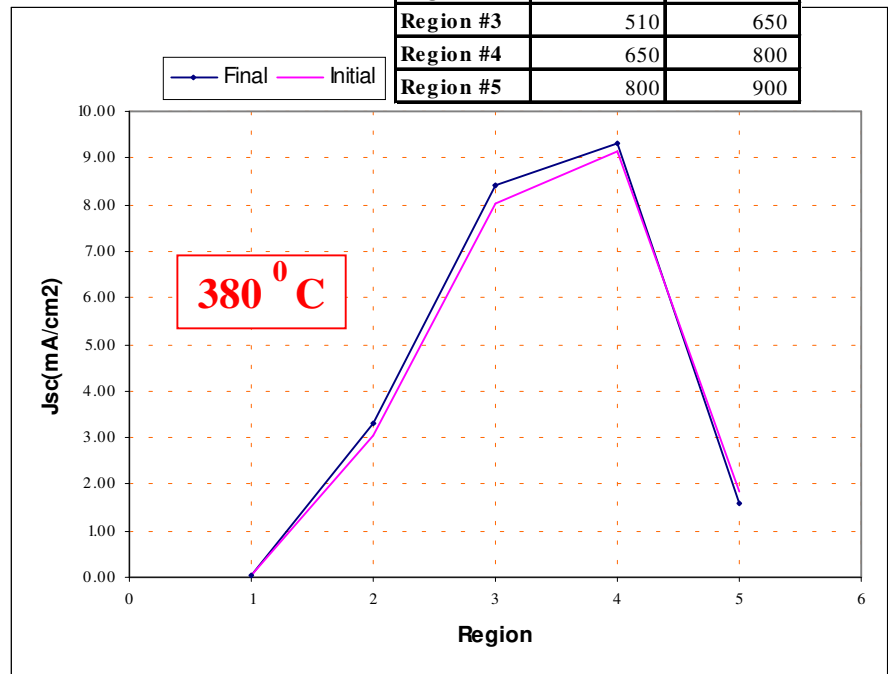
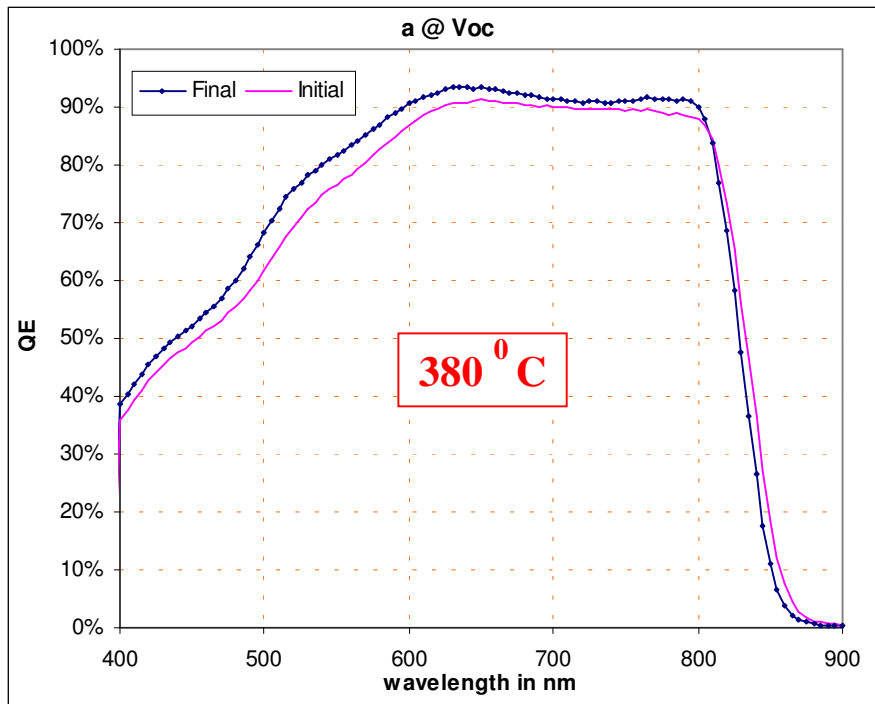


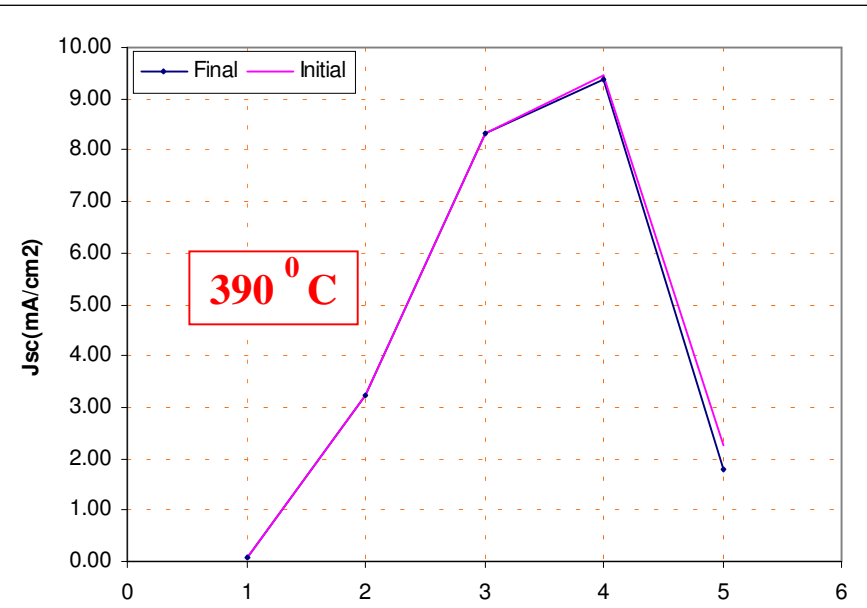
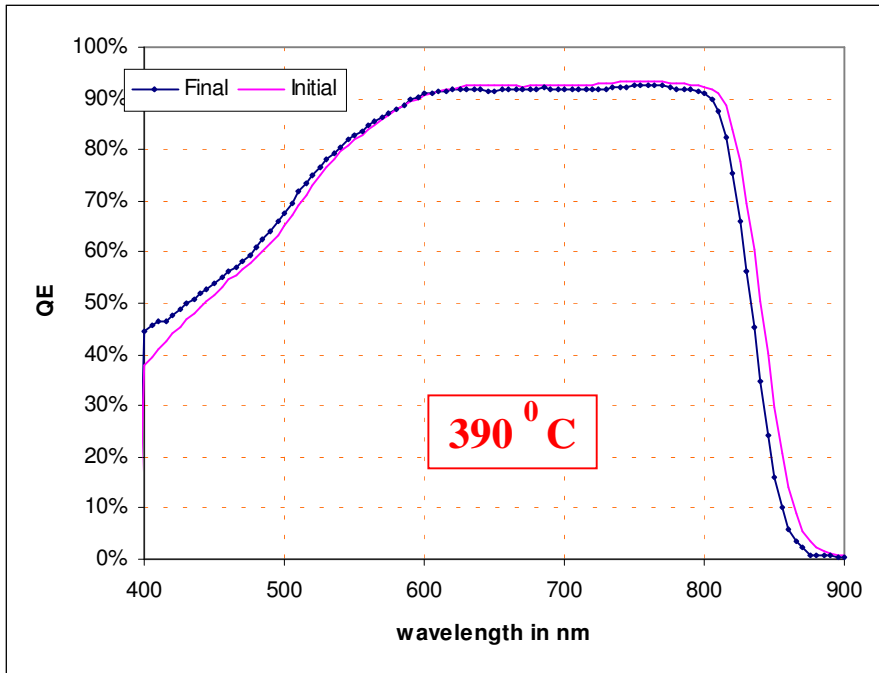
400 ° C



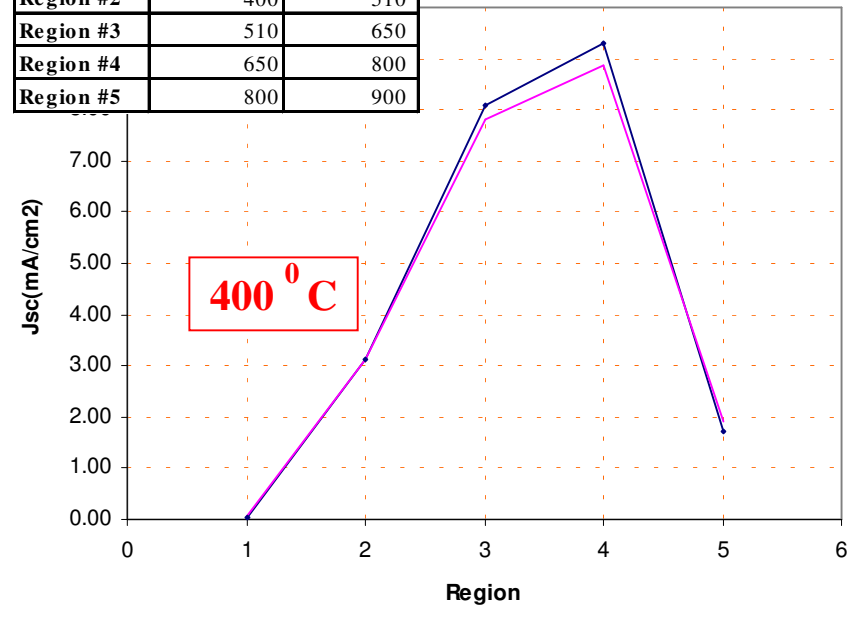
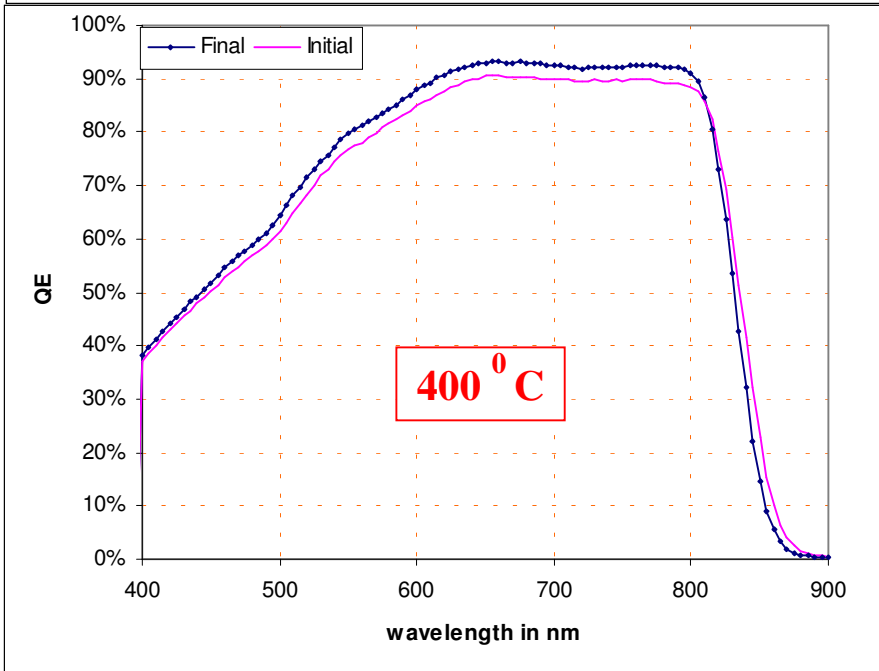


	From (nm)	To (nm)
Region #1	300	400
Region #2	400	510
Region #3	510	650
Region #4	650	800
Region #5	800	900





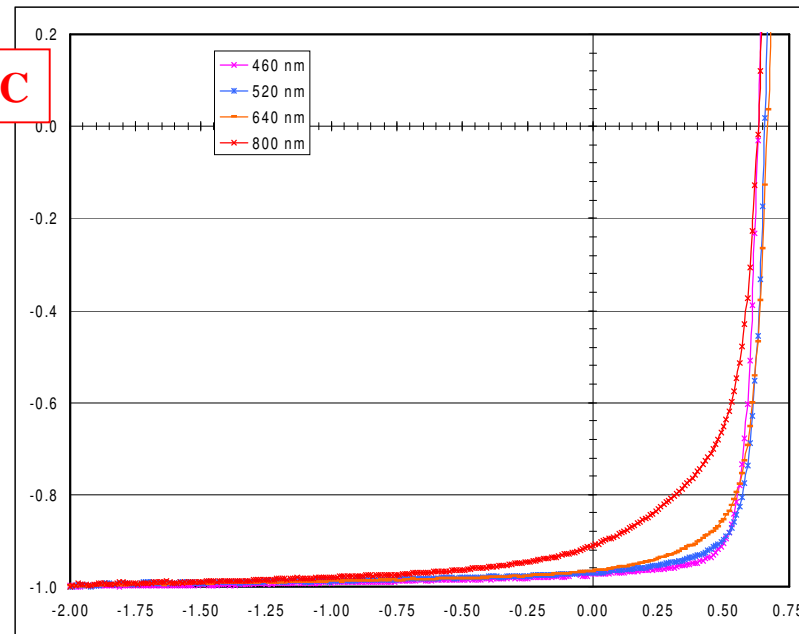
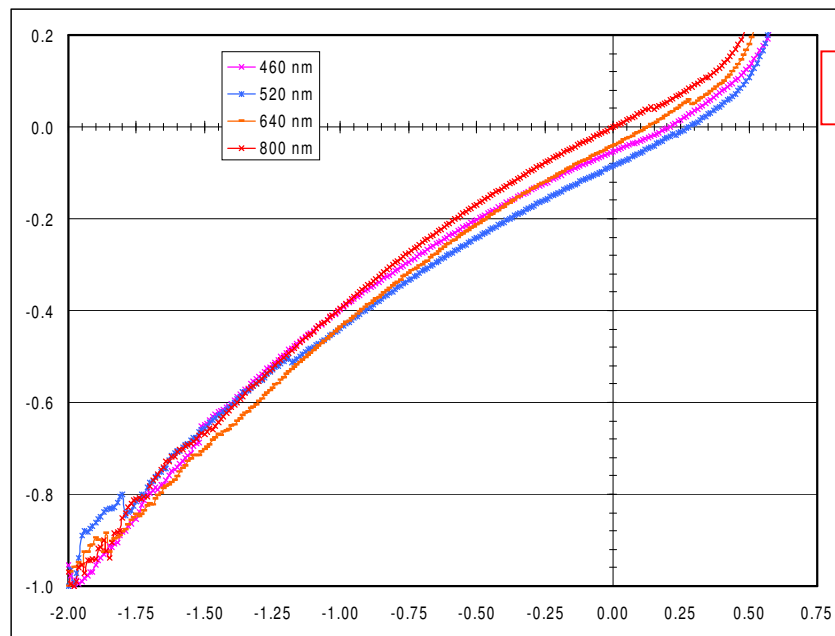
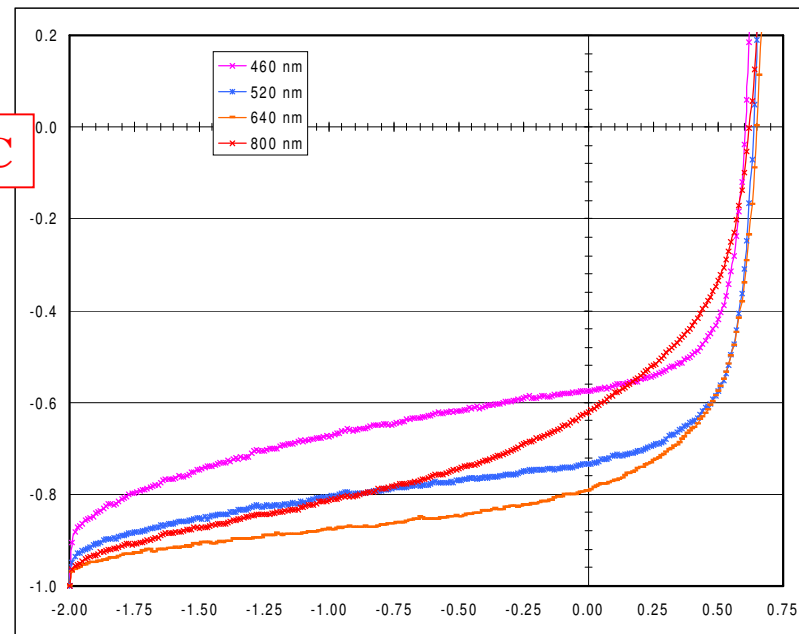
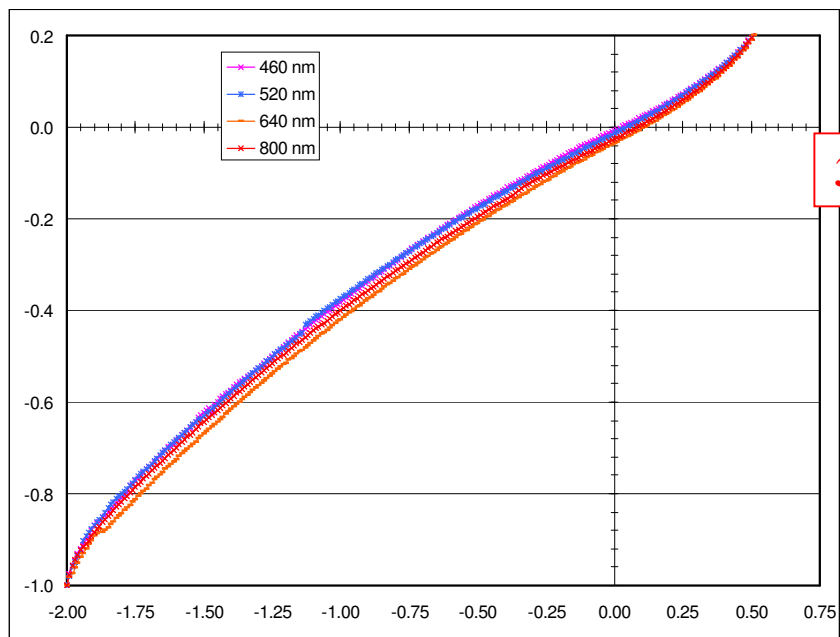
	From (nm)	To (nm)	Region
Region #1	300	400	
Region #2	400	510	
Region #3	510	650	
Region #4	650	800	
Region #5	800	900	



After 1000 Hrs

Color JV

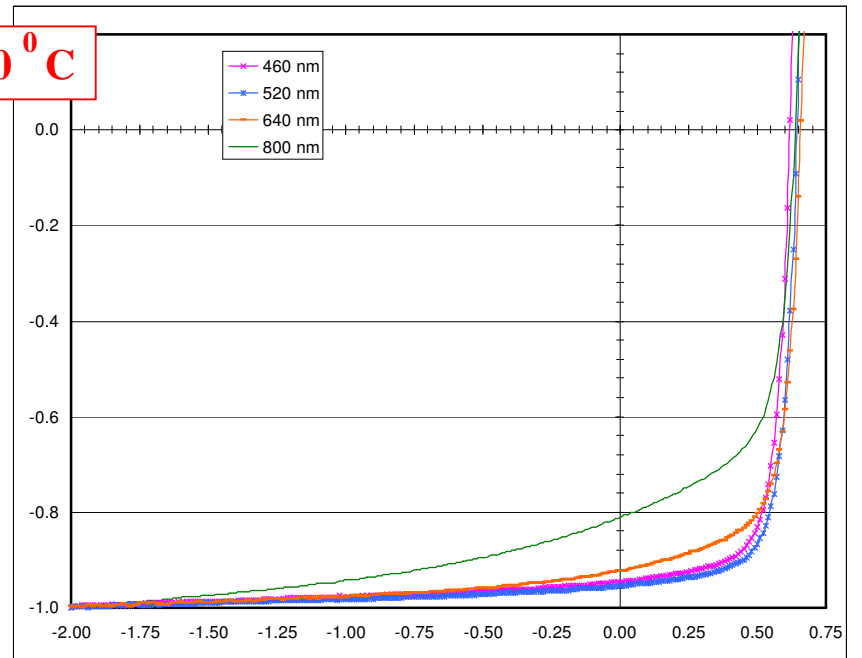
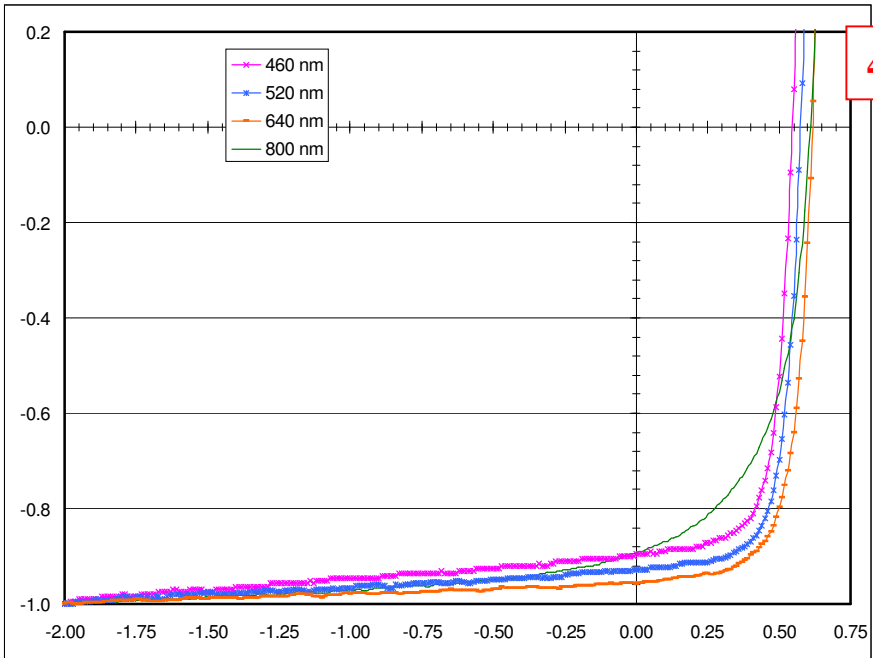
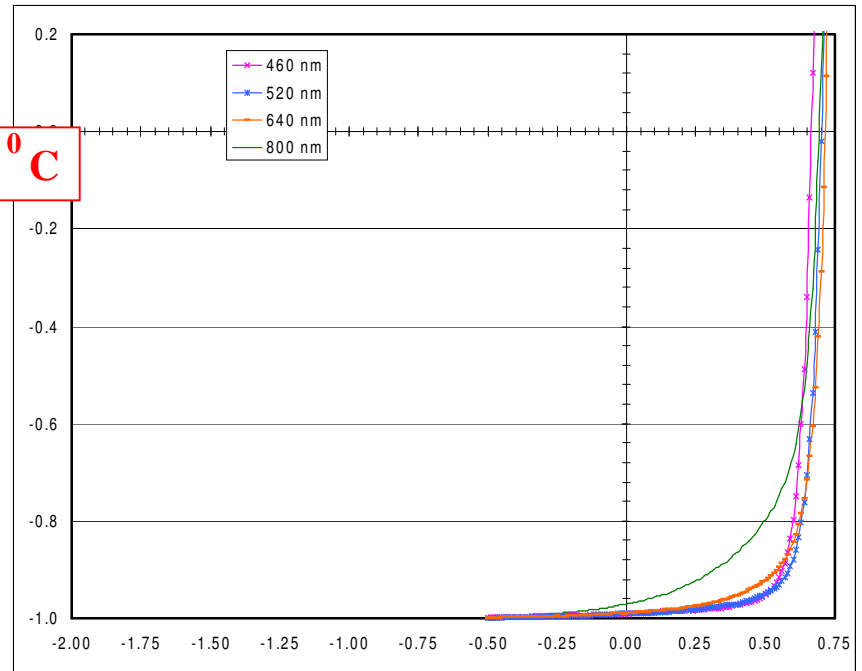
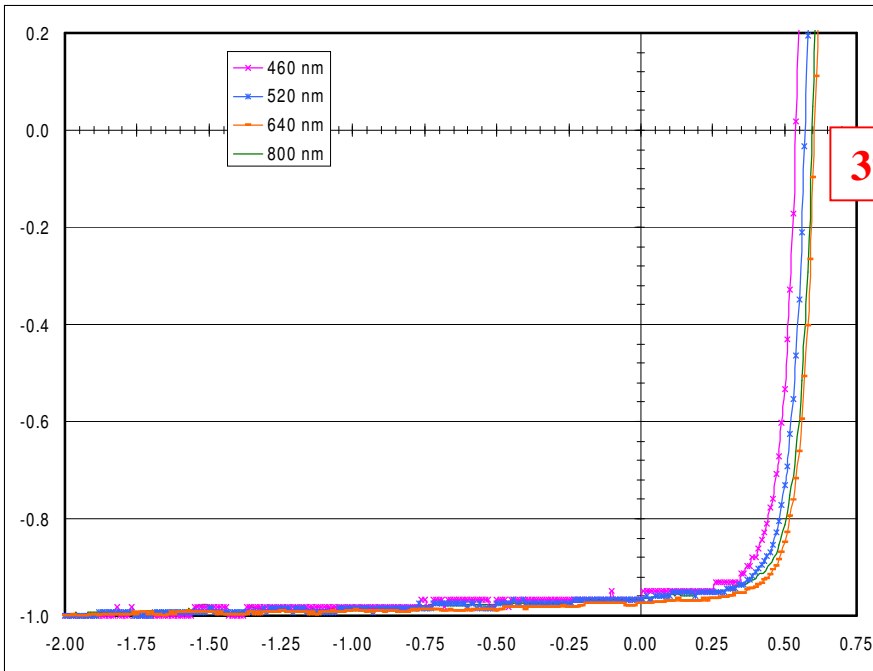
Initial



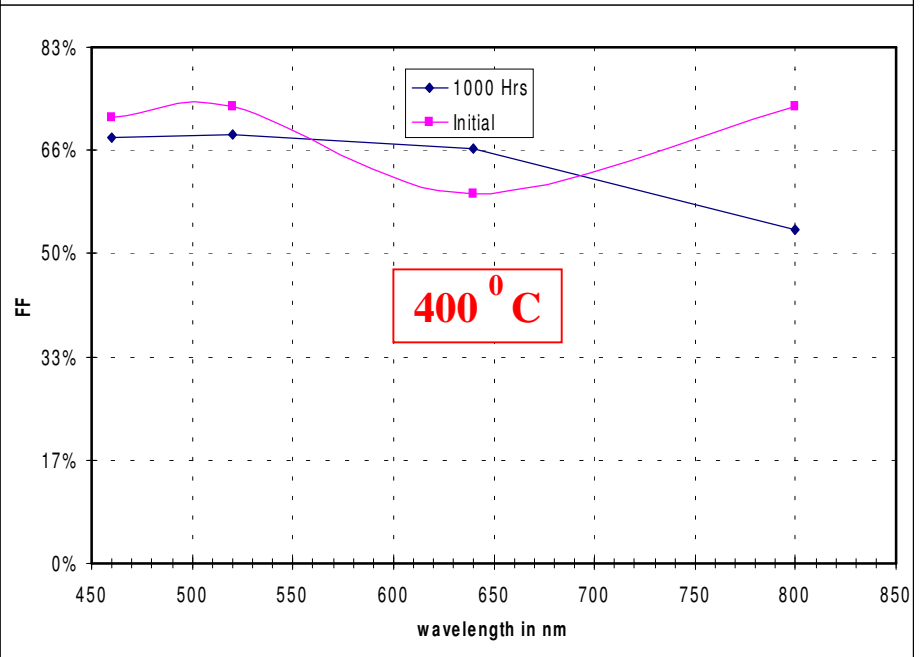
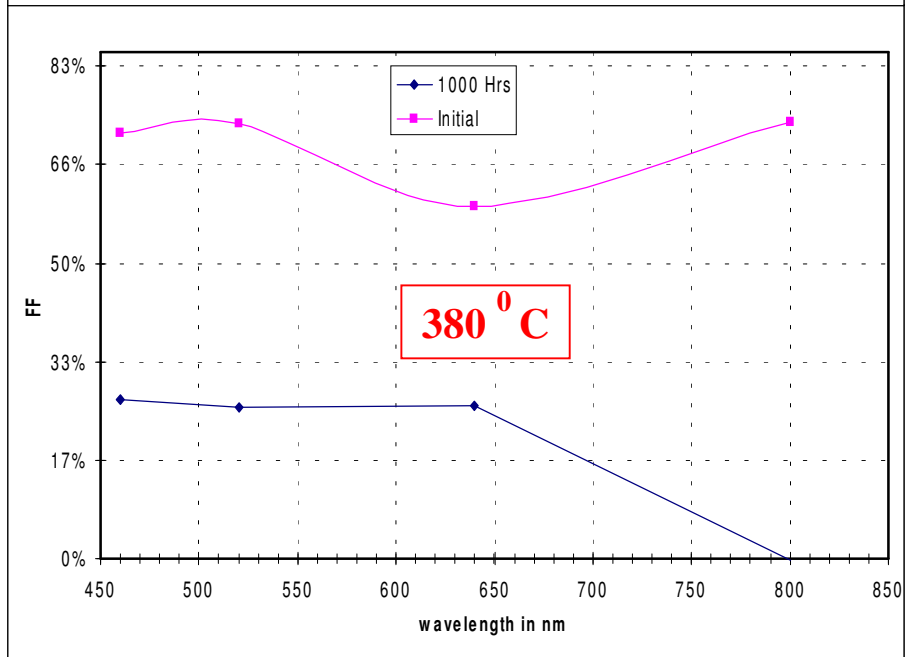
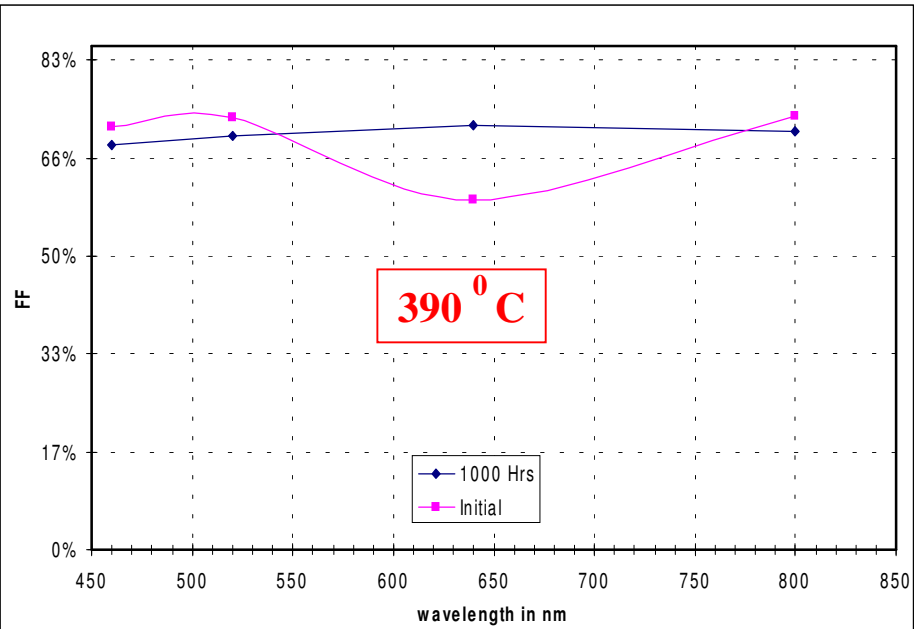
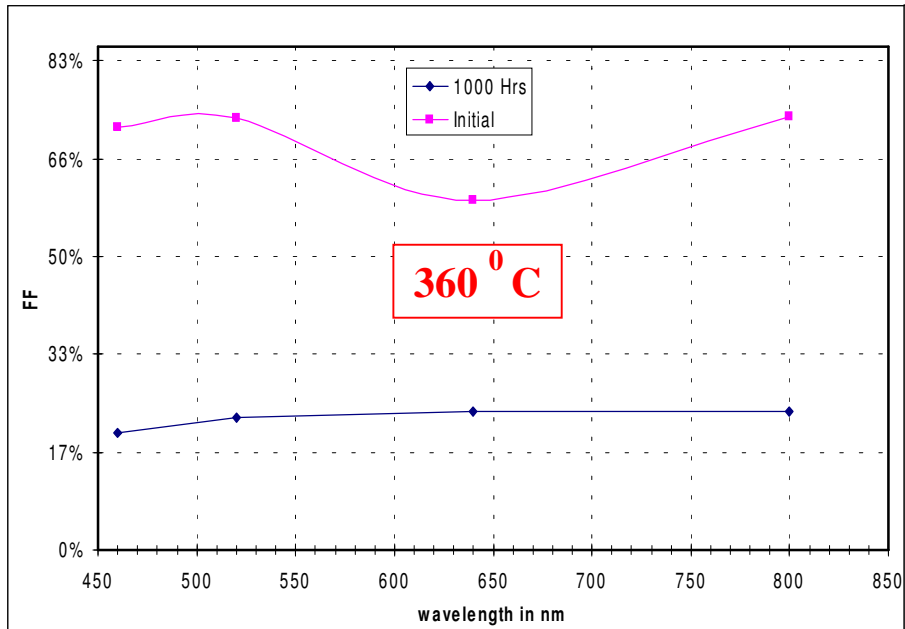
After 1000 Hrs

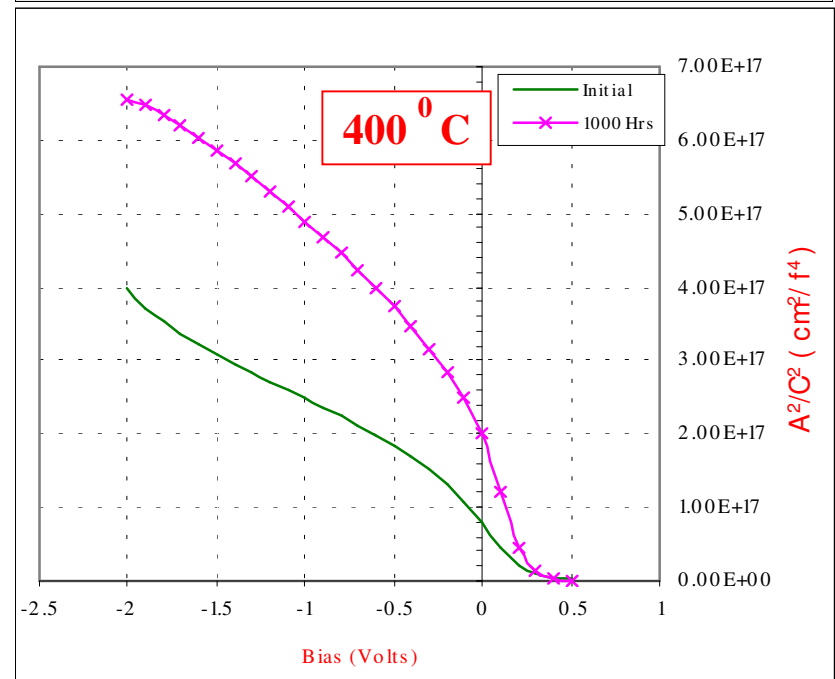
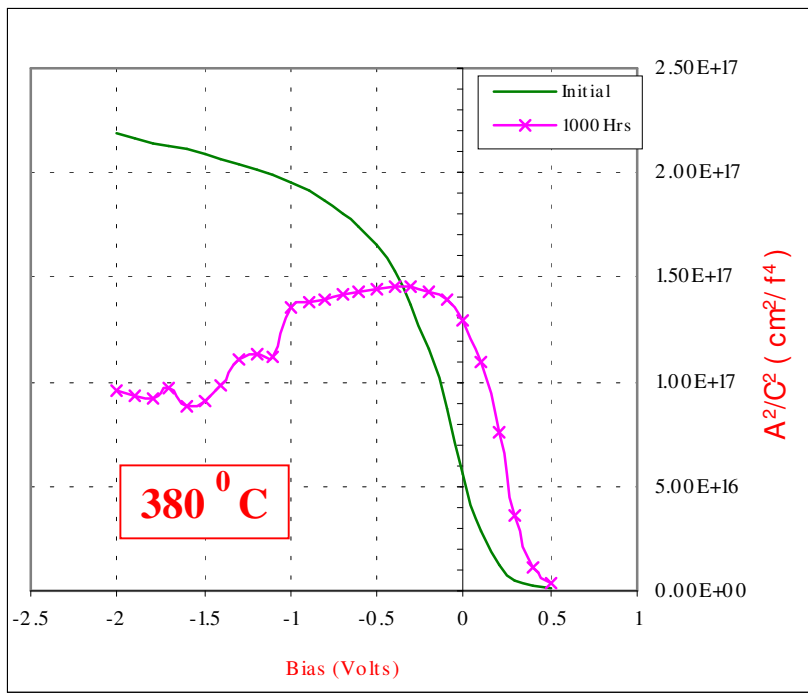
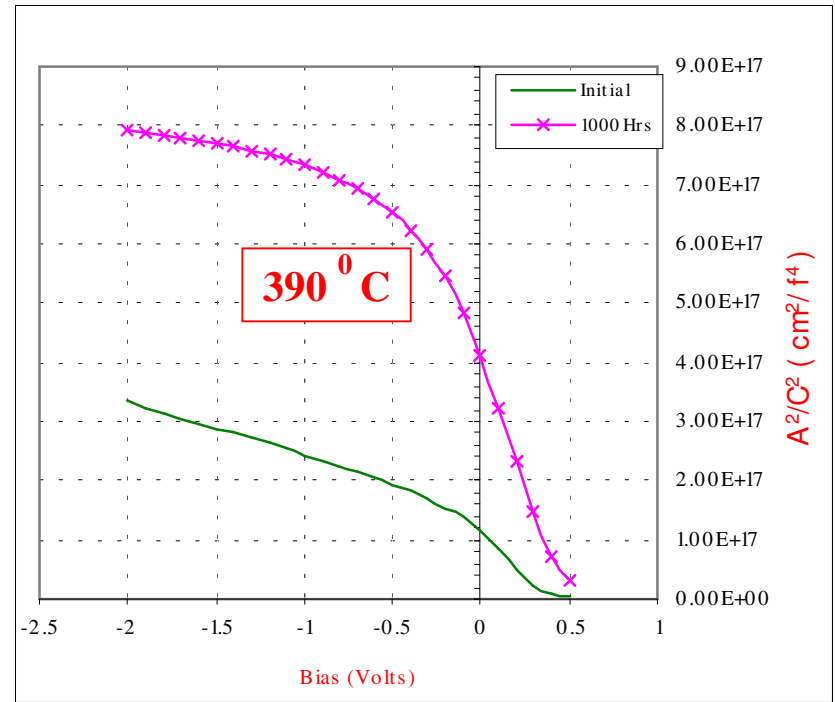
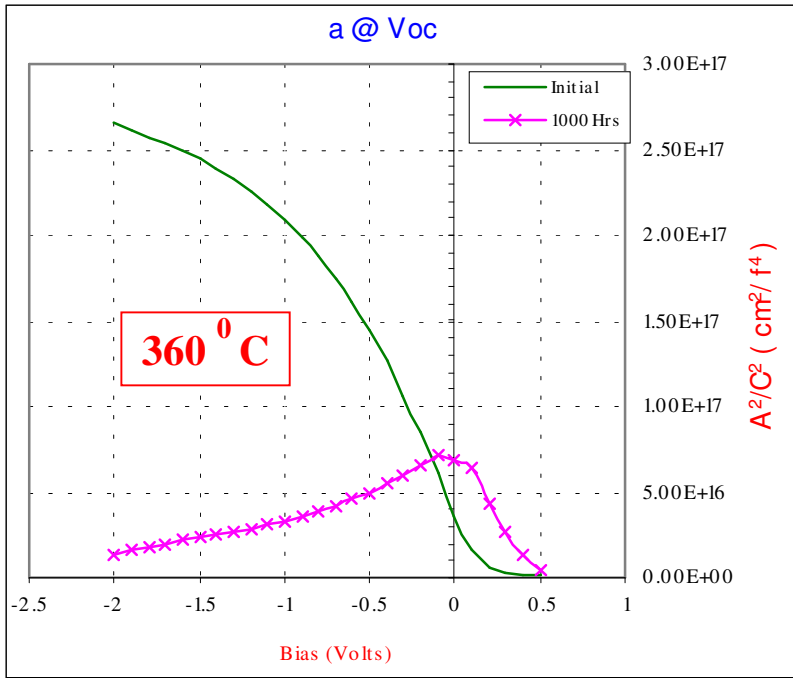
Color JV

Initial

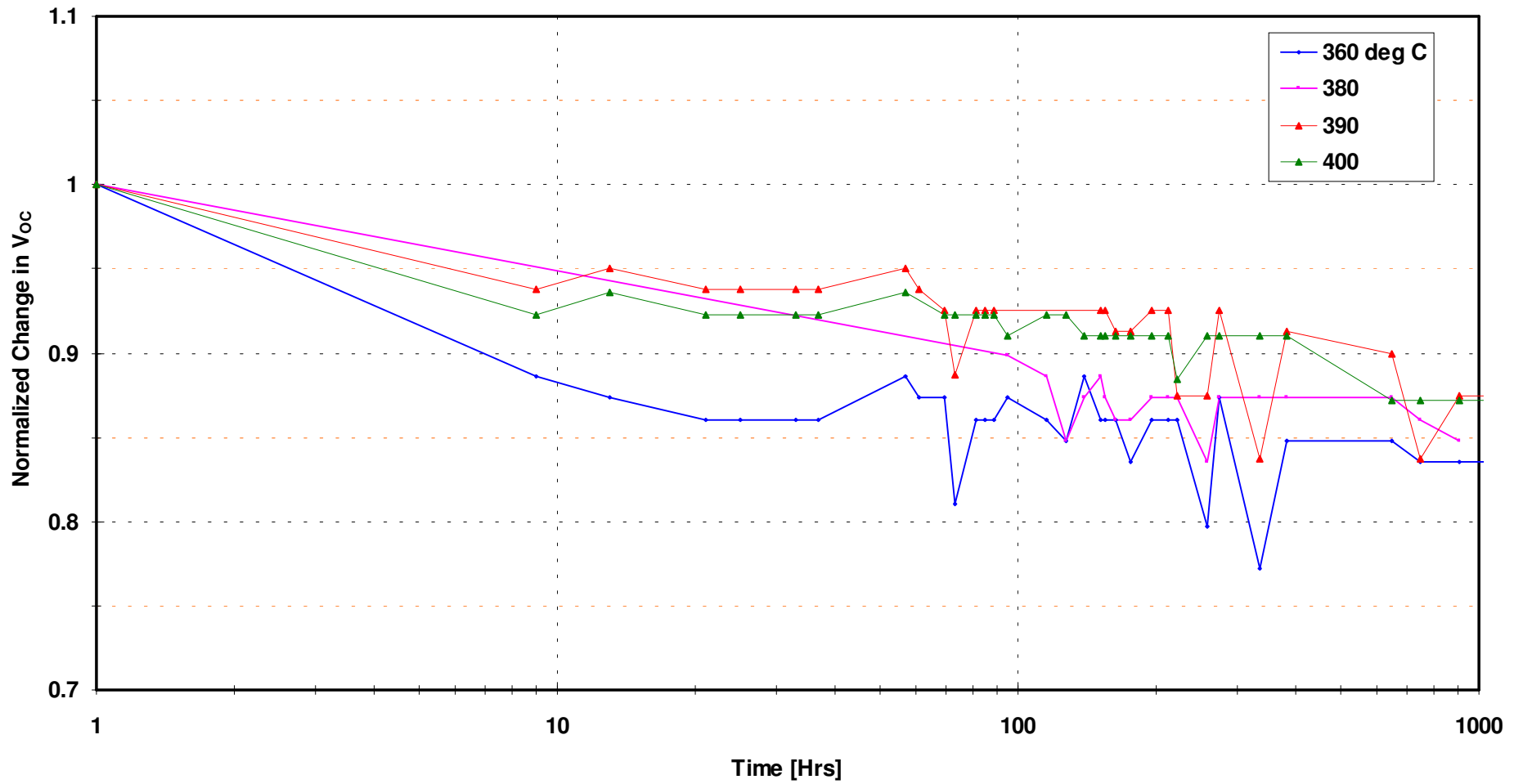


Change in FF in Color JV

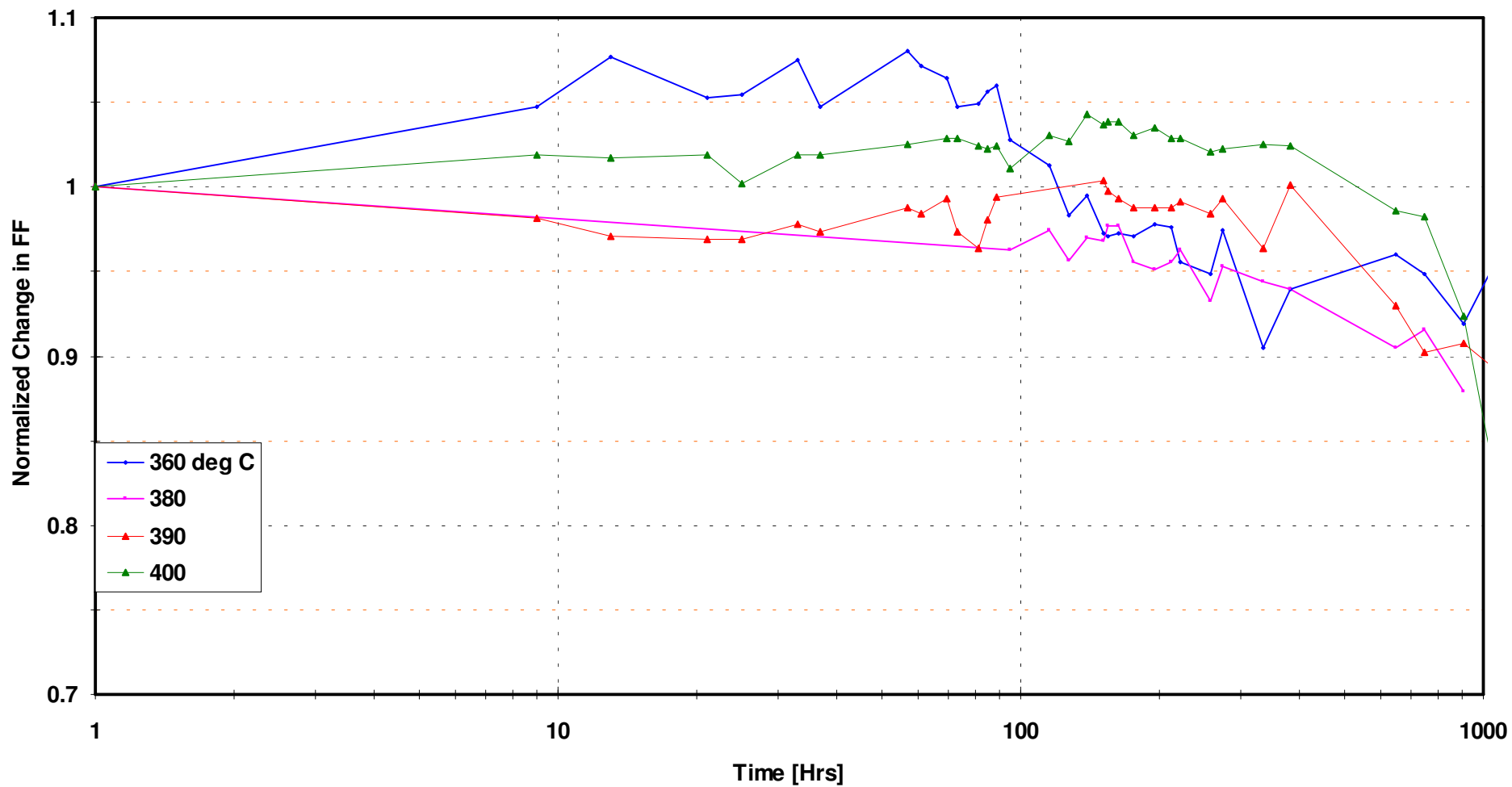




Normalized change in Voc @ open circuit condition



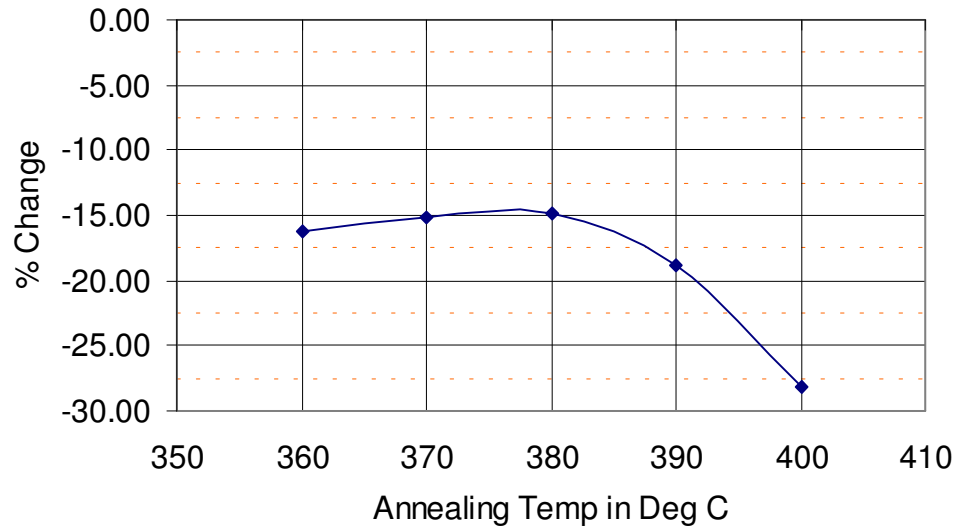
Normalized change in FF @ open circuit condition



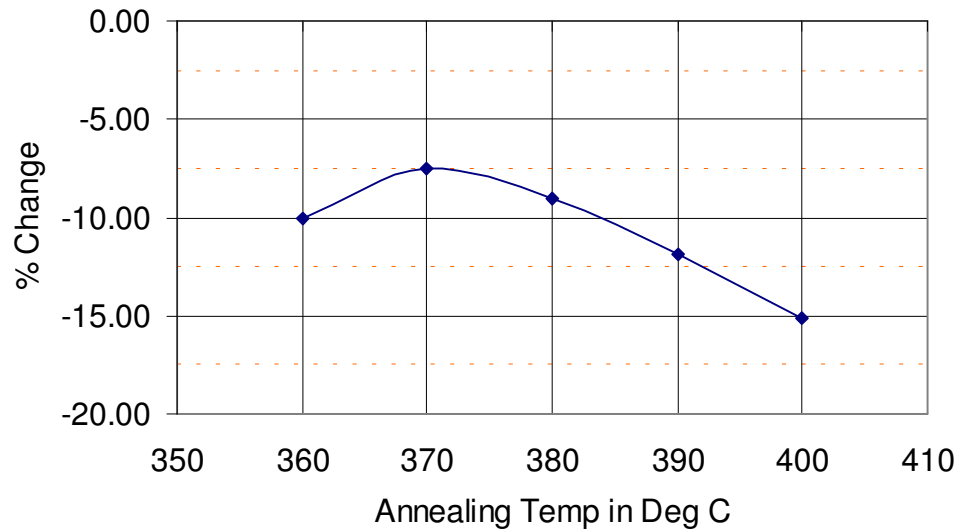
Post Annealing Effect on device stability

Summary

% Change in Voc @ Voc



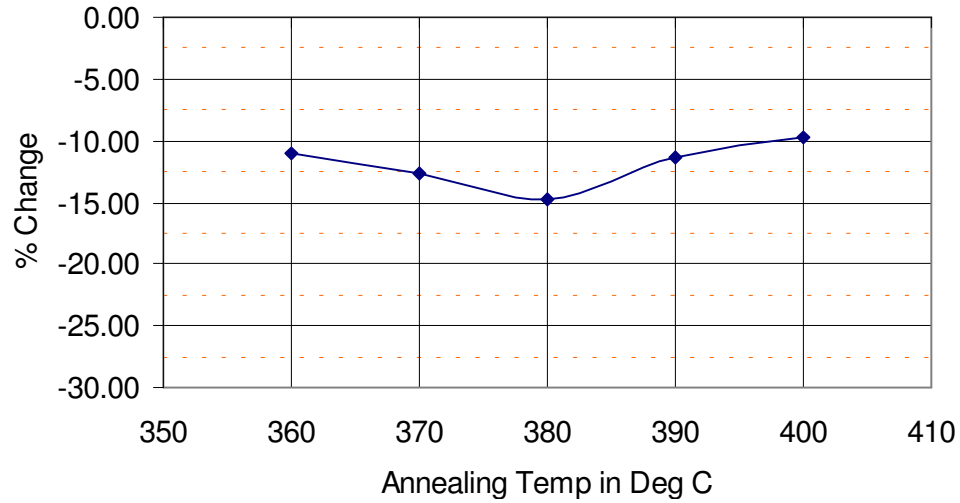
% Change in FF @ Voc



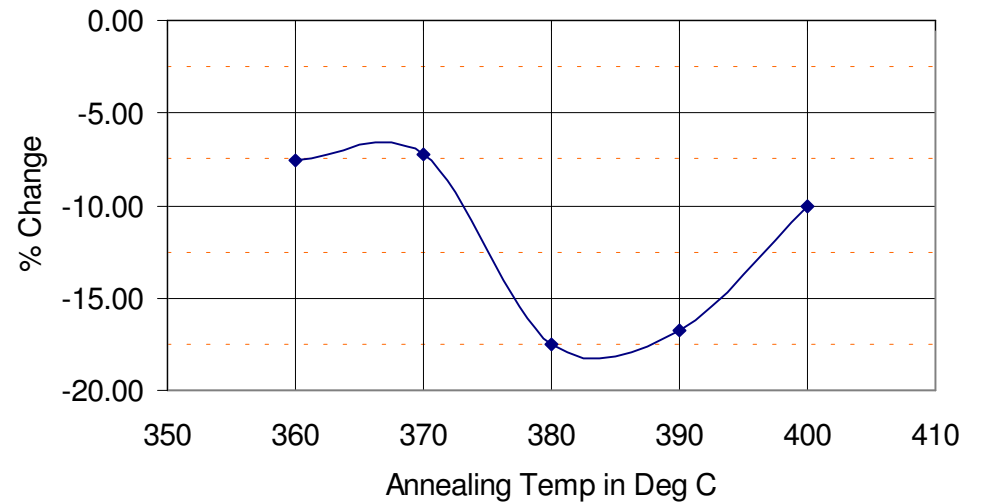
Post Annealing Effect on device stability

Summary

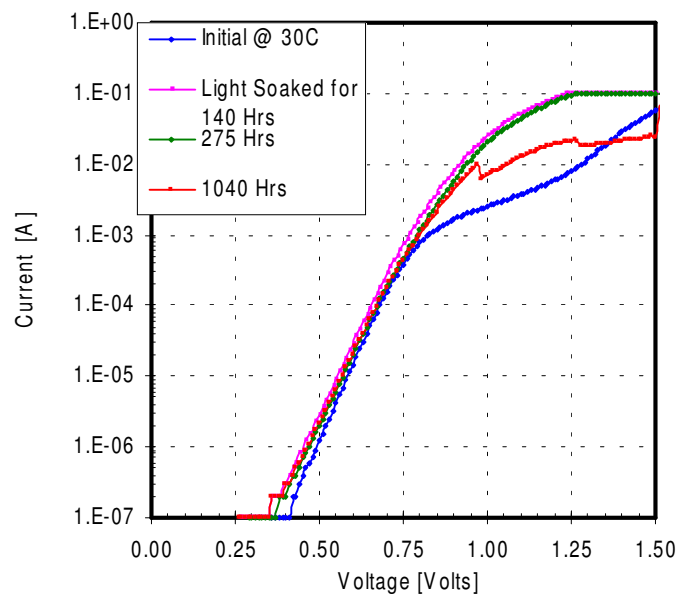
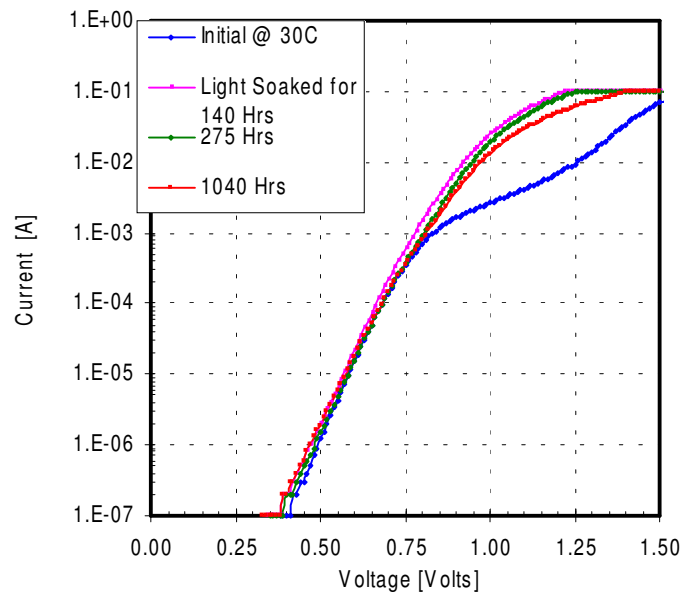
% Change in Voc @ Jsc



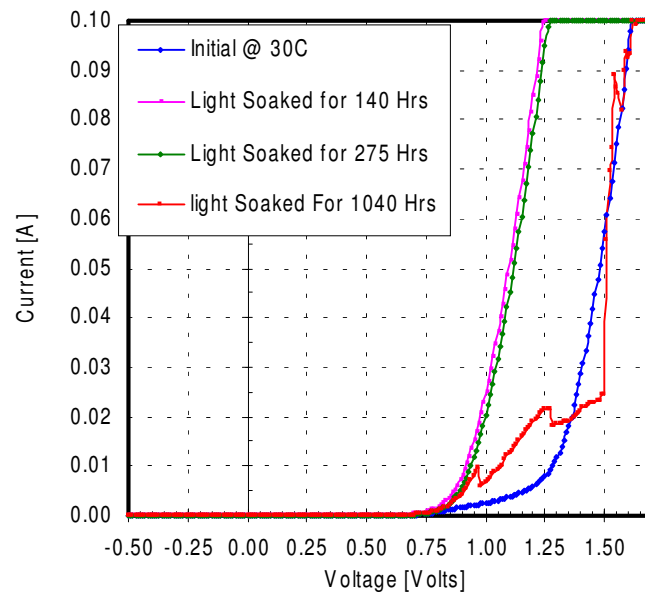
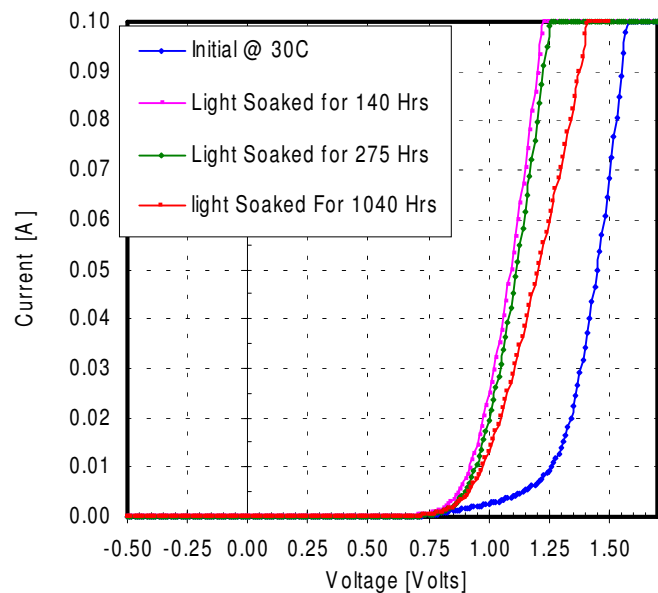
% Change in FF @ Jsc



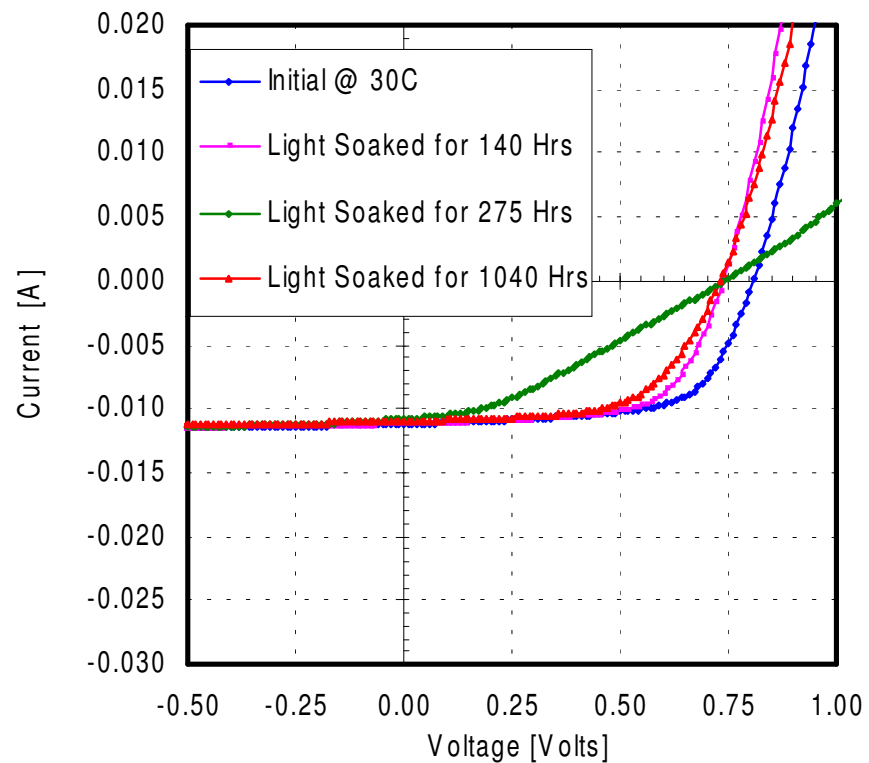
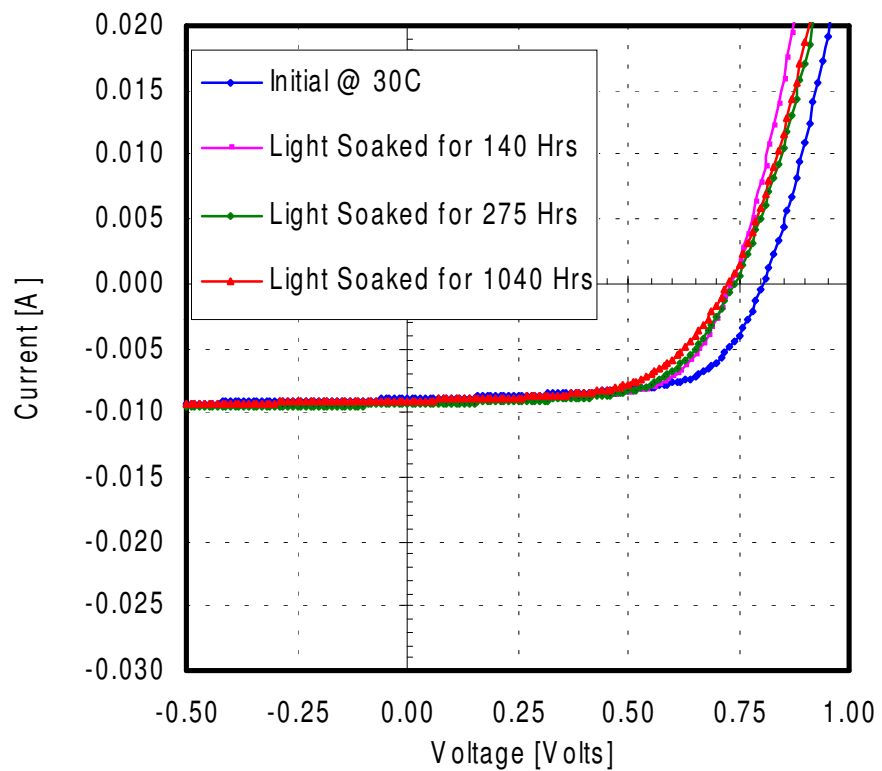
CuCl on CdS



Dark I-V



CuCl on CdS



Future Work

- Integrate and Calibrate measurement system for automation
- Stability analysis of CdTe samples with Cu treatment in different layers
- Analyze the possible degradation mechanisms using present results