MF1518-03

S1D15G14 Series

Rev.1.4

NOTICE

CONTENTS

1. DESCRIPTION

The S1D15G14 is the LCD drivers equipped with the LCD drive power circuit to realize color display with one chip.

The S1D15G14 can be connected to a microprocessor directly, display data are stored in the on-chip display data RAM (=DDRAM). And 312 segment outputs and 82 common outputs are generated for driving LCD. It incorporates the DDRAM with capacity of 312×4(16 gray scale)×84. A single dot of pixel on the LCD corresponds to 4bits of the DDRAM, enabling to display 104(RGB)×82 pixels with one chip. Also accurate LCD driving voltages are generated with built-in power supply circuit.

2. FEATURES

LCD driving

- 312 segment and 82 common LCD drive output
- 4096 colors, or 256 colors from 4096 colors (Normal mode), 8 colors(Idle mode) can be displayed
- PWM grayscale drive by conventional driving
- LCD driving duty selectable : 1/82duty, 1/67duty
- Partial display
- Correspondence between DDRAM and LCD
  Bit data of DDRAM "0,0,0,0" ··· OFF
  "1,1,1,1" ··· ON
  *ON/OFF indicate if voltage is applied to the LCD at the time of normal display.
- DDRAM capacity : 312×4×84=104,832bits

MPU interface

- 2 types of serial interface are available : 8bits, 9bits (D/C + 8bit data)
- Parallel interface is available

Built in circuit

- LCD power supply circuit
  voltage booster, voltage divider and voltage follower : bias ratio 1/9,1/8,1/7,1/6,1/5 selectable
  voltage regulator : high accurate
- Built-in CR oscillator

Power supply

- Power supply voltage
  Input/Output power supply : V_{DDI}-GND= 1.6V to 3.6V
  Internal power supply : V_{DD}-GND= 2.35V to 3.6V
  LCD driving power supply : V_2-MV_2= 10.0V to 25.5V
- Current consumption : 400μA(1/6bias, 85Hz frame frequency, Vseg= 3.3V, normal mode)

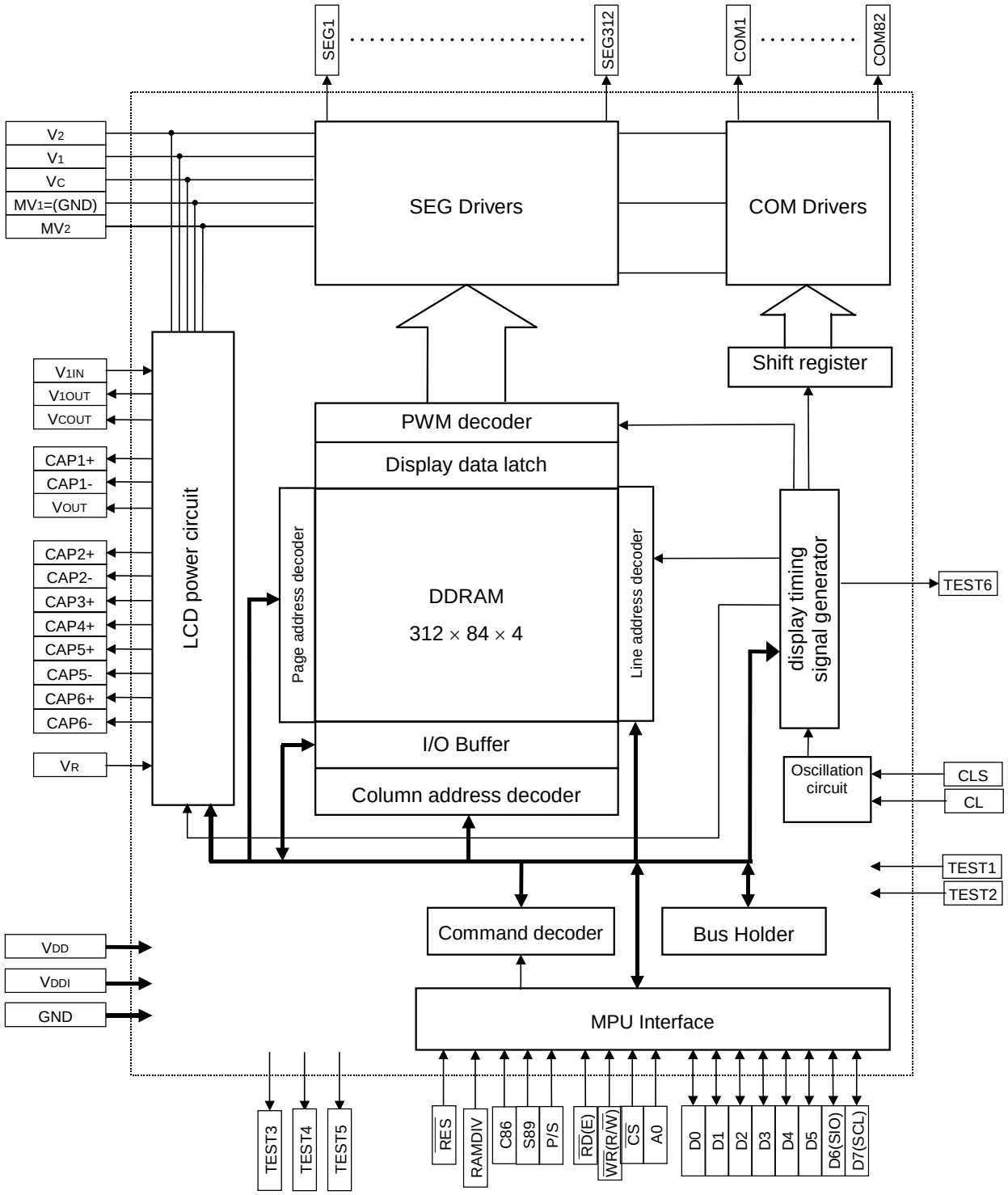
Others

- Shipping form : Au bump bare chip
- Wide range of operating temperatures -40 to +85°C

Notice

- This IC is not designed for strong radio/optical activity proof.

3. BLOCK DIAGRAM



5. PIN COORDINATES

Unit: μm

Pin No.	Pin Name	X	Y
1	CAP6-	-6971.1	-856.5
2	CAP6-	-6871.1	
3	CAP6-	-6771.1	
4	CAP6+	-6637.1	
5	CAP6+	-6537.1	
6	CAP6+	-6437.1	
7	CAP5-	-6303.1	
8	CAP5-	-6203.1	
9	CAP5-	-6103.1	
10	CAP5+	-5969.1	
11	CAP5+	-5869.1	
12	CAP5+	-5769.1	
13	CAP2-	-5635.1	
14	CAP2-	-5535.1	
15	CAP2-	-5435.1	
16	CAP2+	-5301.1	
17	CAP2+	-5201.1	
18	CAP2+	-5101.1	
19	CAP4+	-4967.1	
20	CAP4+	-4867.1	
21	CAP4+	-4767.1	
22	CAP3-	-4633.1	
23	CAP3-	-4533.1	
24	CAP3-	-4433.1	
25	CAP3+	-4299.1	
26	CAP3+	-4199.1	
27	CAP3+	-4099.1	
28	V_2	-3965.1	
29	V_2	-3865.1	
30	V_2	-3765.1	
31	MV_2	-3631.1	
32	MV_2	-3531.1	
33	MV_2	-3431.1	
34	$\overline{RES}$	-3297.1	
35	$\overline{RES}$	-3197.1	
36	$\overline{RES}$	-3063.1	
37	$\overline{CS}$	-2909.1	
38	GND *1	-2755.1	
39	$\overline{WR}$	-2621.1	
40	$\overline{RD}$	-2467.1	
41	V_{DDI} *1	-2313.1	
42	A0	-2179	
43	GND	-2025	
44	GND	-1925	
45	GND	-1825	
46	GND	-1725	
47	GND	-1625	
48	GND	-1525	
49	D0	-1391	
50	D1	-1237	

Pin No.	Pin Name	X	Y
51	D2	-1083	-856.5
52	D3	-929	
53	D4	-775	
54	D5	-621	
55	D6(SIO)	-467	
56	D7(SCL)	-313	
57	TEST6	-159	
58	V_{DDI} *1	-5	
59	RAMDIV	129	
60	GND *1	283	
61	PS	417	
62	V_{DDI} *1	571	
63	C86	705	
64	S89	859	
65	GND *1	1013	
66	TEST1	1147	
67	TEST2	1301	
68	CLS	1455	
69	CL	1609	
70	DUMMY	1763	
71	DUMMY	1875	
72	DUMMY	1987	
73	V_{DDI}	2141	
74	V_{DDI}	2241	
75	V_{DDI}	2341	
76	V_{DDI}	2441	
77	V_{DD}	2575	
78	V_{DD}	2675	
79	V_{DD}	2775	
80	V_{DD}	2875	
81	V_{DD}	2975	
82	V_{DD}	3075	
83	V_{1IN}	3209	
84	V_{OUT}	3309	
85	V_{OUT}	3409	
86	V_{OUT}	3509	
87	V_{1OUT}	3643	
88	V_{1OUT}	3743	
89	V_C	3877	
90	V_C	3977	
91	V_{COUT}	4111	
92	V_{COUT}	4211	
93	V_{1IN}	4345	
94	V_{1IN}	4445	
95	CAP1-	4579	
96	CAP1-	4679	
97	CAP1-	4779	
98	CAP1-	4879	
99	CAP1+	5013	
100	CAP1+	5113	

Pin No.	Pin Name	X	Y
101	CAP1+	5213	-856.5
102	CAP1+	5313	
103	V_R	5447	
104	V_R	5547	
105	V_1	5681	
106	V_1	5781	
107	GND	5915	
108	GND	6015	
109	TEST4	6169	
110	TEST3	6323	
111	V_{DD}	6477	
112	V_{DD}	6577	
113	TEST5	6711	
114	TEST5	6865	
115	TEST5	6965	
116	DUMMY	7212.15	-876
117	DUMMY		-816
118	COM41		-756
119	COM40		-696
120	COM39		-636
121	COM38		-576
122	COM37		-516
123	COM36		-456
124	COM35		-396
125	COM34		-336
126	COM33		-276
127	COM32		-216
128	COM31		-156
129	COM30		-96
130	COM29		-36
131	COM28		24
132	COM27		84
133	COM26		144
134	COM25		204
135	COM24		264
136	COM23		324
137	COM22		384
138	DUMMY		444
139	DUMMY		504
140	DUMMY		564
141	DUMMY	7228	836.5
142	DUMMY	7186	
143	DUMMY	7144	
144	DUMMY	7102	
145	COM21	7060	
146	COM20	7020	
147	COM19	6980	
148	COM18	6940	
149	COM17	6900	
150	COM16	6860	

Unit: μm

Pin No.	Pin Name	X	Y
151	COM15	6820	836.5
152	COM14	6780	
153	COM13	6740	
154	COM12	6700	
155	COM11	6660	
156	COM10	6620	
157	COM9	6580	
158	COM8	6540	
159	COM7	6500	
160	COM6	6460	
161	COM5	6420	
162	COM4	6380	
163	COM3	6340	
164	COM2	6300	
165	COM1	6260	
166	SEG312	6220	
167	SEG311	6180	
168	SEG310	6140	
169	SEG309	6100	
170	SEG308	6060	
171	SEG307	6020	
172	SEG306	5980	
173	SEG305	5940	
174	SEG304	5900	
175	SEG303	5860	
176	SEG302	5820	
177	SEG301	5780	
178	SEG300	5740	
179	SEG299	5700	
180	SEG298	5660	
181	SEG297	5620	
182	SEG296	5580	
183	SEG295	5540	
184	SEG294	5500	
185	SEG293	5460	
186	SEG292	5420	
187	SEG291	5380	
188	SEG290	5340	
189	SEG289	5300	
190	SEG288	5260	
191	SEG287	5220	
192	SEG286	5180	
193	SEG285	5140	
194	SEG284	5100	
195	SEG283	5060	
196	SEG282	5020	
197	SEG281	4980	
198	SEG280	4940	
199	SEG279	4900	
200	SEG278	4860	

Pin No.	Pin Name	X	Y
201	SEG277	4820	836.5
202	SEG276	4780	
203	SEG275	4740	
204	SEG274	4700	
205	SEG273	4660	
206	SEG272	4620	
207	SEG271	4580	
208	SEG270	4540	
209	SEG269	4500	
210	SEG268	4460	
211	SEG267	4420	
212	SEG266	4380	
213	SEG265	4340	
214	SEG264	4300	
215	SEG263	4260	
216	SEG262	4220	
217	SEG261	4180	
218	SEG260	4140	
219	SEG259	4100	
220	SEG258	4060	
221	SEG257	4020	
222	SEG256	3980	
223	SEG255	3940	
224	SEG254	3900	
225	SEG253	3860	
226	SEG252	3820	
227	SEG251	3780	
228	SEG250	3740	
229	SEG249	3700	
230	SEG248	3660	
231	SEG247	3620	
232	SEG246	3580	
233	SEG245	3540	
234	SEG244	3500	
235	SEG243	3460	
236	SEG242	3420	
237	SEG241	3380	
238	SEG240	3340	
239	SEG239	3300	
240	SEG238	3260	
241	SEG237	3220	
242	SEG236	3180	
243	SEG235	3140	
244	SEG234	3100	
245	SEG233	3060	
246	SEG232	3020	
247	SEG231	2980	
248	SEG230	2940	
249	SEG229	2900	
250	SEG228	2860	

Pin No.	Pin Name	X	Y
251	SEG227	2820	836.5
252	SEG226	2780	
253	SEG225	2740	
254	SEG224	2700	
255	SEG223	2660	
256	SEG222	2620	
257	SEG221	2580	
258	SEG220	2540	
259	SEG219	2500	
260	SEG218	2460	
261	SEG217	2420	
262	SEG216	2380	
263	SEG215	2340	
264	SEG214	2300	
265	SEG213	2260	
266	SEG212	2220	
267	SEG211	2180	
268	SEG210	2140	
269	SEG209	2100	
270	SEG208	2060	
271	SEG207	2020	
272	SEG206	1980	
273	SEG205	1940	
274	SEG204	1900	
275	SEG203	1860	
276	SEG202	1820	
277	SEG201	1780	
278	SEG200	1740	
279	SEG199	1700	
280	SEG198	1660	
281	SEG197	1620	
282	SEG196	1580	
283	SEG195	1540	
284	SEG194	1500	
285	SEG193	1460	
286	SEG192	1420	
287	SEG191	1380	
288	SEG190	1340	
289	SEG189	1300	
290	SEG188	1260	
291	SEG187	1220	
292	SEG186	1180	
293	SEG185	1140	
294	SEG184	1100	
295	SEG183	1060	
296	SEG182	1020	
297	SEG181	980	
298	SEG180	940	
299	SEG179	900	
300	SEG178	860	

Unit: μm

Pin No.	Pin Name	X	Y
301	SEG177	820	836.5
302	SEG176	780	
303	SEG175	740	
304	SEG174	700	
305	SEG173	660	
306	SEG172	620	
307	SEG171	580	
308	SEG170	540	
309	SEG169	500	
310	SEG168	460	
311	SEG167	420	
312	SEG166	380	
313	SEG165	340	
314	SEG164	300	
315	SEG163	260	
316	SEG162	220	
317	SEG161	180	
318	SEG160	140	
319	SEG159	100	
320	SEG158	60	
321	SEG157	20	
322	SEG156	-20	
323	SEG155	-60	
324	SEG154	-100	
325	SEG153	-140	
326	SEG152	-180	
327	SEG151	-220	
328	SEG150	-260	
329	SEG149	-300	
330	SEG148	-340	
331	SEG147	-380	
332	SEG146	-420	
333	SEG145	-460	
334	SEG144	-500	
335	SEG143	-540	
336	SEG142	-580	
337	SEG141	-620	
338	SEG140	-660	
339	SEG139	-700	
340	SEG138	-740	
341	SEG137	-780	
342	SEG136	-820	
343	SEG135	-860	
344	SEG134	-900	
345	SEG133	-940	
346	SEG132	-980	
347	SEG131	-1020	
348	SEG130	-1060	
349	SEG129	-1100	
350	SEG128	-1140	

Pin No.	Pin Name	X	Y
351	SEG127	-1180	836.5
352	SEG126	-1220	
353	SEG125	-1260	
354	SEG124	-1300	
355	SEG123	-1340	
356	SEG122	-1380	
357	SEG121	-1420	
358	SEG120	-1460	
359	SEG119	-1500	
360	SEG118	-1540	
361	SEG117	-1580	
362	SEG116	-1620	
363	SEG115	-1660	
364	SEG114	-1700	
365	SEG113	-1740	
366	SEG112	-1780	
367	SEG111	-1820	
368	SEG110	-1860	
369	SEG109	-1900	
370	SEG108	-1940	
371	SEG107	-1980	
372	SEG106	-2020	
373	SEG105	-2060	
374	SEG104	-2100	
375	SEG103	-2140	
376	SEG102	-2180	
377	SEG101	-2220	
378	SEG100	-2260	
379	SEG99	-2300	
380	SEG98	-2340	
381	SEG97	-2380	
382	SEG96	-2420	
383	SEG95	-2460	
384	SEG94	-2500	
385	SEG93	-2540	
386	SEG92	-2580	
387	SEG91	-2620	
388	SEG90	-2660	
389	SEG89	-2700	
390	SEG88	-2740	
391	SEG87	-2780	
392	SEG86	-2820	
393	SEG85	-2860	
394	SEG84	-2900	
395	SEG83	-2940	
396	SEG82	-2980	
397	SEG81	-3020	
398	SEG80	-3060	
399	SEG79	-3100	
400	SEG78	-3140	

Pin No.	Pin Name	X	Y
401	SEG77	-3180	836.5
402	SEG76	-3220	
403	SEG75	-3260	
404	SEG74	-3300	
405	SEG73	-3340	
406	SEG72	-3380	
407	SEG71	-3420	
408	SEG70	-3460	
409	SEG69	-3500	
410	SEG68	-3540	
411	SEG67	-3580	
412	SEG66	-3620	
413	SEG65	-3660	
414	SEG64	-3700	
415	SEG63	-3740	
416	SEG62	-3780	
417	SEG61	-3820	
418	SEG60	-3860	
419	SEG59	-3900	
420	SEG58	-3940	
421	SEG57	-3980	
422	SEG56	-4020	
423	SEG55	-4060	
424	SEG54	-4100	
425	SEG53	-4140	
426	SEG52	-4180	
427	SEG51	-4220	
428	SEG50	-4260	
429	SEG49	-4300	
430	SEG48	-4340	
431	SEG47	-4380	
432	SEG46	-4420	
433	SEG45	-4460	
434	SEG44	-4500	
435	SEG43	-4540	
436	SEG42	-4580	
437	SEG41	-4620	
438	SEG40	-4660	
439	SEG39	-4700	
440	SEG38	-4740	
441	SEG37	-4780	
442	SEG36	-4820	
443	SEG35	-4860	
444	SEG34	-4900	
445	SEG33	-4940	
446	SEG32	-4980	
447	SEG31	-5020	
448	SEG30	-5060	
449	SEG29	-5100	
450	SEG28	-5140	

Unit: μm

Pin No.	Pin Name	X	Y
451	SEG27	-5180	836.5
452	SEG26	-5220	
453	SEG25	-5260	
454	SEG24	-5300	
455	SEG23	-5340	
456	SEG22	-5380	
457	SEG21	-5420	
458	SEG20	-5460	
459	SEG19	-5500	
460	SEG18	-5540	
461	SEG17	-5580	
462	SEG16	-5620	
463	SEG15	-5660	
464	SEG14	-5700	
465	SEG13	-5740	
466	SEG12	-5780	
467	SEG11	-5820	
468	SEG10	-5860	
469	SEG9	-5900	
470	SEG8	-5940	
471	SEG7	-5980	
472	SEG6	-6020	
473	SEG5	-6060	
474	SEG4	-6100	
475	SEG3	-6140	
476	SEG2	-6180	
477	SEG1	-6220	
478	COM42	-6260	
479	COM43	-6300	
480	COM44	-6340	
481	COM45	-6380	
482	COM46	-6420	
483	COM47	-6460	
484	COM48	-6500	
485	COM49	-6540	
486	COM50	-6580	
487	COM51	-6620	
488	COM52	-6660	
489	COM53	-6700	
490	COM54	-6740	
491	COM55	-6780	
492	COM56	-6820	
493	COM57	-6860	
494	COM58	-6900	
495	COM59	-6940	
496	COM60	-6980	
497	COM61	-7020	
498	COM62	-7060	
499	DUMMY	-7102	
500	DUMMY	-7144	

Pin No.	Pin Name	X	Y
501	DUMMY	-7186	836.5
502	DUMMY	-7228	
503	DUMMY	-7212.15	564
504	DUMMY		504
505	DUMMY		444
506	COM63		384
507	COM64		324
508	COM65		264
509	COM66		204
510	COM67		144
511	COM68		84
512	COM69		24
513	COM70		-36
514	COM71		-96
515	COM72		-156
516	COM73		-216
517	COM74		-276
518	COM75		-336
519	COM76		-396
520	COM77		-456
521	COM78		-516
522	COM79		-576
523	COM80		-636
524	COM81		-696
525	COM82		-756
526	DUMMY		-816
527	DUMMY		-876

*1 : V_{DDI} and GND Pins are for pulling up and down. Thus, it can't used for feeding power.
*2 : DUMMY pins are not connected inside the IC.

6. SERIES SPECIFICATIONS

Model name	Die.No	Description
S1D15G14D01B000	D15GED1B	Malfunctions when rewriting the set value after resetting the DISCTL command.
S1D15G14D02B000	D15GED2B or D15GED2S	No application of the above restrictions

※ If considering purchasing our products, contact our sales for detailed information.

7. PIN DESCRIPTION

Power supply pins

Name	I/O	Description	Number of pins
V_{DDI}	Supply	Power supply for Interface circuit	7
V_{DD}	Supply	This is an internal operation power supply. Power supply connected to system V_{CC}.	8
GND	Supply	This IC connected to the system GND.	11
V_2,V_1, V_C,MV_2	Supply	Multi-level power supply for LCD drive. The voltages should maintain the following relationship: $V_2>V_1>V_C>MV_1=GND>MV_2$.	10

LCD power supply circuit pins

Name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor connection pin which generates V_{OUT} from V_C.	4
CAP1-	O	Boosting capacitor connection pin which generates V_{OUT} from V_C.	4
V_{OUT}	O	Booster output.	3
CAP2+	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP2-	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP3+	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP3-	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP4+	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP5+	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP5-	O	Boosting capacitor connection pin which generates MV_2 from V_C as V_{1IN}.	3
CAP6+	O	Boosting capacitor connection pin which generates V_2 from MV_2 as V_C.	3
CAP6-	O	Boosting capacitor connection pin which generates V_2 from MV_2 as V_C.	3

LCD power supply control signal

Name	I/O	Description	Number of pins
V_R	I	Connect external resister for LCD power supply circuit. This terminal is enabled by PWRCTL command. When internal resister is used, this terminal shouldn't be connected. When using a built-in resister, leave this pin open.	2
V_{1IN}	I	Input pin of LCD drive power supply.	3
V_{1OUT}	O	Output pin of LCD drive power supply.	2
V_{COUT}	O	Output pin of LCD drive power supply.	2

System bus connection bus

Name	I/O	Description	Number of pins
D7(SCL)	I/O	P/S=LOW : Serial clock input P/S=HIGH : Parallel data input / output data	1
D6(SIO)	I/O	P/S=LOW : Serial data input P/S=HIGH : Parallel data input / output data	1
D5	I/O	Parallel data bus P/S=LOW : High impedance P/S=HIGH : Parallel data input / output data	1
D4	I/O		1
D3	I/O		1
D2	I/O		1
D1	I/O		1
D0	I/O		1
P/S	I	Choose interface type P/S=LOW : Serial interface P/S=HIGH : Parallel interface	1
C86	I	Choose parallel interface type P/S=LOW : maintained HIGH or LOW P/S=HIGH : HIGH: 80MPU interface, LOW: 68MPU interface	1
S89	I	Choose serial interface type P/S=LOW : HIGH: 8bit serial interface, LOW: 9bit serial interface P/S=HIGH : maintained HIGH or LOW	1
A0	I	Determine whether the data bits are data or command P/S=LOW and S89=LOW: maintained HIGH or LOW Except the above : HIGH: write parameter or display data, LOW: write command	1
$\overline{RD}$(E)	I	Parallell interface read signal P/S=LOW : maintained HIGH or LOW P/S=HIGH : Parallel interface read signal C86= HIGH : Inputs read signals. C86= LOW : Inputs enable signals.	1
$\overline{WR}$(R/$\overline{W}$)	I	Parallel interface write signal P/S=LOW : maintained HIGH or LOW P/S=HIGH : Parallel interface write signal C86= HIGH : Inputs write signals. C86= LOW : Inputs read/write select signals.	1
$\overline{CS}$	I	Chip select input. Data input is enable when $\overline{CS}$ is LOW.	1
RAMDIV	I	Choose Display RAM area LOW: Page 0 to 83 are available HIGH: Page 0 to 66 are available	1
$\overline{RES}$	I	When $\overline{RES}$ is caused to go LOW, initialization is executed.	3

Display timing pins

Name	I/O	Description	Number of pins
CL	I	External clock input. When internal clock is used, this terminal should be maintained LOW or HIGH.	1
CLS	I	Clock select pin CLS=LOW : External clock is used CLS=HIGH : Internal clock from Built-in oscillator is used	1

Test pins

Name	I/O	Description	Number of pins
TEST1	I	It is the test pin. This pin must be fixed at LOW.	1
TEST2	I	It is the test pin. This pin must be fixed at LOW.	1
TEST3 to TEST6	O	They are the test pins. Their pin must be OPEN.	6

LCD Driver pins

Name	I/O	Description	Number of pins
SEG1 to SEG312	O	Segment output pin Applicable pins are limited depending on setting of the DISCTL command. ・When the command is set to 1/67 duty, data displayed at the column addresses 0 to 97 are output to SEG10 to 303. Output to SEG1 to 9 and SEG304 to 312 become indefinite. ・When the command is set to 1/82 duty, data displayed at the column addresses 0 to 103 are output to SEG1 to 312.	312
COM1 to COM82	O	Common output pin Applicable pins are limited depending on setting of the DISCTL command. ・When the command is set to 1/67 duty, outputs to 67 pins of COM8 to 41 and COM50 to 82 become valid. Outputs to COM1 to 7 and COM42 to 49 become indefinite. ・When the command is set to 1/82 duty, all signals to COM1 and COM82 become valid.	82

8. FUNCTIONAL DESCRIPTION

8.1 Serial Data Input

Commands and data are input and output in series. However ,the contents of the display RAM cannot be read. For the serial interface, the following two modes are available. These modes can be selected when the pin S89 is set to HIGH or LOW.

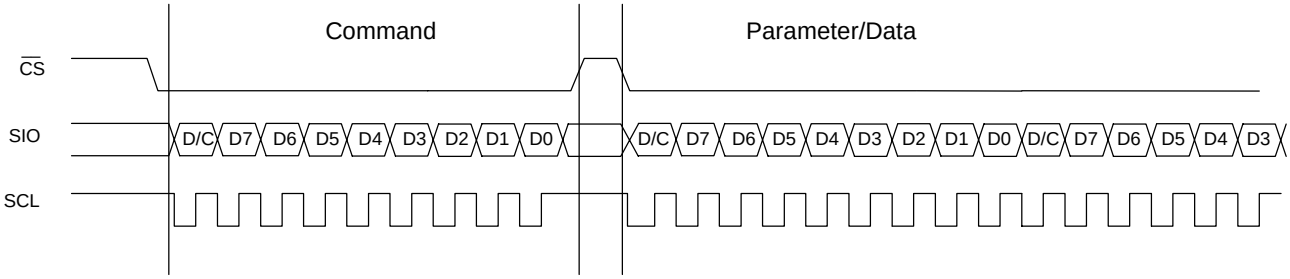
① 9-bit Interface
3 pins of $\overline{CS}$, SCL and SIO are used. The data format becomes D/$\overline{C}$ (data/command identification bit) + 8 bits, or 9-bit unit.

② 8-bit Interface
4 pins of $\overline{CS}$, SCL, SIO and A0 are used. The data format is a 8-bit one, and the data/command identification is made with levels of the A0 signal.

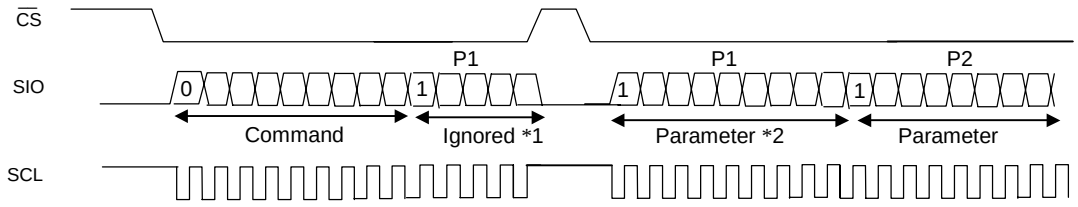
8.1.1 Serial Interface

Write Data Mode

① In case of 9-bit Interface
When SCL rises after $\overline{CS}$ changes to LOW, the data of SIO is taken in. Data are transmitted from the MPU to the SIO pin synchronously as SCL falls, and S1D15G14 takes in signals from the SIO pin as SCL rises. In addition to the D/C signal of data/command identification bit, 8-bit data is first transmitted as the most significant bit to the SIO pin. After the data transmission ends, set the $\overline{CS}$ pin to the HIGH level. The following shows the timing charts.

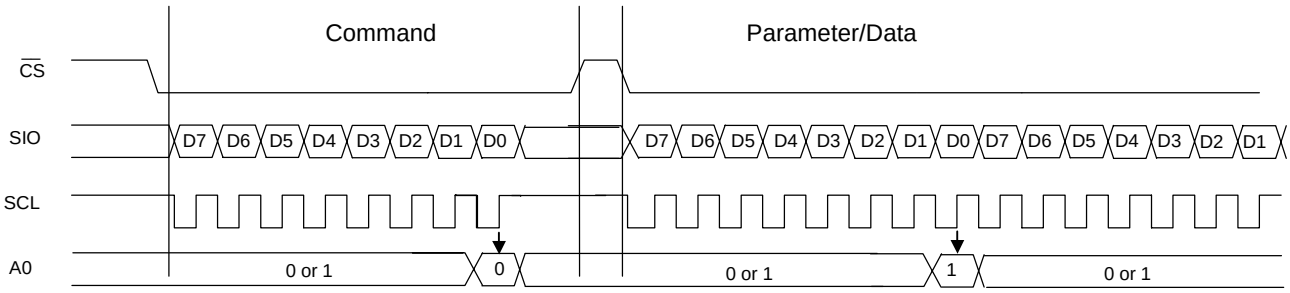


Also, other timing charts show suspension of transfer after change of the $\overline{CS}$ pin to HIGH during data transfer. When the command is sent, the $\overline{CS}$ pin changes to HIGH while the parameter P1 is transferred and the transfer is suspended, the parameter P1 suspended halfway is not taken in S1D15G14. Then, set the $\overline{CS}$ pin to LOW and resume the data transfer, and data to be received are recognized as those from P1.

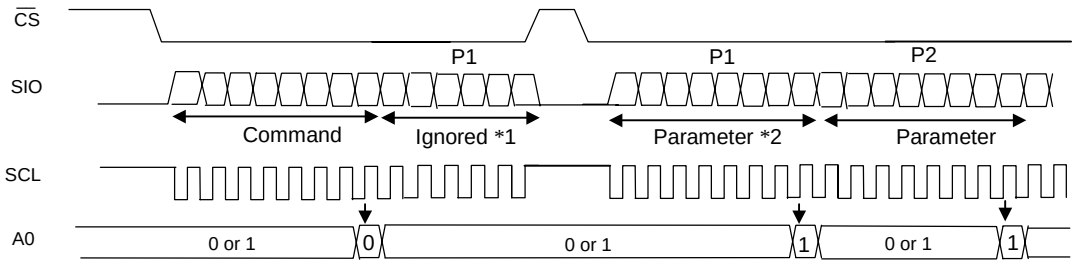


*1 Shows that $\overline{CS}$ has changed to HIGH level during data transfer.
*2 The suspended *1 is ignored, and Parameter *2 after resumption of transfer is recognized as Parameter 1.

② In case of 8-bit Interface,
When SCL rises after $\overline{CS}$ changes to LOW, the data of SIO is taken in. 8-bit data are transmitted from the MPU to the SIO pin first as the most significant bit synchronously as SCL falls, and S1D15G14 takes in signals from the SIO pin as SCL rises.
At the time, data/command identification is made at the A0 pin. After the data transmission, set the $\overline{CS}$ pin to the HIGH level.



Also, other timing charts show suspension of transfer after change of the $\overline{CS}$ pin to HIGH during data transfer. When the command is sent, the $\overline{CS}$ pin changes to HIGH while the parameter P1 is transferred and the transfer is suspended, the parameter P1 suspended halfway is not taken in S1D15G14. Then, set the $\overline{CS}$ pin to LOW and resume the data transfer, and data to be received are recognized as those from P1.



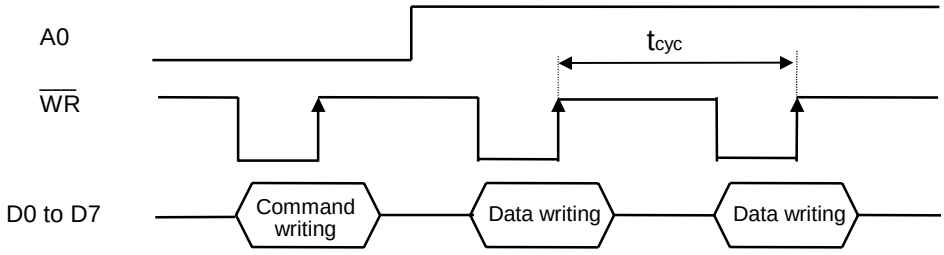
*1 Shows that $\overline{CS}$ has changed to HIGH level during data transfer.
*2 The suspended *1 is ignored, and Parameter *2 after resumption of transfer is recognized as Parameter 1.

8.2 Parallel Interface

When viewed from the MPU, S1D15G14 accesses the built-in display memory through the internal bus holder, and a high-speed data transfer, which requests no wait time, is possible. The write and read timing charts are as follows (and show examples of operation with the 80-series MPU interface).

8.2.1 In case of writing in S1D15G14 display memory from MPU

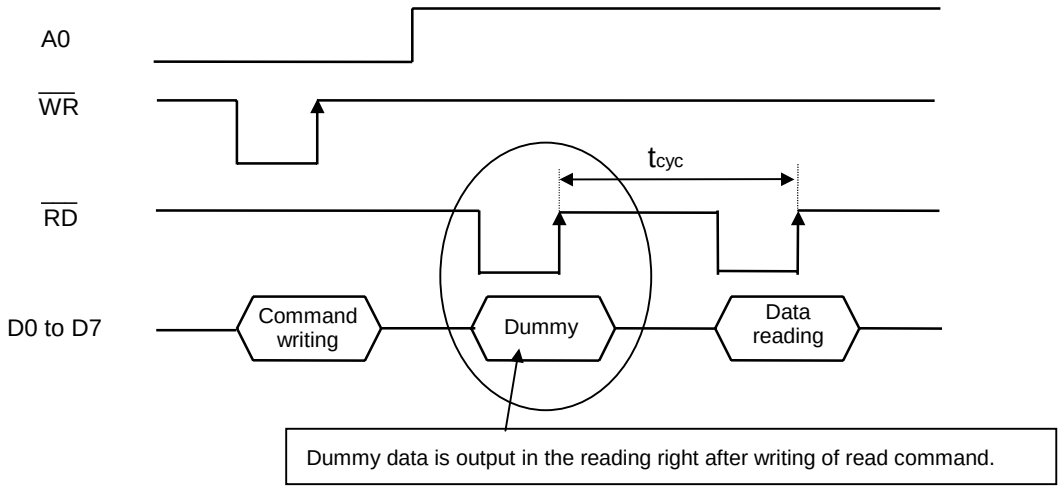
Display data are written following the memory write command.



8.2.2 In case of reading display memory data from S1D15G14

Data are read following the RAM data read command.

※ The DDRAM read sequence is limited, and data at a specified address is not output (dummy read) in data reading right after the RAM data read command and is output at the time of second data reading.

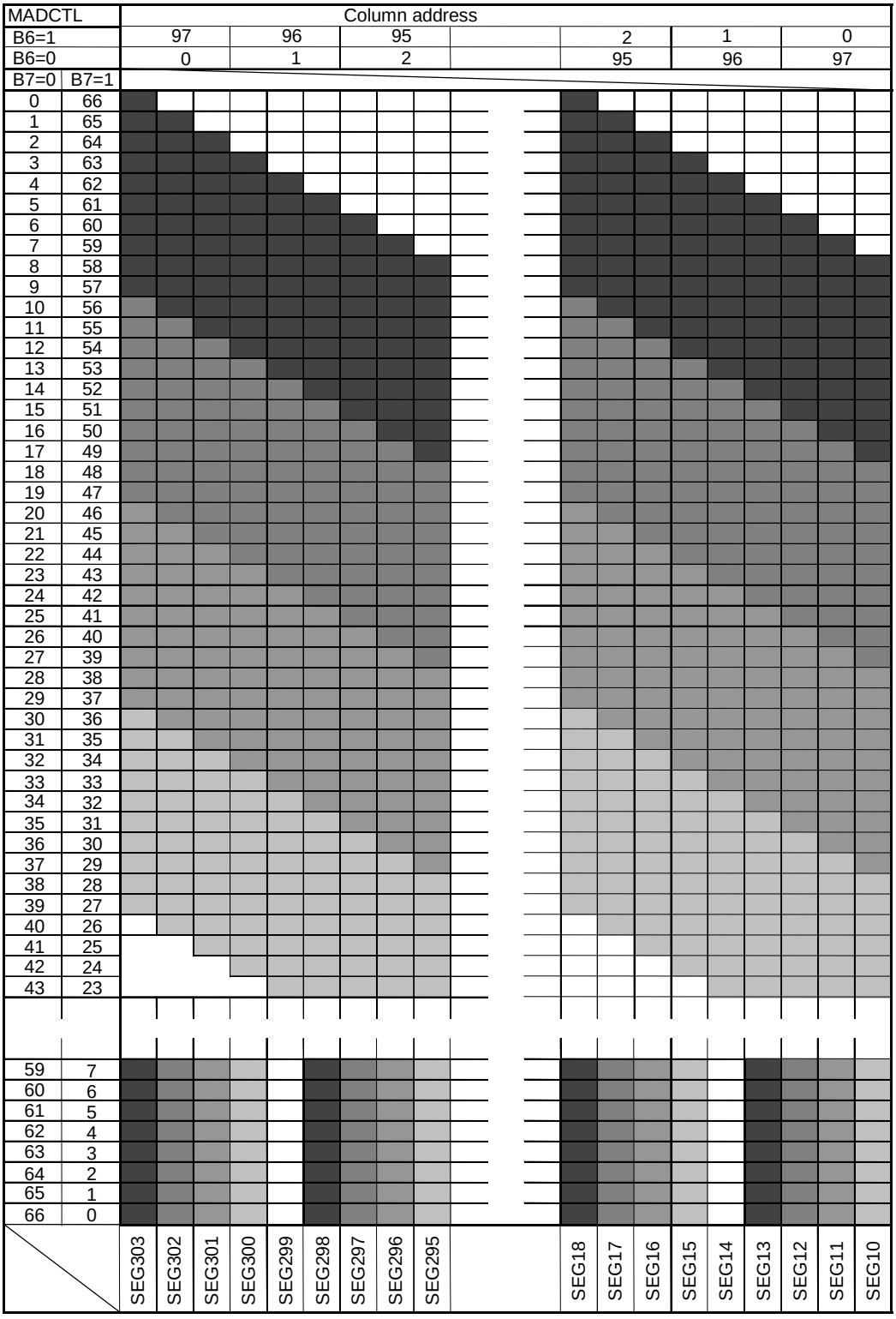


8.3 Memory map

Memory maps are shown below. They are two memory maps from the level of the RAMDIV pin. For the detail, see 7.4, MPU Interface.

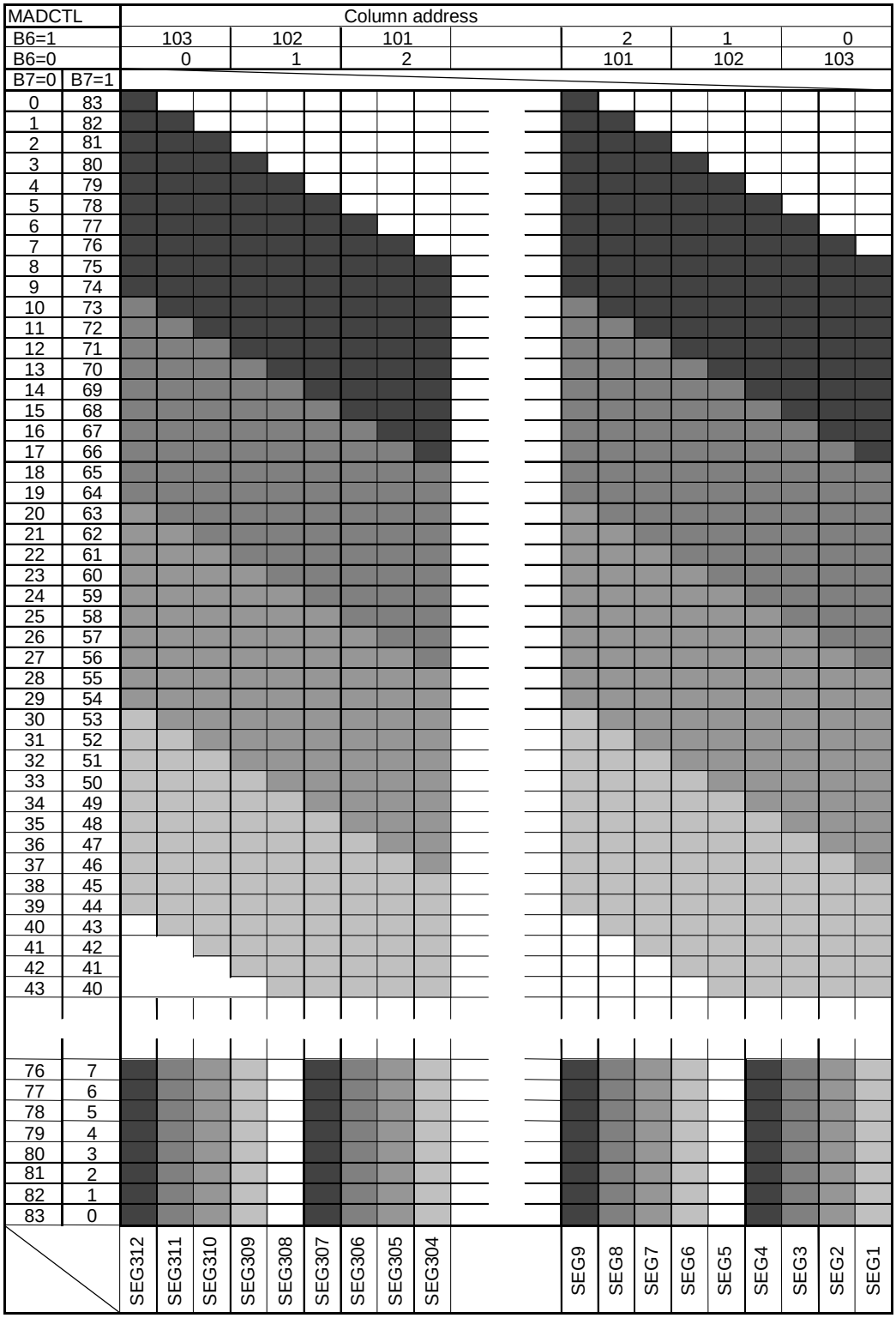
8.3.1 In Case of 1/67 duty

Condition : RAMDIV=HIGH, DISCTL command P31="0"
Refer to the below figure for setup of the MADCTL command.



8.3.2 In case of 1/82 duty

Condition : RAMDIV=LOW, DISCTL Command P31="1"
Refer to the below figure for setup of the MADCTL command.



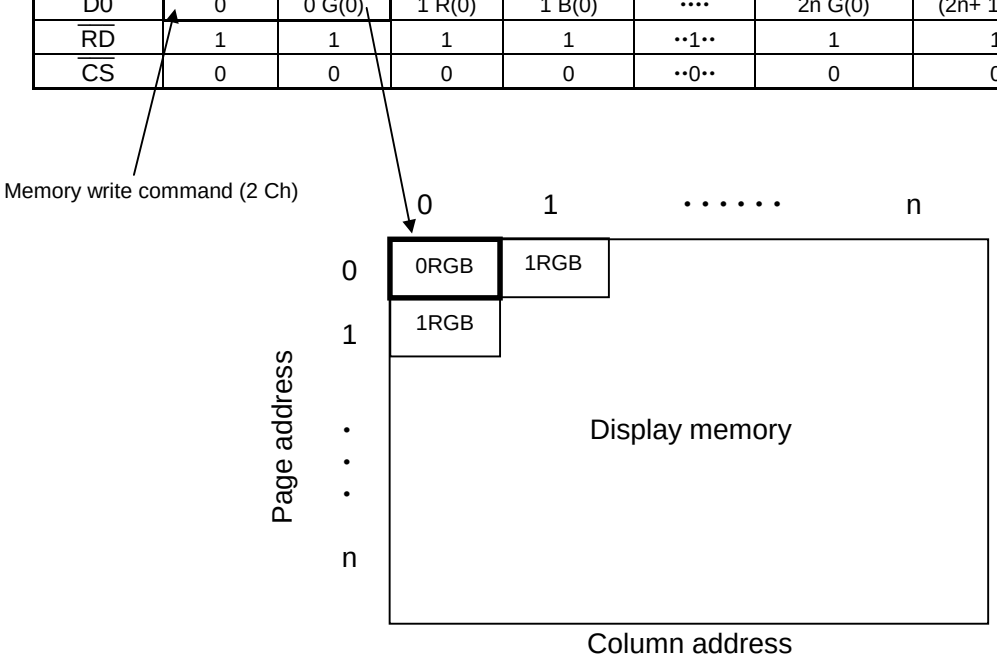
8.4 MPU Interface

This paragraph explains relations between data that the MPU read in the display memory of S1D15G14 and data to be practically stored in the display memory.

8.4.1 444 Mode (Display in 4096 colors)

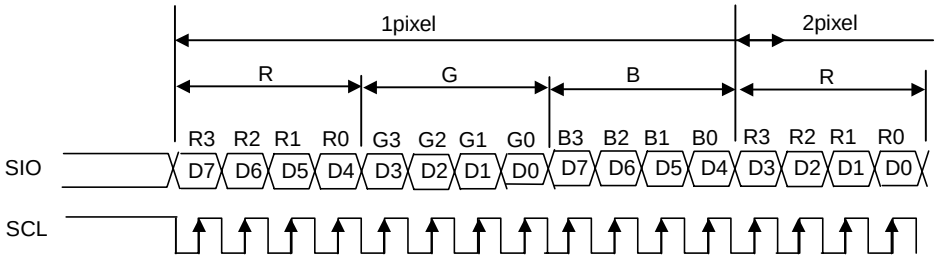
In this mode, data for 2RGB are written in the display memory when the MPU writes three times. Actually, the first two write signals write data for the first RGB in the display memory and the third write signal writes data for the 2nd RGB. When write signal is input only once, nothing is written in the display memory.

$\overline{WR}$	0	1	2	3	••••	3/2(n+1)	3/2(n+2)	3/2(n+3)
A0(D/C)	0	1	1	1	••••	1	1	1
D7	0	0 R(3)	0 B(3)	1 G(3)	••••	2n R(3)	2n B(3)	(2n+ 1) G(3)
D6	0	0 R(2)	0 B(2)	1 G(2)	••••	2n R(2)	2n B(2)	(2n+ 1) G(2)
D5	1	0 R(1)	0 B(1)	1 G(1)	••••	2n R(1)	2n B(1)	(2n+ 1) G(1)
D4	0	0 R(0)	0 B(0)	1 G(0)	••••	2n R(0)	2n B(0)	(2n+ 1) G(0)
D3	1	0 G(3)	1 R(3)	1 B(3)	••••	2n G(3)	(2n+ 1) R(3)	(2n+ 1) B(3)
D2	1	0 G(2)	1 R(2)	1 B(2)	••••	2n G(2)	(2n+ 1) R(2)	(2n+ 1) B(2)
D1	0	0 G(1)	1 R(1)	1 B(1)	••••	2n G(1)	(2n+ 1) R(1)	(2n+ 1) B(1)
D0	0	0 G(0)	1 R(0)	1 B(0)	••••	2n G(0)	(2n+ 1) R(0)	(2n+ 1) B(0)
$\overline{RD}$	1	1	1	1	••1••	1	1	1
$\overline{CS}$	0	0	0	0	••0••	0	0	0



The MADCTL command decides the sequence of storing data in the display memory.

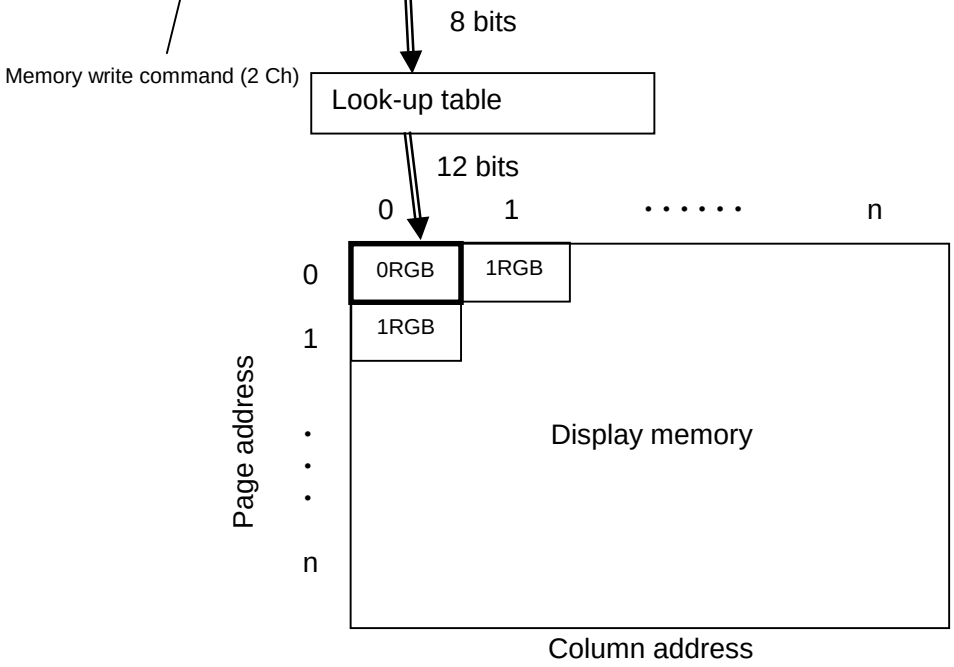
The equivalence of MPU data with serial interface is shown as follows:



8.4.2 332 Mode (Display in 256 colors)

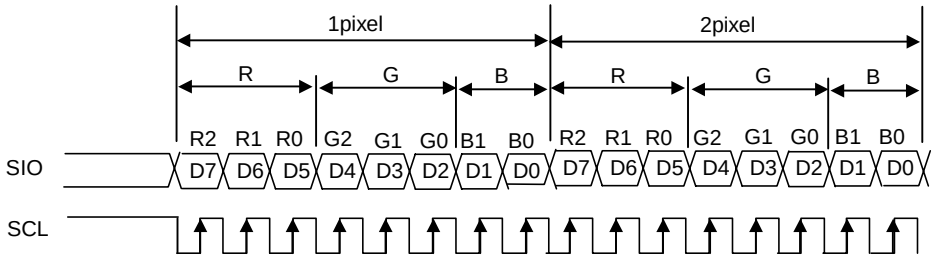
In this mode, data for 1RGB are written when the MPU writes once. Display data written in 8 bits are converted into 12-bit data on the look-up table to be set by the RGBSET command and are stored in the display memory.

$\overline{WR}$	0	1	2	••••	n+1
A0(D/C)	0	1	1	••••	1
D7	0	0 R(2)	1 R(2)	••••	n R(2)
D6	0	0 R(1)	1 R(1)	••••	n R(1)
D5	1	0 R(0)	1 R(0)	••••	n R(0)
D4	0	0 G(2)	1 G(2)	••••	n R(2)
D3	1	0 G(1)	1 G(1)	••••	n G(1)
D2	1	0 G(0)	1 G(0)	••••	n G(0)
D1	0	0 B(1)	1 B(1)	••••	n B(1)
D0	0	0 B(0)	1 B(0)	••••	n B(0)
$\overline{RD}$	1	1	1	••1••	1
$\overline{CS}$	0	0	0	••0••	0



The MADCTL command decides the sequence of storing data in the display memory.

The equivalence of MPU data with serial interface is shown as follows:

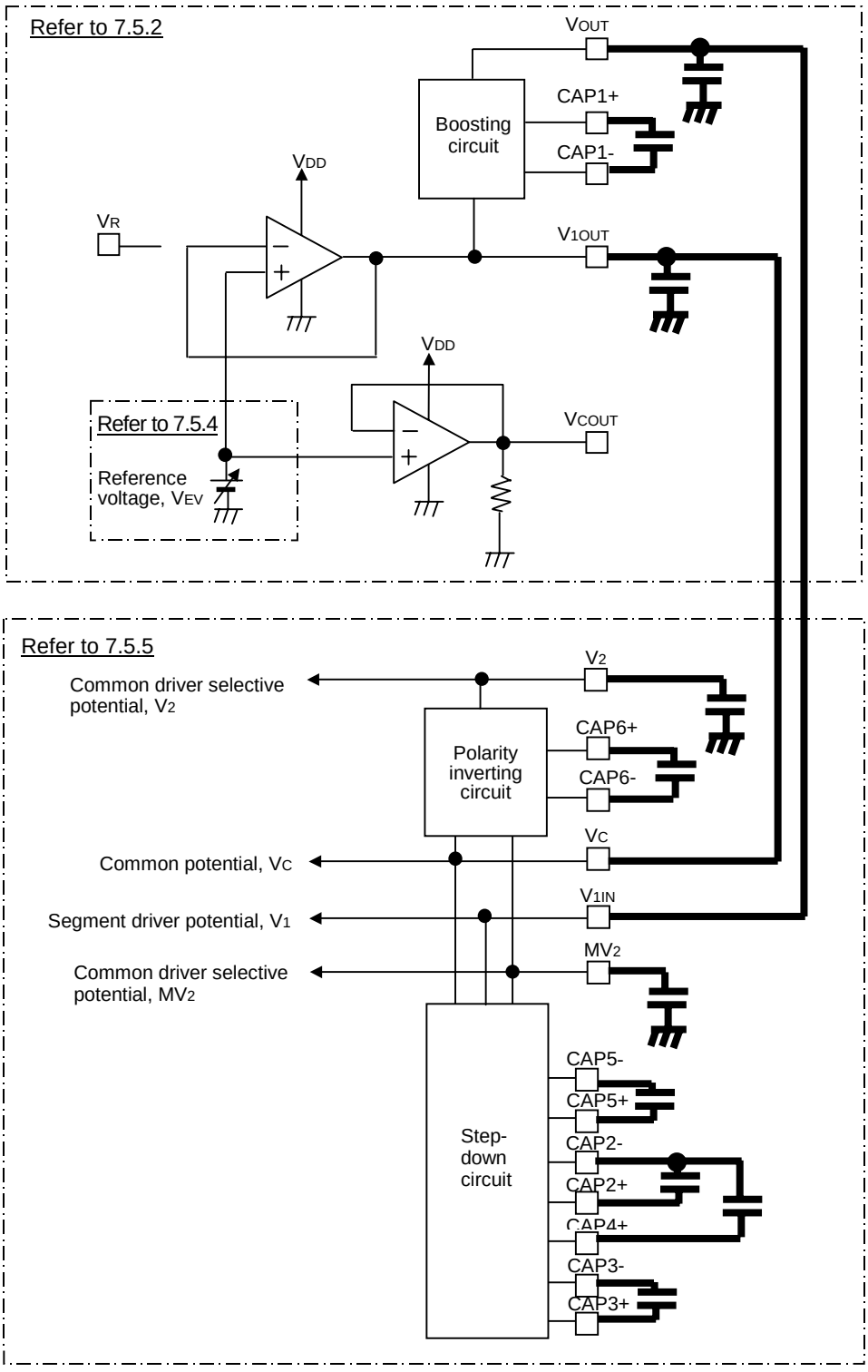


8.5 LCD Drive Power Supply Circuit

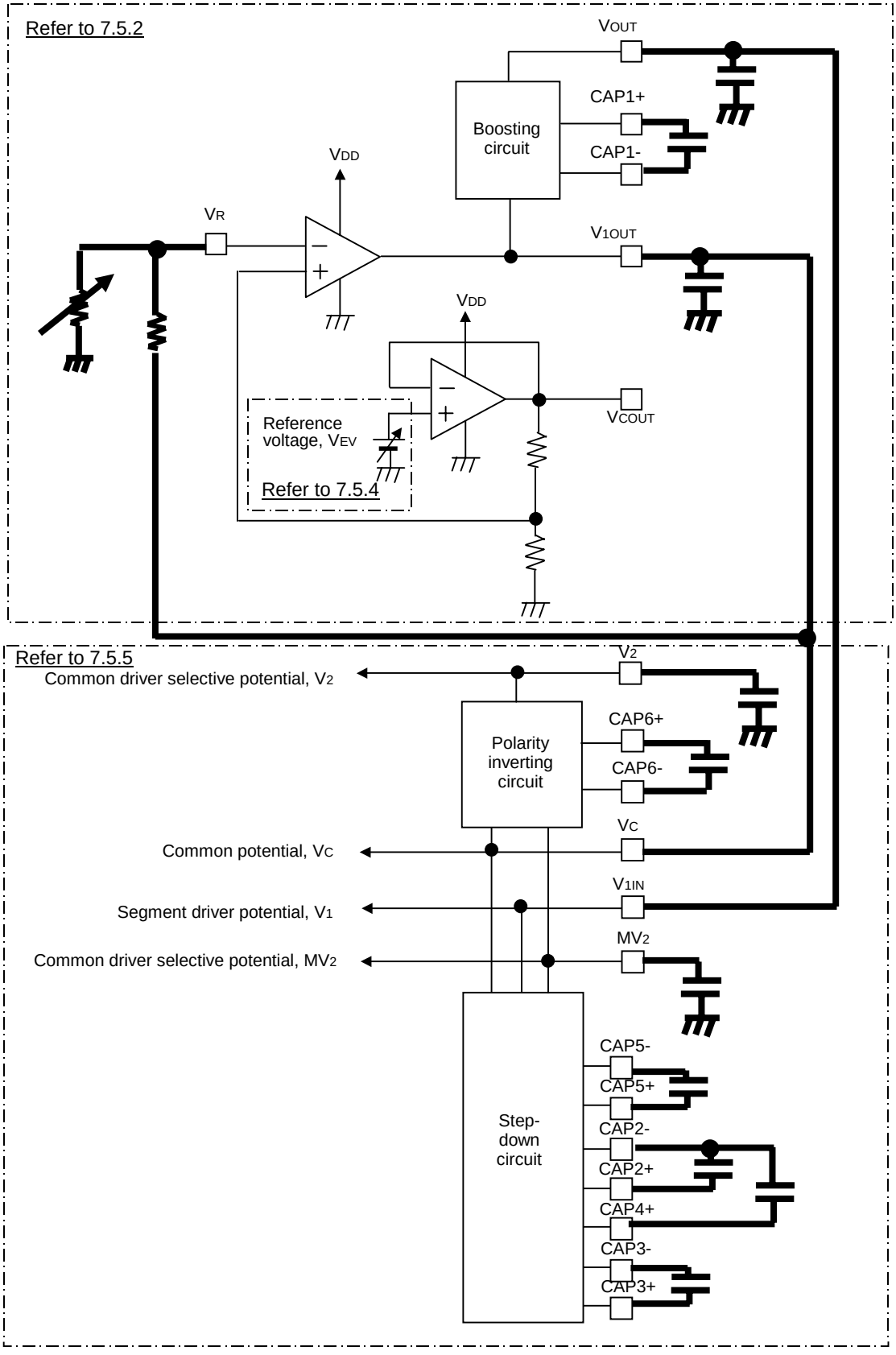
The S1D15G14 has a built-in power supply circuit that generates voltage necessary for driving the LCD.

8.5.1 Power Supply Block

The pin connections for the S1D15G14 built-in power supply blocks are shown below.
① When internal resistance is used (to adjust the LCD voltage with electronic volume)
Note that the external parts and wirings are indicated in boldface.

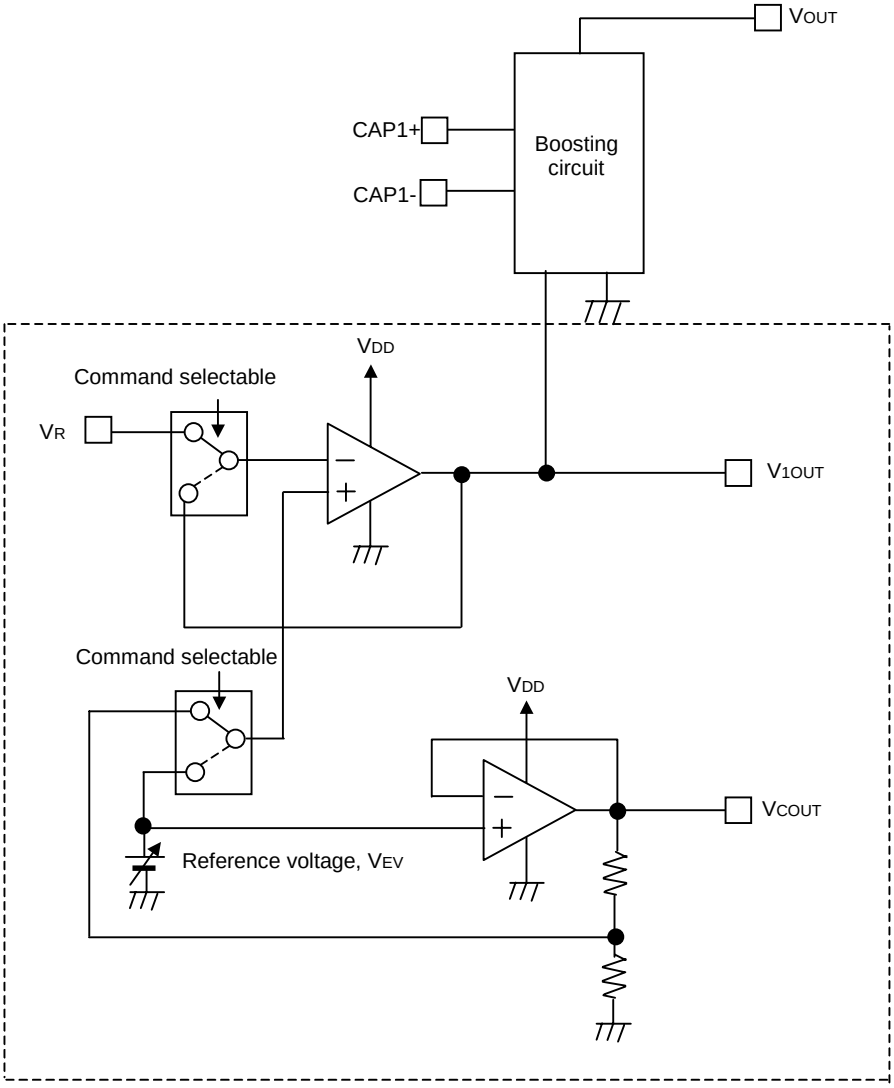


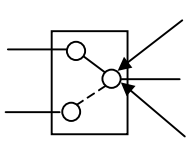
② When external resistance is used (to adjust the LCD voltage with the external variable resister)
Note that the external parts and wirings are indicated in boldface.



8.5.2 Power Supply Block (Reference voltage circuit/voltage follower)

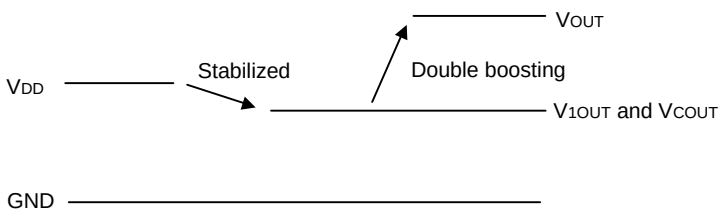
The reference voltage circuit and the voltage follower generate on/off polarity for the segment driver and central polarity for the segment common driver.



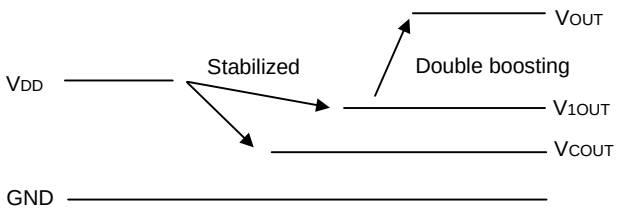


V_{1OUT}, V_{COUT} and V_{OUT} are generated by the V_{DD} polarity. The potential relations of the internal and external resistances are as follows.

Internal resistance



External resistance

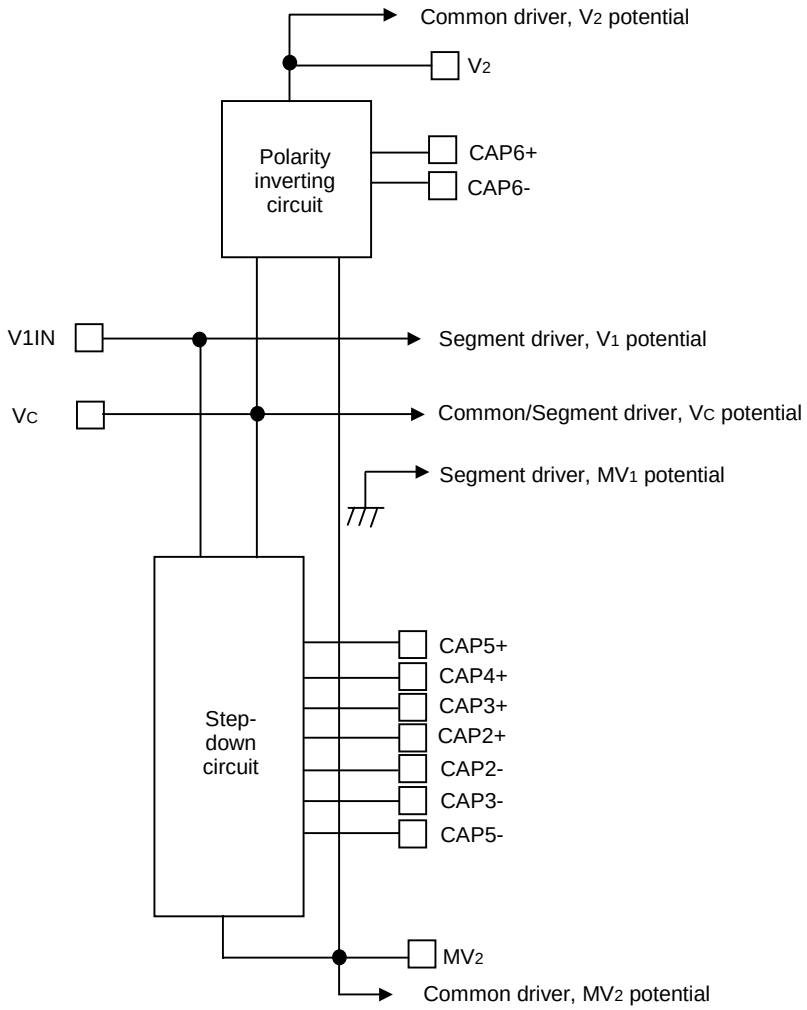


The following table describes the relationship between the external wire connection and LCD driving voltage.

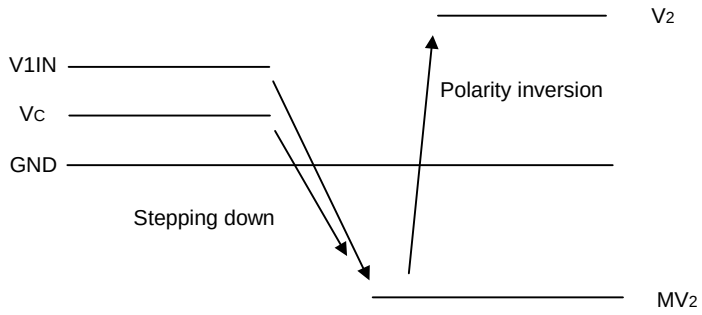
Pin name	Internal resistance		External resistance	
	Wire connection	**LCD driving voltage**	**Wire connection**	**LCD driving voltage**
V_{OUT}	Connected to V_{1IN}	Segment V_1	Connected to V_{1IN}	Segment V_1
V_{1OUT}	Connected to V_C	V_C	Connected to V_C	V_C
V_{COUT}	Open	—	Open	—

8.5.3 Power Supply Block 2 (Step-down circuit and polarity inverting circuit)

The step-down circuit and the polarity inverting circuit generate selective potential of the common driver.



V_2/MV_2 is generated from the pin input voltage, V_{1IN}/V_C. The potential relations are as follows:



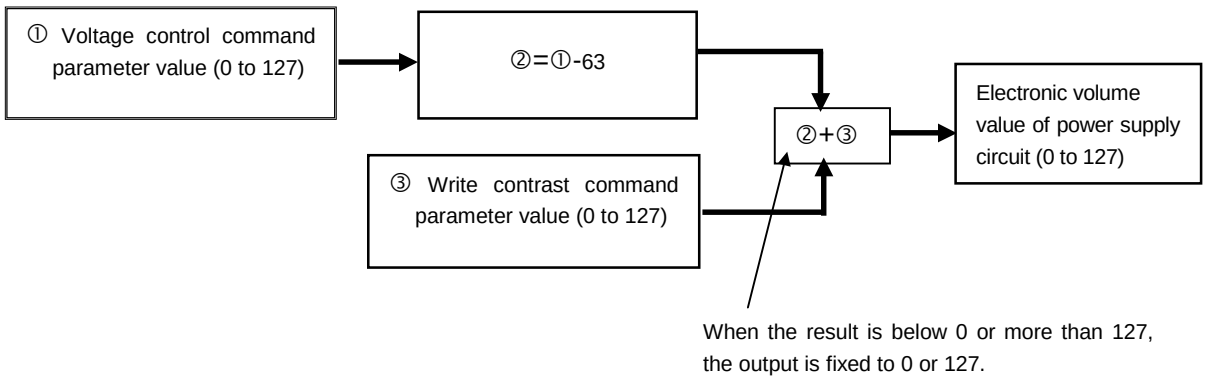
Also, to change the LCD drive bias, change the step count (= connection of external capacitor) of the MV_2 step-down circuit.

8.5.4 Reference Voltage Circuit

S1D15G14 generates the LCD drive reference voltage, V_{EV}, from V_{DD}, converts it into impedance with the OP amplifier and outputs it to V_{1OUT}.

① Electronic Volume Function

The V_{EV} voltage is variable by a command (Write contrast or Voltage control) and can be adjusted to the optimum value in the software. Setting of the two commands is reflected to operation of the power supply circuit as shown below:



These two commands are used for the following purposes.
① Voltage control command: used to compensate variations of the LCD panel and the IC.
② Write contrast command: used to adjust the display contrast.

V_{EV} can be expressed by the following formula:

$$V_{1OUT} = V_{EV} = \left(\frac{89+\alpha}{218}\right) \times V_{REG}$$

α = (Voltage Control parameter value) - 63 + (Write Contrast parameter value)
The relations of $0 \le \alpha \le 127$ always exist. Even when the calculation result of the above formula is below 0 or more than 127, the value a is fixed to 0 or 127.

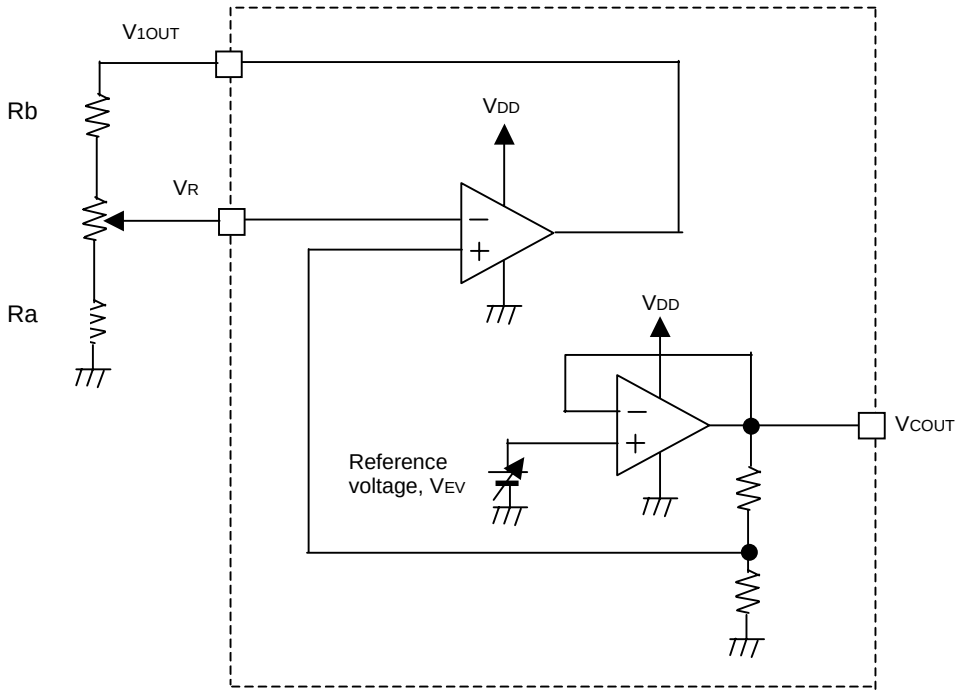
Where, V_{REG} is the reference voltage inside the IC and is 1.8V (Typ.) when T_a = 25°C. Also, the value a ranges from 0 to 127 and V_{REG} is 1.8V (Typ.), and therefore, V_{EV} is variable between 0.73V and 1.80V.

Please be careful for the set-up value not to exceed operation voltage.

② External Resister

When the external trimming resister is used to adjust the LCD drive voltage finely, connect the external resisters as follows. Also, in this case, set Parameter P14 to "1" by the Power Control command and select the external resisters.

Internal circuit when external resistance is used



In this case, the output voltage V_{1OUT} is calculated by the following formula. (In the calculation, the resistance value of the variable resister was set to 0.)

$$V_{1OUT} = \frac{Ra + Rb}{Ra} \times \frac{V_{EV}}{2}$$

③ Temperature Gradient

Also, the command (Temperature gradient set) can be used to change the temperature gradient of V_{REG}. The display quality can be corrected and retained in wide temperature ranges by selecting temperature gradients suitable to temperature characteristics of the LCD panel.

Temperature gradients can be selected from the following four kinds: Respective temperature gradient values are for refer only.

The intersection of the temperature gradient is 25 °C.

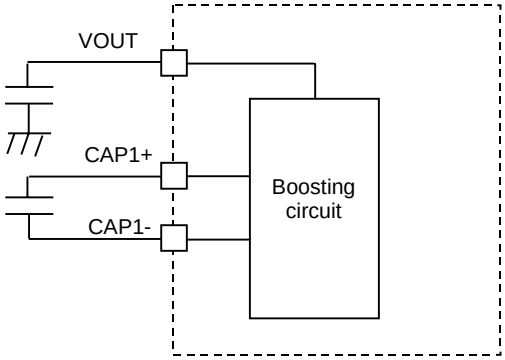
Parameter		Average temperature gradient (%/°C)
0	0	-0.05
0	1	-0.1
1	0	-0.15
1	1	-0.2

8.5.5 Boosting Circuit, Step-down Circuit and Polarity Inverting Circuit

The boosting circuit, the step-down circuit and the polarity inverting circuit, for which the capacitor charge pump circuit is used, generates voltages of the LCD drive.

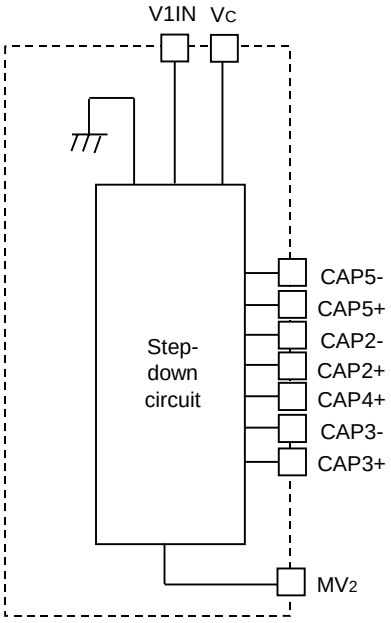
① Boosting Circuit

This circuit doubles the voltage between V_{1OUT} and GND, outputs it to V_{OUT} and generates ON/OFF potentials of the segment driver. Connect a capacitor each between CAP1+ and CAP1- and between V_{OUT} and GND.



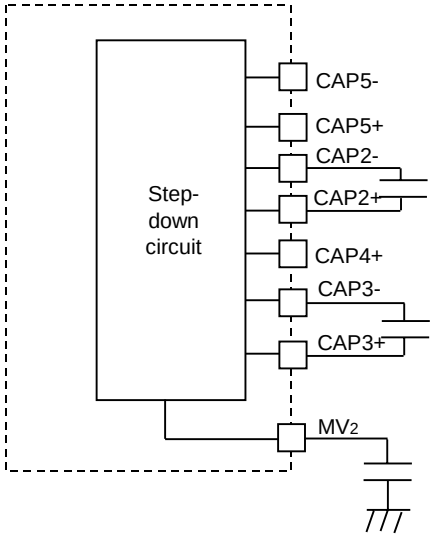
② Step-down Circuit

This circuit reduces the voltages between V_{1IN}/V_C and GND to 1/4.5 at most, outputs it to MV_2 and generates selective potentials of the common driver. To change the reduction rate, connect an external capacitor and set the bias rate with the parameters P35 to P33 of the Display Control command.

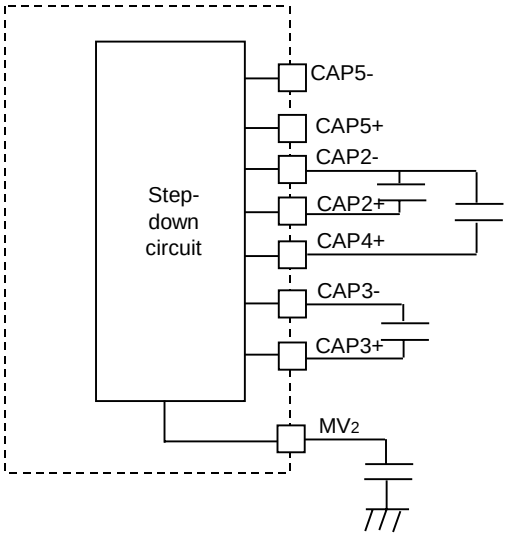


The following shows how to connect external parts.

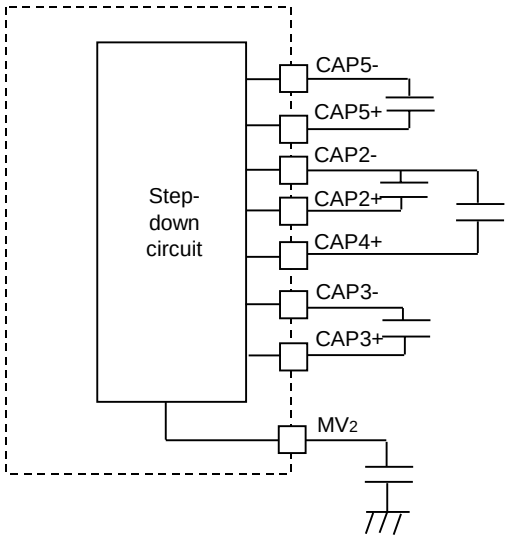
In case of 1/5 bias or 1/6 bias
P35,P34,P31 = 1,0,0 or 0,1,1



In case of 1/7 bias or 1/8 bias
P35,P34,P31 = 0,1,0 or 0,0,1



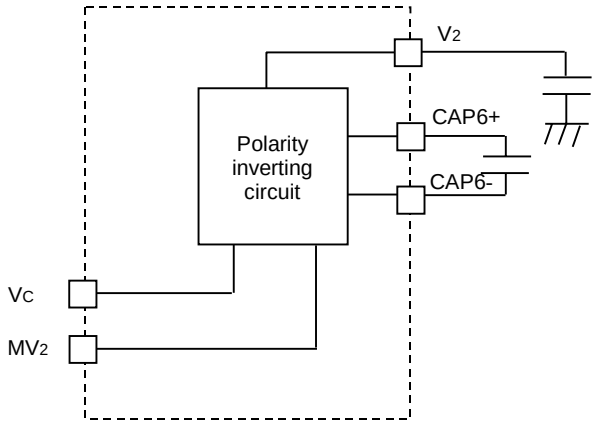
In case of 1/9 bias
P35,P34,P31 = 0,0,0



Note)
If software bias setting and above external circuit are unmatched, this IC doesn't work correctly.
(example)In case of combination using 1/9bias external circuit and 1/6 bias register setting.
→ this IC doesn't work correctly.

③ Polarity Inverting Circuit

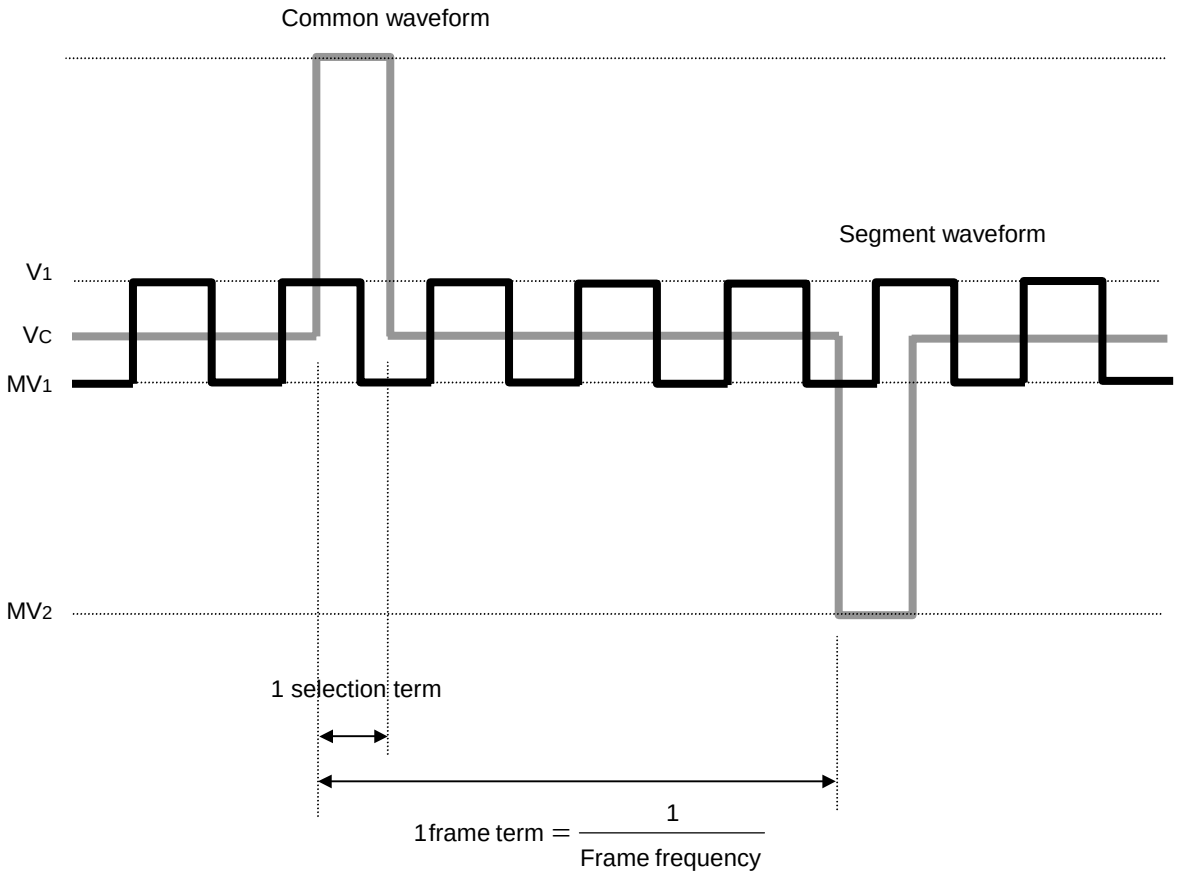
This circuit inverts the polarity of the voltage between V_C and MV_2, outputs it to V_2 and generates selective potentials of the common driver. Connect a capacitor each between CAP6+ and CAP6- and between V_2 and GND.



8.6 LCD Drive Circuit

8.6.1 Driving Method

S1D15G14 drives the LCD panel by the principle driving method.
The following shows the command and the segment drive waveforms.



There are two methods for setting 1 selection term to be used for the normal and idle modes of display status, respectively.

(1) Normal mode
Set with Parameter 1 of the Display Control command.

$$1\text{Selection term} = \frac{1}{f_{OSC1}} \times (\text{Clock count of Parameter 1})$$

(2) Idle mode
Dividing ratio is set with the Parameter 3 (P37) of the display control command (DISCTL).

$$1\text{Selection term} = \frac{1}{f_{OSC2}} \div (\text{Dividing ratio})$$

One frame term depends on setting of the above Parameter 1 of the Display Control command and setting of duties of Parameters 3 to 5.

$$1 \text{ frame term} = (1 \text{ selection term}) \times (\text{Display duty})$$

8.6.2 LCD Drive Bias

The LCD drive bias rate in a principle drive is calculated from the following formula:

$$\text{Bias rate} = \sqrt{\text{Drive duty}} + 1$$

When the LCD is driven according to this formula, the rate of ON voltage to OFF voltage becomes the maximum.

Since S1D15G14 allows to select the LCD drive bias out of 1/5 to 1/9 bias, select the optimum drive bias taking characteristics of applicable LCD and the number of external parts into account. The smaller the bias rate is set, the more the number of external parts reduces and the smaller the rate of ON voltage to OFF voltage of LCD drive becomes.

The following shows the formula to calculate common and segment amplitudes from Duty, Bias and LCD threshold (Vth):

① Segment Amplitude (V_{SEG})

$$\frac{V_{SEG}}{2} = \frac{Vth}{\sqrt{1 + \frac{Bias^2 - 4 \times Bias + 3}{Duty}}}$$

Note : Set V_{SEG} to 3.6V or less.

② Common Amplitude (V_{COM})

$$\frac{V_{COM}}{2} = (BIAS - 1) \times \frac{V_{SEG}}{2}$$

8.7 Display Mode

For S1D15G14, two display modes, i.e., Normal Mode and Idle Mode, are available depending on setting of commands. Respective operations are shown in the table below:

Item	Normal Mode	Idle Mode
LCD system operation	Oscillator 1	Oscillator 2
Oscillator 1 (Typ. 840kHz)	Operation	Stop
Oscillator 2 (Typ. 13kHz)	Stop	Operation
Number of displayable colors	4,096 colors	8 colors

Each mode can be set or cancelled by the Normal Display ON, Idle Mode ON/OFF commands.

Normal Mode :

Circuits of the LCD system operate regarding output of Oscillator 1 as the reference clock and can be displayed in 4,096 colors.

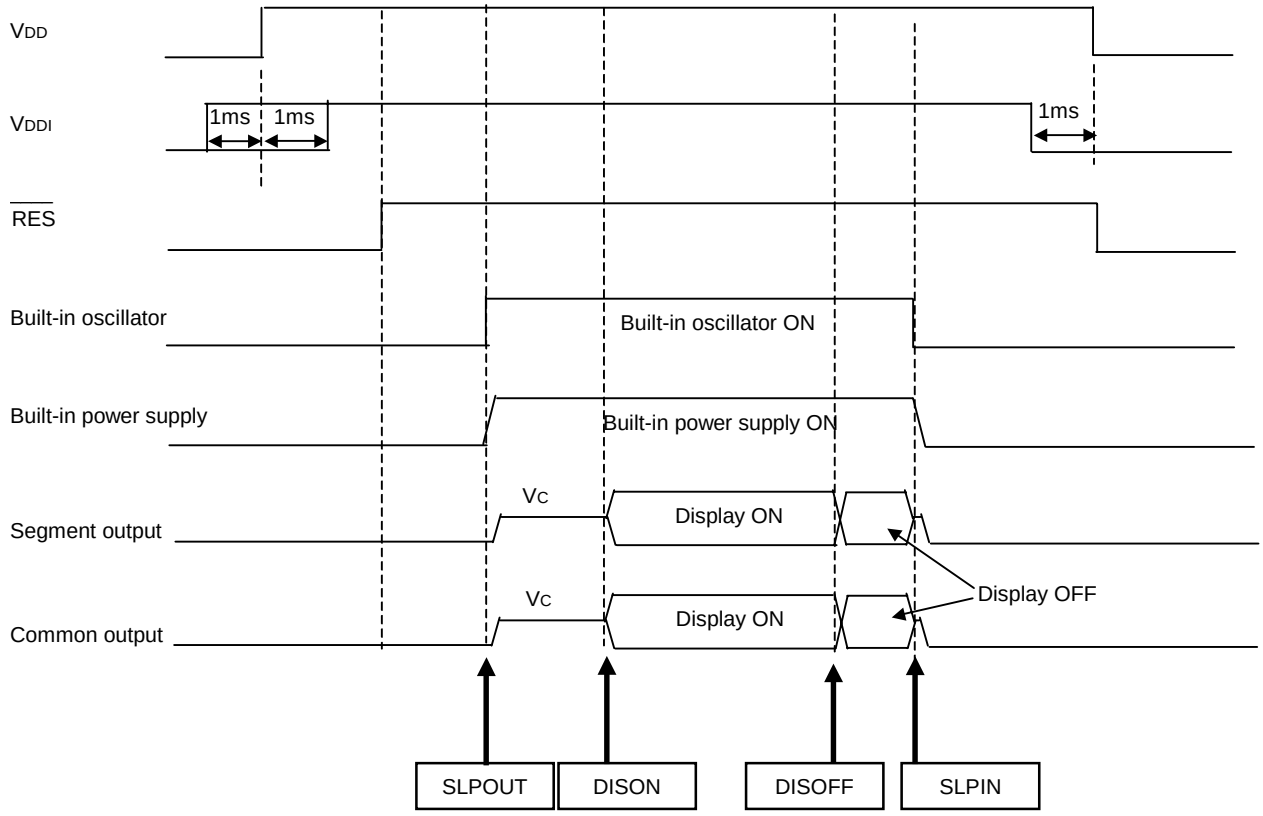
Idle Mode :

Circuits of the LCD system operate regarding output of Oscillator 1 as the reference clock, and their display colors are reduced to 8 colors. The most significant bit of each color of RGB is used for display out of data in the display RAM. In this mode, the display color is limited to 8 colors, but these circuits can operate with low power consumption because the operation frequency is reduced.

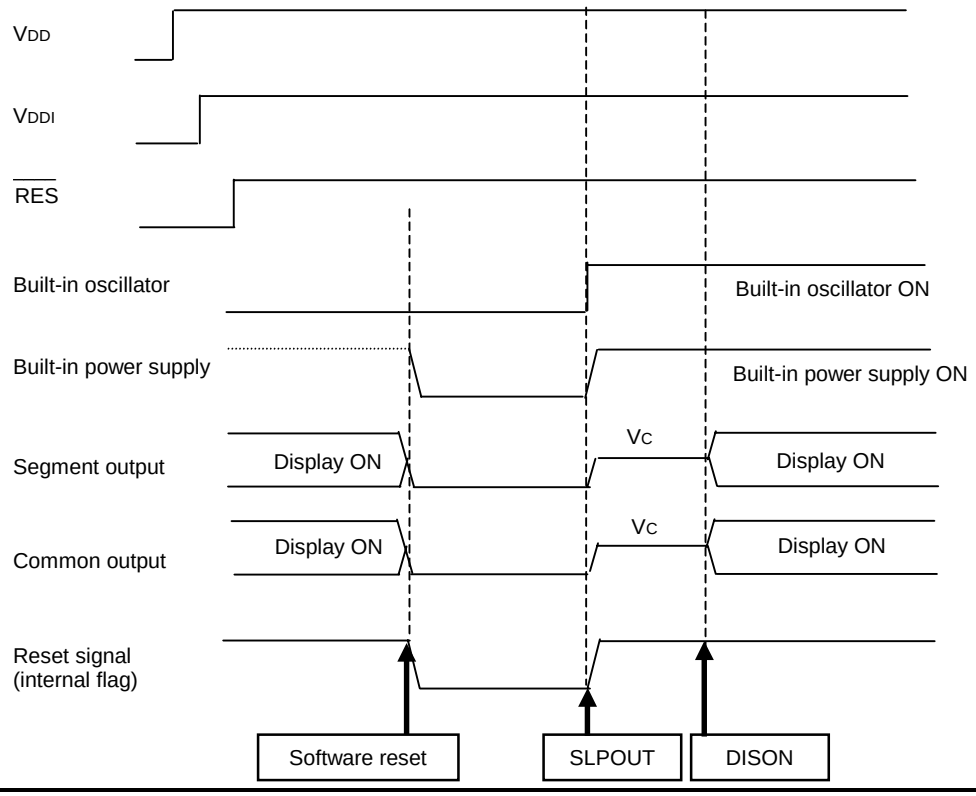
8.8 ON/OFF, reset sequence

The following figures show the reset sequence and the status when the power is ON/OFF, and when software reset is done.

Hardware reset



Software reset



9. COMMANDS

9.1 Command table

No	HEX	Command name	Number of parameters	Status after reset *1	Status reading *2 ○: Available ×: Not available
1	00	NOP	—	—	×
2	01	Software reset	—	—	×
3	02	Booster voltage OFF	—	Built-in power supply OFF	○
4	03	Booster voltage ON	—		○
5	04	TEST mode	—	—	×
6	09	Read display status	—	Default value	×
7	10	Sleep in	—	Sleep in	○
8	11	Sleep out	—		○
9	12	Partial display mode ON	—	OFF	○
10	13	Display normal mode ON	—	ON (Normal display)	○
11	20	Inversion OFF	—	OFF (Normal display)	○
12	21	Inversion ON	—		○
13	22	All pixel OFF	—	OFF (Normal display)	○
14	23	All pixel ON	—		○
15	25	Write contrast	1	Default value	×
16	28	Display OFF	—	Display OFF	○
17	29	Display ON	—		○
18	2A	Column address set	2	Default value	×
19	2B	Page address set	2	Default value	×
20	2C	Memory write	Write data	—	×
21	2D	Colour set	20	Indeterminate	×
22	2E	RAM data read	—	—	×
23	30	Partial area	2	Default value	×
24	33	Vertical scrolling definition	3	Default value	×
25	34	TEST mode	—	—	×
26	35	TEST mode	—	—	×
27	36	Memory access control	1	Default value	○
28	37	Vertical scrolling start address	1	Default value	○
29	38	Idle mode OFF	—	Idle mode OFF	○
30	39	Idle mode ON	—		○
31	3A	Interface pixel format	1	Default value	○
32	DE	TEST mode	—	—	×
33	AA	NOP2	—	—	×
34	C6	Initial escape	—	—	×
35	DA	TEST mode	—	—	×
36	DB	TEST mode	—	—	×
37	DC	TEST mode	—	—	×
38	B2	TEST mode	1	—	×
39	B3	Gray scale position set 0	15	Indeterminate	×
40	B4	Gray scale position set 1	15	Indeterminate	×
41	B5	Gamma curve set	1	Default value	○
42	B6	Display control	7	Indeterminate	○
43	B7	Temperature gradient set	14	Indeterminate	×
44	B8	TEST mode	—	—	×
45	B9	Refresh set	1	Indeterminate	×
46	BA	Voltage control	2	Indeterminate	×
47	BD	Common driver output select	1	Indeterminate	×
48	BE	Power control	1	Indeterminate	×

*1: Indicates the status of each command after reset.
Default value: The default value for each command in the after-reset status is set.
See the detailed description of commands, for the status.
Indeterminate: The status is indeterminate that must be cancelled by initialization.

*2: Indicates the commands that the Read display status command (09h) can read the status.
○: The command execution status and all or a part of parameters that are set can be read.
×: The status cannot be read.

9.2 Command process time and notes

No.	HEX	Command name	Command execution timing *1		Time required for command process *2		Restrictions
			Immediately	V-Sync	MPU cycle	Frame number	
1	00	NOP	○	—	1	—	
2	01	Software reset	○	—	1	—	Apply a waiting time of 5ms after execution.
3	02	Booster voltage OFF	○	—	1	—	
4	03	Booster voltage ON	○	—	1	—	Apply a waiting time of more than 30ms until execution of the DISON command.
5	04	TEST mode	—	—	—	—	
6	09	Read display status	○	—	1	—	
7	10	Sleep in	○ Display OFF	○ Display ON	1 Display OFF	Maximum of 1 Display ON	
8	11	Sleep out	○ Display OFF	○ Display ON	1 Display OFF	Maximum of 1 Display ON	
9	12	Partial display mode ON	—	○	—	Maximum of 1	
10	13	Display normal mode ON	—	○	—	Maximum of 1	
11	20	Inversion OFF	—	○	—	Maximum of 1	
12	21	Inversion ON	—	○	—	Maximum of 1	
13	22	All pixel OFF	—	○	—	Maximum of 1	
14	23	All pixel ON	—	○	—	Maximum of 1	
15	25	Write contrast	○	—	1	—	
16	28	Display OFF	—	○	—	Maximum of 1	
17	29	Display ON	—	○	—	Maximum of 1	
18	2A	Column address set	○	—	1	—	
19	2B	Page address set	○	—	1	—	
20	2C	Memory write	○	—	1	—	
21	2D	Colour set	○	—	1	—	
22	2E	RAM data read	○	—	1	—	
23	30	Partial area	○	—	1	—	
24	33	Vertical scrolling definition	○	—	1	—	
25	34	TEST mode	—	—	—	—	
26	35	TEST mode	—	—	—	—	
27	36	Memory access control	○	—	1	—	
28	37	Vertical scrolling start address	○	—	1	—	
29	38	Idle mode OFF	—	○	—	*3	Waiting time *3 is required for sequential execution.
30	39	Idle mode ON	—	○	—		
31	3A	Interface pixel format	○	—	1	—	
32	DE	TEST mode	—	—	—	—	
33	AA	NOP2	○	—	1	—	
34	C6	Initial escape	○	—	1	—	
35	DA	TEST mode	—	—	—	—	
36	DB	TEST mode	—	—	—	—	
37	DC	TEST mode	—	—	—	—	
38	B2	TEST mode	—	—	—	—	
39	B3	Gray scale position set 0	○	—	1	—	
40	B4	Gray scale position set 1	○	—	1	—	
41	B5	Gamma curve set	○	—	1	—	
42	B6	Display control	○	—	1	—	
43	B7	Temperature gradient set	○	—	1	—	
44	B8	TEST mode	—	—	—	—	
45	B9	Refresh set	○	—	1	—	
46	BA	Voltage control	○	—	1	—	
47	BD	Common driver output select	○	—	1	—	
48	BE	Power control	○	—	1	—	

*1: Displays when the input command or parameter is executed.
Immediately: Executes upon writing of command and parameter.
In case of 80-series parallel interface: Rising time of signal $\overline{WR}$
In case of serial interface: Rising time of SCL signal that received the least significant bit (D0).
V-Sync: Executes in sync with the frame next to the frame into which the command or the parameter is written.

*2: Displays the time the input command requires for processing.
MPU cycle: Executes upon writing and processed within the MPU cycle time.
Frame number: Executes in sync with the displayed frame and processed within the time required for the number of frames.
The frame time is displayed in the display mode (normal/idle mode) upon input of the command.

*3: Displays each process time for idle mode ON/OFF.
Idle mode ON:
① (1 frame in idle mode) + (1 frame in normal mode)
② 1/ (f_{osc2}/ (division rate*3))* (number of GCP in normal mode during 1H-period)

Apply time required for processing ① + ②.

Idle mode OFF:
Apply time required for processing (1 frame in idle mode) + (1 frame in normal mode).

※ Apply the above processing time when turning the idle mode ON/OFF.

9.3 Details of Commands

(1) No Operation (NOP)
This is Non-Operation Command ①.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	0	0	00

This command enables to end the read/write sequence of the display memory. This command can escape from test mode, so that it is recommended to input this command periodically.

(2) Software Reset (SWRESET)
This is Software Reset Command. Use this command to reset the inside.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	0	1	01

This command works in the same way as the function of Hardware Reset by setting LOW to the $\overline{RES}$ pins.

(3) Booster Voltage OFF (BSTOFF)
This is Built-in Power Off Command.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	1	0	02

When this command is executed, the LCD drive power supply circuit is turned OFF.
Sleep in/out Command can also turn OFF/ON the LCD drive power supply circuit, but this command turns OFF the LCD drive power supply circuit independently.

The following command enables to get out of the status set by this command.

Exit commands	HEX
Booster voltage ON	03

***** After reset is done, the Booster Voltage ON/OFF status is OFF.

(4) Booster voltage ON (BSTON)
This is Power Supply ON Command.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	1	1	03

When this command is executed, the LCD drive power supply circuit is turned ON.
Sleep in/out Command can also turn ON/OFF the LCD drive power supply circuit, but this command turns ON the LCD drive power supply circuit independently.

* After reset is done, the Booster Voltage ON/OFF status is OFF.

(5) TEST mode
This is IC Test Mode Command.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	1	0	0	04

(6) Read display status (RDDST)
This command is for reading statuses of the IC.

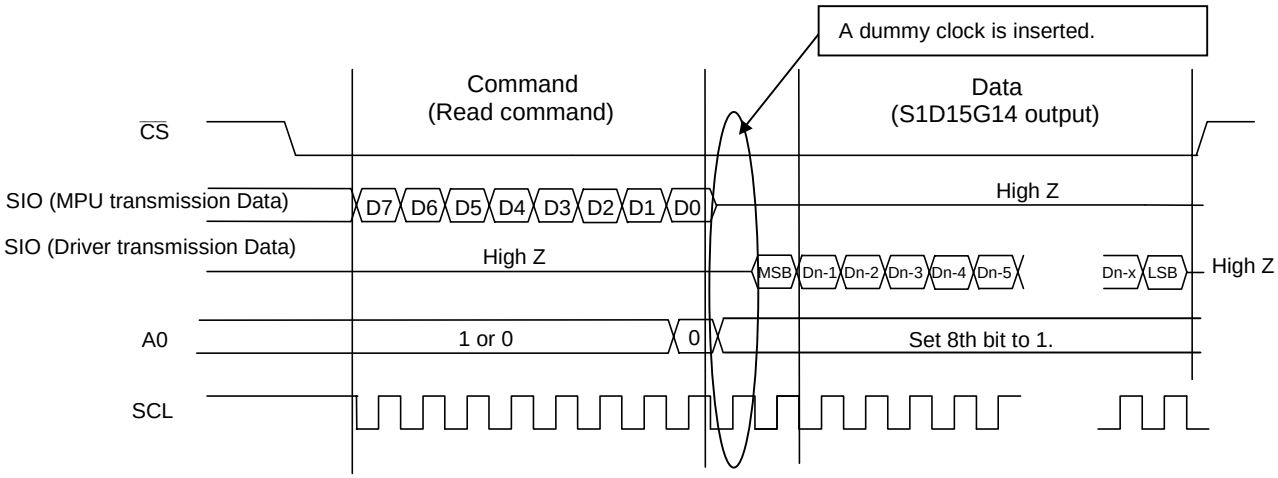
D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	1	0	0	1	09

After this command is input, 32-bit data are read that show statuses of the IC.

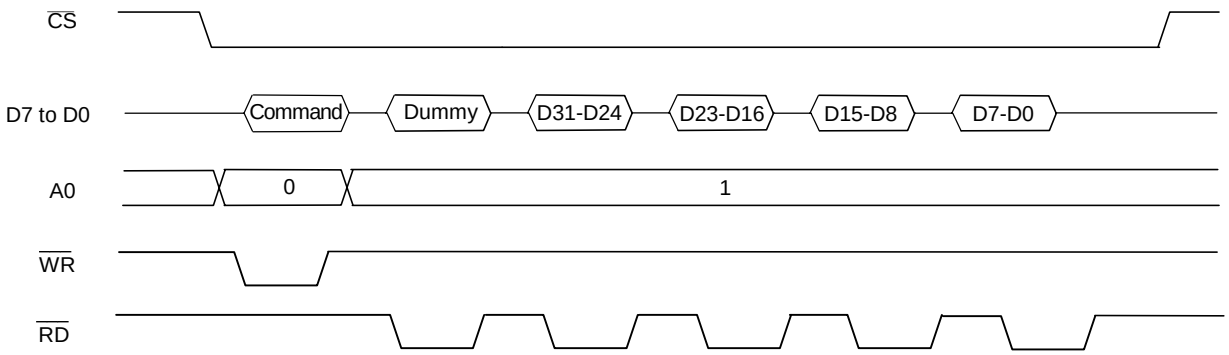
D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	1	0	0	1	09
1	DD	DD	DD	DD	DD	DD	DD	DD	DD
1	D31	D30	D29	D28	D27	D26	D25	D24	XX
1	D23	D22	D21	D20	D19	D18	D17	D16	XX
1	D15	D14	D13	D12	D11	D10	D9	D8	XX
1	D7	D6	D5	D4	D3	D2	D1	D0	XX

DD : Dummy data
Data to be read first after the command is input becomes a dummy data.

The $\overline{CS}$ pin must be at the LOW level until execution of this command reads the 4th byte status. Maintain the timing in the following diagram.



For 8-bit interface



80 series parallel interface

Details of D0 to D31

Bit	Descriptions
31	Booster voltage status
30	Page address order
29	Column address order
28	Page/column order
27	Line address order
26	RGB/BGR order
25	0 is set all the time.
24	0 is set all the time.
23	Switching between com outputs and RAM
22	Interface color pixel format definition
21	
20	
19	Idle mode ON/OFF
18	Partial mode ON/OFF
17	Sleep in/out
16	Display normal mode
15	Vertical scrolling ON/OFF
14	0 is set all the time.
13	Inversion ON/OFF
12	All pixels ON
11	All pixels OFF
10	Display ON/OFF
9	Indefinite
8	Gamma curve selection
7	
6	
5	0 is set all the time.
4	0 is set all the time.
3	0 is set all the time.
2	0 is set all the time.
1	0 is set all the time.
0	0 is set all the time.

B31 is for booster voltage status:
shows operating statuses of the built-in power supply circuit.
1 : The built-in power supply circuit is turned ON.
0 : The built-in power supply circuit is turned OFF.
“0” is returned in the sleep status.

B30 is for page address order (serial interface → display driver).
shows the page address order when display data is written.
0 : Access from the top address to the bottom address.
1 : Access from the bottom address to the top address.

B29 is for column address order (serial interface → display driver).
shows the column address order when display data is written.
0 : Access from the top address to the bottom address.
1 : Access from the bottom address to the top address.

B28 is for page/column block selection (serial interface → display driver).
shows that display data is written in any direction of the page/column direction.
0 : Write in the page direction
1 : Write in the column direction.

B27 is for Common scanning direction.
shows in which direction the common driver is scanned.
0 : Scanning from the top to the bottom.
1 : Scanning from the bottom to the top.

B26 is for RGB - BGR order (MPU → Driver).
shows the RGB-BGR order in writing display data in the display RAM.
0 : RGB
1 : BGR

B25 : 0 is read all the time.

B24 : 0 is read all the time.

B23 is for switching between RAM and common outputs (RAM → common outputs).
shows the relations between common address and common output.
0 : Normal
1 : Vertical reverse

B22, B21, B20 : Interface color pixel format definition.
shows settled statuses of the interface color pixel format.

Format	B22	B21	B20
Not defined	0	0	0
Not defined	0	0	1
8 bit/pixel	**0**	**1**	**0**
12 bit/pixel	**0**	**1**	**1**
Not defined	1	0	0
Not defined	1	0	1
Not defined	1	1	0
Not defined	1	1	1

B19 is for idle mode.
shows if the idle mode is ON.
0 : The Idle Mode is OFF. (Normal mode)
1 : The Idle Mode is ON. (Reduced color mode)

B18 is for partial mode.
shows if the partial mode is ON.
0 : The Partial Mode is OFF.
1 : The Partial Mode is ON.

B17 is for "Sleep in/out".
shows if the sleep-in status is ON.
0 : Sleep-in status
1 : Sleep-out status

B16 is for "Display normal mode".
shows if the normal mode is ON.
0 : The Normal Mode is OFF.
1 : The Normal Mode is ON.

B15 is for Vertival scroll mode.
shows ON/OFF status of the vertical scroll.
0 : Vertical scroll is OFF.
1 : Vertical scroll is ON.

B14 : 0 is read all the time.

B13 is for inversion ON/OFF.
shows if the screen is normal/inverted.
0 : The screen is normal.
1 : The screen is inverted.

B12 is for all pixels ON.
shows if all pixels are ON.
0 : Normal status
1 : All screens are ON.

B11 is for all pixels OFF.
shows if all pixels are OFF.
0 : Normal status.
1 : All screens are OFF.

B10 is for display ON/OFF.
shows if display is ON or OFF.
0 : Display is OFF.
1 : Display is ON.

B9 : Becomes indefinite.

Gamma curve selection (B8, B7, B6).
shows which register is selected out of the two-gradation setting.

GAMMA CURVE SELECTION	B8	B7	B6
GCP0 is selected	**0**	**0**	**0**
GCP1 is selected	**0**	**0**	**1**
not defined	0	1	0
not defined	0	1	1
not defined	1	0	0
not defined	1	0	1
not defined	1	1	0
not defined	1	1	1

The default value after reset

Bit	Descriptions	Default value	Status
31	Booster voltage status	0	Built-in power supply OFF
30	Page address order	0	Top to Bottom
29	Column address order	0	Top to Bottom
28	Page/column order	0	Column direction
27	Line address order	0	Top to Bottom
26	RGB/BGR order	0	RGB
25	0 is set all the time.	0	—
24	0 is set all the time.	0	—
23	Switching between com outputs and RAM	0	Normal mode
22	Interface color pixel format definition	0	12bit/pixel
21		1	
20		1	
19	Idle mode ON/OFF	0	Normal mode
18	Partial mode ON/OFF	0	No partial
17	Sleep in/out	0	Sleep-in
16	Display normal mode	1	Normal mode
15	Vertical scrolling ON/OFF	0	Scrolling OFF
14	0 is set all the time.	0	—
13	Inversion ON/OFF	0	Display normal (no inversion)
12	All pixels ON	0	Normal
11	All pixels OFF	0	Normal
10	Display ON/OFF	0	Display OFF
9	Indefinite	Indefinite	—
8	Gamma curve selection	0	GCP0
7		0	
6		0	
5	0 is set all the time.	0	—
4	0 is set all the time.	0	—
3	0 is set all the time.	0	—
2	0 is set all the time.	0	—
1	0 is set all the time.	0	—
0	0 is set all the time.	0	—

(7) Sleep in (SLPIN)
This command is sued to set the IC to the sleep status.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	1	0	0	0	0	10

When this command is input, all LCD driver output pins are set to the V_C level and the LCD drive power supply circuit and the built-in oscillator are turned OFF. Since the LCD drive power supply circuit is OFF, all LCD driver output pins come to the GND level and to the still status. The display ON/OFF status before input of this command determines how this circuit gets in the sleep status.

When the display is ON:
the circuit gets in the sleep status in the time of 2 to 3 frames after the command is input.
When the display is OFF:
the circuit gets in the sleep status right after the command is input.

The following command enables to get out of the status set by this command.

Exit commands	HEX
Sleep out	11

***** After reset is done, the Sleep in/out status is IN.

(8) Sleep out (SLPOUT)
This command cancels sleep status of this IC.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	1	0	0	0	1	11

The display ON/OFF status before input of this command determines how this circuit gets out of the sleep status.

When the display is ON:
the display is turned on in the time of 3 frames after this command is input.
When the display is OFF:
input the display ON command 40ms or more later after inputting the sleep out command.

***** After reset is done, the Sleep in/out status is IN.

(9) Partial mode ON (PTLON)
When this command is input, the partial display is turned ON.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	1	0	0	1	0	12

The following command enables to get out of the status set by this command.

Exit commands	HEX
Normal display mode ON	13

Use the Partial Area command to set partial areas.

For common/segment driver output, the display OFF level is output in other than the partial display area irrespective of gradation setting. Also, this command does not allow accessing the display RAM.

***** After reset is done, the Normal display mode status is ON.

(10) Normal display mode ON (NORON)
This command is for setting the normal display status.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	1	0	0	1	1	13

***** After reset is done, the Normal display mode status is ON.

(11) Display Inversion OFF
This command is for making display normal.
The normal display status means that the effective value of voltage applied to the LCD becomes the maximum when the RAM data is “1111.” Also, this command is executed without changing the display memory.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	0	0	0	0	20

***** After reset is done, the Display inversion status is OFF.

(12) Display Inversion ON
This command is for inverting display.
The inverted display status means that the effective value of voltage applied to the LCD becomes the maximum when the RAM data is “0000.” Also, this command is executed without changing the display memory.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	1	0	1	21

The following command enables to get out of the status set by this command.

Exit commands	HEX
Display inversion OFF	20

***** After reset is done, the Display inversion status is OFF.

(13) All pixels OFF
This command is for turning OFF all LCD displays.
The display on status means that the effective value of voltage applied to LCD becomes the maximum.
After this command is executed, the access to the RAM stops, and the LCD driver output is fixed to the OFF level irrespective of gradation pulse setting.
Also, this command is executed irrespective of status of the display memory.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	0	0	1	0	22

The following command enables to get out of the status set by this command.

Exit commands	HEX
Partial mode ON	12
Normal display mode ON	13

***** After reset is done, the All pixel status is OFF and Display OFF status.

(14) All pixels ON
This command is for turning on all LCD displays.
The display ON status means that the effective value of voltage applied to LCD becomes the maximum.
After this command is executed, the access to the RAM stops, and the LCD driver output is fixed to the on level irrespective of gradation pulse setting.
Also, this command is executed irrespective of status of the display memory.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	0	0	1	1	23

The following command enables to get out of the status set by this command.

Exit commands	HEX
Normal display mode ON	13
Partial mode ON	12

* After reset is done, the All pixel status is OFF and Display OFF status.

(15) Write contrast (WRCNTR)
This command is for setting contrast of the LCD display.
Execution of this command changes the LCD drive voltage output to segment/common driver.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	0	1	0	1	25

Parameter to be input after this command sets contrasts.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
1	P7	P6	P5	P4	P3	P2	P1	P0	XX

These parameter values are for setting 0 to 127. (Set “0” for P7.)
The center value is 63, and the LCD drive voltage rise when the parameter is set large and the voltage reduces when the parameter is set small.

***** All default values for P7 to P0 after resetting are 63.

(16) Display OFF
This command is for turning OFF the LCD display.
When this command is input, the access to the RAM stops and the driver output changes as follows:
Segment : OFF level is output irrespective of RAM data and gradation setting.
Common : The same as the display on status.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	0	0	0	28

The following command enables to get out of the status set by this command.

Exit commands	HEX
display ON	29

***** After reset is done, the Display status is OFF.

(17) Display on
This command is for turning on the LCD display.
When this command is input, the display corresponding to the display RAM data and display setting is output to the LCD driver.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	0	0	1	29

***** After reset is done, the Display status is OFF.

(18) Column address set (CASET)
This command is for setting column addresses.
When display data is transferred from the MPU to the display RAM, this command is used to set a write area. In case of column address scanning, addresses are incremented from the start address to the end address and the page address is increased by 1, then, the column address returns to the start column. When executing this command, set the start column and the end column at the same time so that the start column becomes smaller than the end column.
Also, if the column address is set outside the display RAM area, data writing outside the area is ignored and correct data is not read in reading data.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	0	1	0	2A

Set the 8-bit start column address and the 8-bit end column address according to parameters to be input after this command.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	0	1	0	2A
1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	XX
1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	XX

* Default values after reset are as follows.
SC7 to SC0: 0
EC7 to EC0: 103 (RAMDIV pin=LOW), 97 (RAMDIV pin=HIGH)

(19) Page address set (PASET)
This command is for setting page addresses.
When display data is transferred from the MPU to the display RAM, this command is used to set a write area. In case of page address scanning, addresses are incremented from the start address to the end address and the column address is increased by 1, then, the page address returns to the start page. When executing this command, set the start page and the end page at the same time so that the start page becomes smaller than the end page.
Also, if the page address is set outside the display RAM area, data writing outside the area is ignored and correct data is not read in reading data.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	0	1	1	2B

Set the 8-bit start page address and the 8-bit end page address according to parameters to be input after this command.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	0	1	1	2B
1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	XX
1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	XX

* Default values after reset are as follows.
SP7 to SP0: 0
EP7 to EP0: 83 (RAMDIV pin=LOW), 66 (RAMDIV pin=HIGH)

(20) Memory write (RAMWR)
This command is for writing data in the display RAM.
When this command is input, the page address and the column address turn into the start address. When data is written in the display RAM, the column address or the page address is increased by 1. When any other command is input, this IC gets out of the status set by this command.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	1	0	0	2C

After inputting this command, you can write display data.

Sequence to write in the display RAM

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	1	0	0	2C
1	D7	D6	D5	D4	D3	D2	D1	D0	XX
1	D7	D6	D5	D4	D3	D2	D1	D0	XX
					.				
					.				
1	D7	D6	D5	D4	D3	D2	D1	D0	XX
1	D7	D6	D5	D4	D3	D2	D1	D0	XX

The following command enables to get out of the status set by this command.

Exit commands	HEX
Any other command	XX

(21) Colour set (RGBSET)
This command is for setting the look-up table of display colors.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	1	1	0	1	2D

Display information is set according to parameters to be input after this command. The look-up table is used when the 256-color mode is set by the interface color pixel format command.
After selecting 256 colors (8 bits : RRRGGGBB) from 4096 colors (12 bits : RRRRGGGGBBBB), use them as follows:

RED

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX	INDEX
0	0	0	1	0	1	1	0	1	2D	—
1	x	x	x	x	R3	R2	R1	R0	XX	0
1	x	x	x	x	R3	R2	R1	R0	XX	1
1	x	x	x	x	R3	R2	R1	R0	XX	2
1	x	x	x	x	R3	R2	R1	R0	XX	3
1	x	x	x	x	R3	R2	R1	R0	XX	4
1	x	x	x	x	R3	R2	R1	R0	XX	5
1	x	x	x	x	R3	R2	R1	R0	XX	6
1	x	x	x	x	R3	R2	R1	R0	XX	7

GREEN

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX	INDEX
1	x	x	x	x	G3	G2	G1	G0	XX	0
1	x	x	x	x	G3	G2	G1	G0	XX	1
1	x	x	x	x	G3	G2	G1	G0	XX	2
1	x	x	x	x	G3	G2	G1	G0	XX	3
1	x	x	x	x	G3	G2	G1	G0	XX	4
1	x	x	x	x	G3	G2	G1	G0	XX	5
1	x	x	x	x	G3	G2	G1	G0	XX	6
1	x	x	x	x	G3	G2	G1	G0	XX	7

BLUE

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX	INDEX
1	x	x	x	x	B3	B2	B1	B0	XX	0
1	x	x	x	x	B3	B2	B1	B0	XX	1
1	x	x	x	x	B3	B2	B1	B0	XX	2
1	x	x	x	x	B3	B2	B1	B0	XX	3

***** After reset is done, values in the look-up table become unstable. Perform initialization.

(22) RAM data read

This command is for reading data from the display RAM.

After this command is input, the read status becomes available. Also, when this command is input, the page address and the column address are always set to the start address. When any data is read after this command, the contents of the display data RAM can be read, and the page address or the column address is incremented at the same time. When any command is input, the data reading is automatically cancelled.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	0	1	1	1	2E

Execute this command as per the following procedures;

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	0	0	1	1	1	2E
1	RD	RD	RD	RD	RD	RD	RD	RD	XX

RD : Display RAM data

(23) Partial area (PLTAR)

This command is for setting display areas at the time of partial display.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	0	0	0	30

The areas are set according to two parameters to be input after this command.

This command is set as follows:

1. Input the command.
2. Set the start line (8 bits).
3. Set the end line (8 bits).

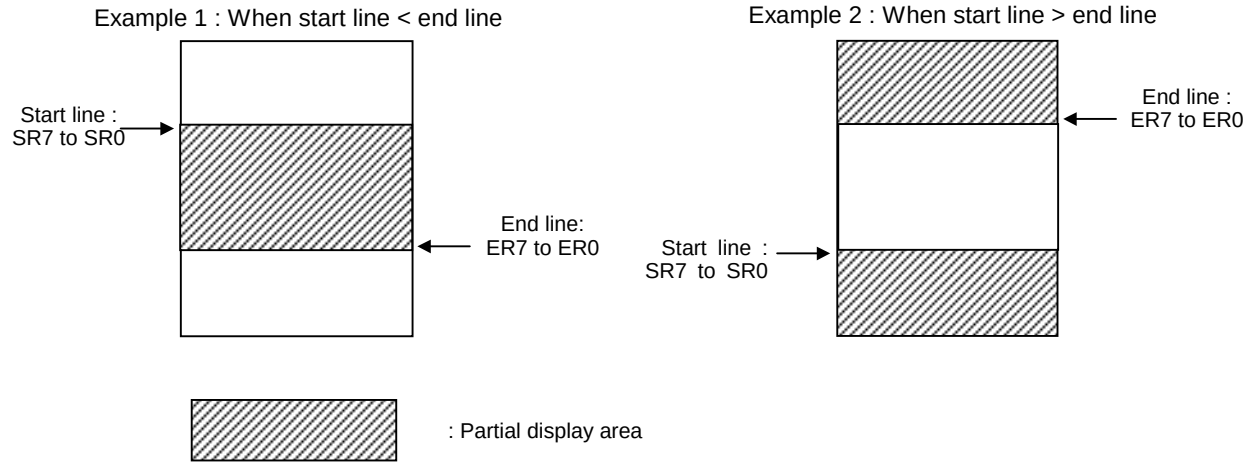
D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	0	0	0	30
1	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	XX
1	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	XX

S1D15G14 turns into the following status in partial non-display area:

Driver output : Display OFF is output irrespective of RAM data and gradient setting.

RAM access : None

The following shows setting examples of display area:



* Default values after reset are as follows.

SR7 to SR0: 0

ER7 to ER0: 0

(24) Vertical scrolling definition (VSCRDEF)
This command is for setting vertical scrolling areas.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	0	1	1	33

Scrolling areas are set according to three parameters to be input after this command. This command is executed as follows:
1. Input the command.
2. Set the number of lines (TF7 to TF0) to be used as the upper fix area of display in the display memory. When all parameters are 0, the upper fix area does not exist.
3. Set the number of lines (SA7 to SA0) to be used as the scrolling area in the display memory.
4. Set the number of lines (BF7 to BF0) to be used as the lower fix area of display in the display memory. When all parameters are 0, the lower fix area does not exist.

The input sequence is as follows:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	0	1	1	33
1	TF7	TF6	TF5	TF4	TF3	TF2	TF1	TF0	XX
1	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	XX
1	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0	XX

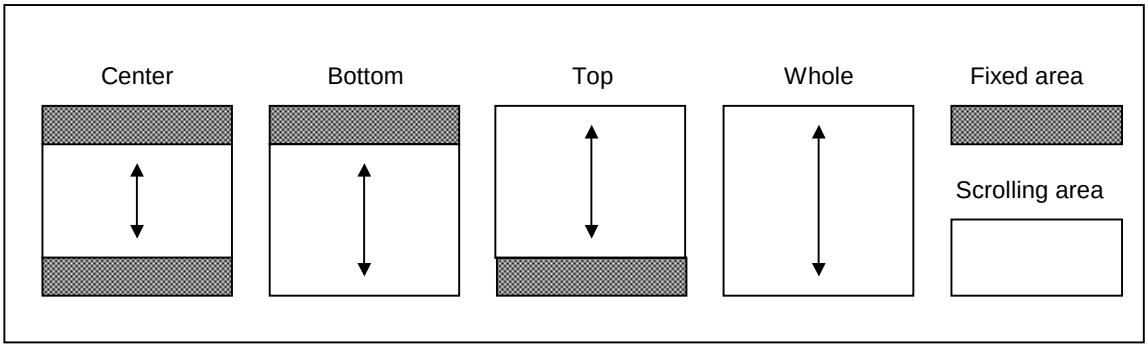


Fig. 1 Display Scroll Mode

Note: The top fixed area changes according to B4 bit of the memory access control command.

* Default values after reset are as follows.
TF7 to TF0: 0
SA7 to SA0: 0
BF7 to BF0: 53H

(25) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	1	0	0	34

(26) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	1	0	1	35

(27) Memory access control (MADCTL)
This command is for setting the method that the MPU accesses the display memory.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	1	1	0	36

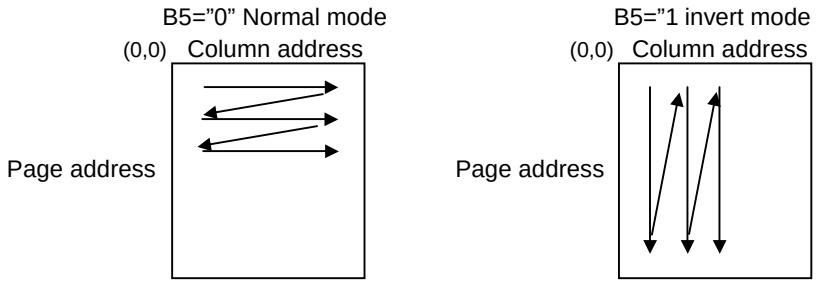
This command is executed as follows:
1. Input the command.
2. Set the memory access direction.
The input sequence is as follows:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	1	1	0	36
1	B7	B6	B5	B4	B3	0	0	B0	XX

B7 : To set the position of Page 0 in the display RAM.
0 : To be arranged in line from the top to the bottom.
1 : To be arranged in line from the bottom to the top.

B6 : To set the position of Column 0 in the display RAM.
0 : To be arranged in line from left to right.
1 : To be arranged in line from right to left.

B5 : To set the page/column direction in writing in the display RAM.
This setting is used for screen rotation.
0 : To be written in the column direction in the normal mode.
1 : To be written in the page direction in the inverting mode.



B4 : To set the scanning direction of the common driver.
0 : To be scanned from the top to the bottom.
1 : To be scanned from the bottom to the top.

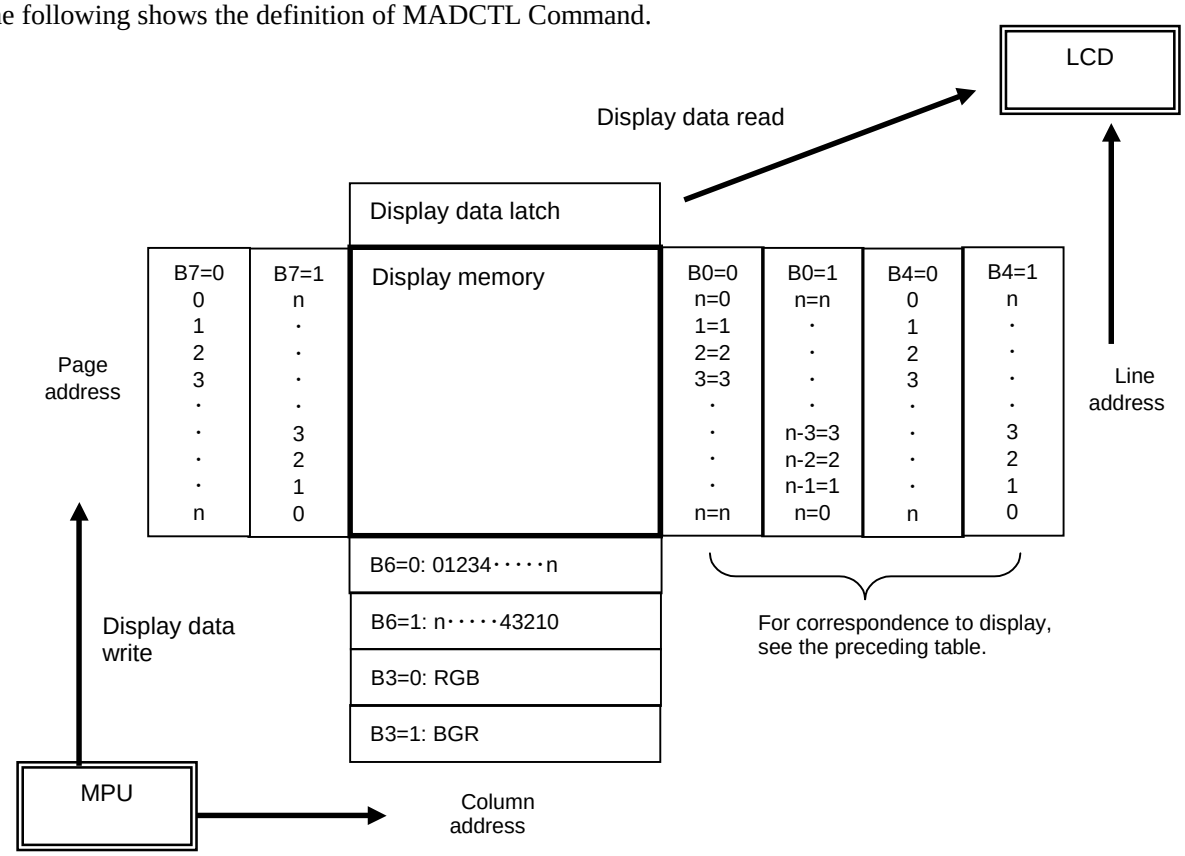
B3 : To set the RGB to BGR sequence.
To set the RGB to BGR sequence in writing from the MPU to the display RAM.
0 : RGB
1 : BGR

B0 : To set relations between the display RAM and the common output.
The screen is vertically inverted by setting the display RAM read sequence by this command.
0 : Normal
1 : Vertical inversion

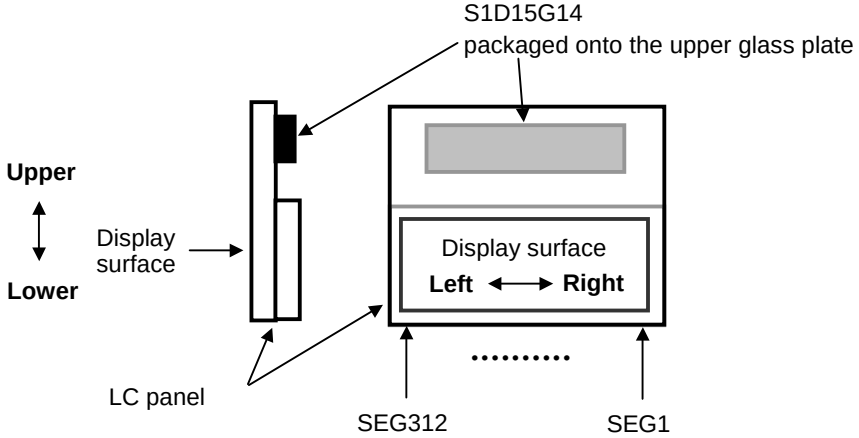
Combination of B4 and B0 (Function of S1D15G14)

B4	B0	Display RAM read sequence	Common scanning direction	Display state
0	0	Top → Bottom	Top → Bottom	Normal
0	1	Bottom → Top	Top → Bottom	Vertical inversion
1	0	Bottom → Top	Bottom → Top	Normal
1	1	Top → Bottom	Bottom → Top	Vertical inversion

The following shows the definition of MADCTL Command.



Also, in this command description, the display of head, tail, left and right is defined under the condition where the driver is mounted to the liquid crystal panel as shown below and the DISCTL command (B6h)'s parameter P32= "0" is set.



* Default values after reset are as follows.
  B7: From top to bottom
  B6: From left to right
  B5: Normal mode
  B4: From top to bottom
  B3: RGB
  B0: Normal

(Note)
Parameter P32 of the DISCTL command defines the top and bottom values of this command.

(28) Vertical scrolling start address (VSCRSADD)
This command is for setting scrolling start addresses.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	1	1	1	37

Note : This command is input at the time of vertical scrolling. The set vertical scrolling addresses become valid from the next frame of the display.

The vertical scrolling start address is set according to one parameter to be input after this command. The address in the display RAM to be shown by this start address is the top of the scrolling area in the display area.
This command is executed as follows:
1. Input this command.
2. Set the display RAM start address 8 bits.
The input sequence is as follows:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	0	1	1	1	37
1	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	XX

Note : Positions of top fixed area, scrolling area and bottom fixed area are changed according to B4 bit of the memory access control command (MADCTL).
The displayed position turns 180 degrees when “1” is set to B4 bit.

The following command enables to get out of the status set by this command.

Exit commands	HEX
Normal display mode ON	13
Partial mode ON	12

* Default values after reset are as follows.
  SA7 to SA0: 0

(29) Idle mode OFF (IDMOFF)
This command is used to cancel the idle mode of this IC.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	1	0	0	0	38

***** After reset is done, the idle mode status is OFF.

(30) Idle mode ON (IDMON)
This command is used to select the idle mode.
The idle mode is used to display in reduced number of colors (8-color display). In case of display in reduced number of colors, the most significant bit out of 4 bits each of RGB in the display RAM is used for display data. Other bits exert no influence on display.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	1	0	0	1	39

***** After reset is done, the idle mode status is OFF.

(31) Interface pixel format (COLMOD)
This command is for setting the pixel format when the MPU writes data in the display RAM.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	1	0	1	0	3A

The format is set according to one parameter to be input after this command.
This command is executed as follows:
1. Input this command.
2. Set the pixel format.
The input sequence is as follows:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	1	1	1	0	1	0	3A
1	X	X	X	X	X	P2	P1	P0	XX

x : Bits to be ignored. Either of “0” and “1” will do.

Interface Formats	P2	P1	P0
Not defined	0	0	0
Not defined	0	0	1
8 bit/pixel	0	1	0
12 bit/pixel	0	1	1
Not defined	1	0	0
Not defined	1	0	1
Not defined	1	1	0
Not defined	1	1	1

When 8-bit/pixel = 256-color display is selected, data transmitted from the MPU are converted in the look-up table and are written in the display RAM.

* Default values after reset are as follows.
P2, P1, P0: 0, 1, 1 12 bits/pixel is selected.

(32) TEST mode (TSTMOD)
This command is used to test the IC.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	**1**	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**DE**

When this command is input, the IC gets into the test mode and comes not to accept other commands. If this command is input due to noise or other reason, the NOP command or NOP2 enables to get out of the test mode. When the IC enters the test mode, the display indications may become incorrect. In this case, the following phenomena may occur.
・The selective polarity is outputted for more than one of the common pins.
・The LCD reference voltage's temperature gradient changes.
・Oscillation stops.
・The normal oscillation frequency and reference voltage values change.

(33) Nop Operation 2(NOP2)
This is Non-operation command ②.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	0	1	0	1	0	AA

This command does not affect other operations.

(34) Initial escape
This command is for initialization of settings inside the IC.
Input this command in the order shown in the example of software setup.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	1	0	0	0	1	1	0	C6

(35) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	1	0	1	1	0	1	0	DA

(36) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	1	0	1	1	0	1	1	DB

(37) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	1	0	1	1	1	0	0	DC

(38) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	0	1	0	B2

(39),(40) Gray scale position set (GCPSET0, GCPSET1)
These commands are for setting gray scale positions.
Since this IC is provided with two series of registers, these commands GCPSET0 and GCPSET1 are used to set them.

GCPSET0 Command

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	0	1	1	B3

GCPSET1 Command

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	0	0	B4

These commands are executed as follows:

GCPSET0

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	0	1	1	B3
1	P17	P16	P15	P14	P13	P12	P11	P10	XX
1	P27	P26	P25	P24	P23	P22	P21	P20	XX
↓	↓	↓	↓	↓	↓	↓	↓	↓	XX
1	P157	P156	P155	P154	P153	P152	P151	P150	XX

GCPSET1

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	0	0	B4
1	P17	P16	P15	P14	P13	P12	P11	P10	XX
1	P27	P26	P25	P24	P23	P22	P21	P20	XX
↓	↓	↓	↓	↓	↓	↓	↓	↓	XX
1	P157	P156	P155	P154	P153	P152	P151	P150	XX

P17 to P10 : GCP1 : Gray level to be output when the RAM data is “0001.”
P27 to P20 : GCP2 : Gray level to be output when the RAM data is “0010.”
•
•
P157 to P150 : GCP15 : Gray level to be output when the RAM data is “1111.”

Note :
1. Set this register before executing Sleep Out Command. Do not change it during display.
2. Select any setting area from 2 to (Clock count in 1 section term to be set at P1 of DISCTL).
3. Be sure to observe the following relations:
   GCP1<GCP2 • • • < GCP15
4. Outputs at the time of RAM data = “0000” are fixed.

***** After reset is done, values of registers become unstable. Perform initialization.

(41) Gamma Curve set (GAMSET)
This command is for setting selection of two GCP registers.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	0	1	B5

This command is executed as follows:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	0	1	B5
1	*	*	*	*	*	*	P11	P10	XX

P10, P11 : Selects the GCP register.
0 : GCPSET0 is selected.
1 : GCPSET1 is selected.

P11	P10	GCP register
0	0	The previous status is preserved.
0	1	GCP0 is selected.
1	0	GCP1 is selected.
1	1	The previous status is preserved.

***** After reset is done, values of registers become P11, P10=0,1.

(42) Display control (DISCTL)
This command is for setting displays.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	1	0	B6

This command is executed as follows:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	0	1	0	B6
1	P17	P16	P15	P14	P13	P12	P11	P10	XX
1	P27	P26	P25	P24	P23	P22	P21	P20	XX
1	P37	*	P35	P34	P33	P32	P31	P30	XX
1	*	P46	P45	P44	P43	P42	P41	P40	XX
1	*	P56	P55	P54	P53	P52	P51	P50	XX
1	*	P66	P65	P64	P63	P62	P61	P60	XX
1	P77	P76	P75	P74	P73	P72	P71	P70	XX

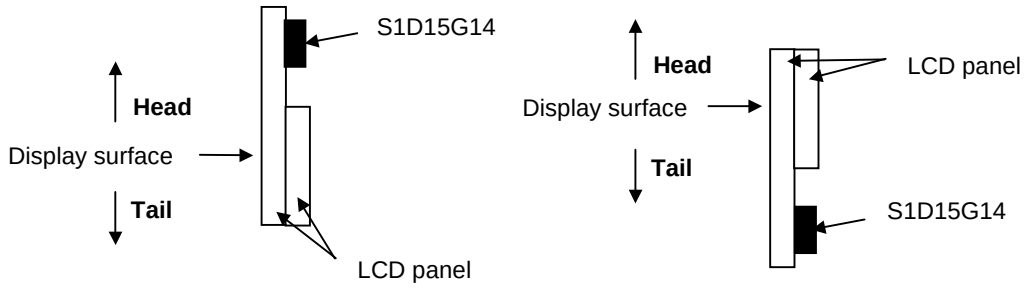
P17 to P10: To set the length of one selection term by the number of issues of the oscillation clock.
This value must be larger than those set by the GCPSET0 and GCPSET1 commands.
P27 to P20: To set N inversions.
P27 = 0: To execute N line inversion at the cycle set by P26 to P20.
1: No N line inversion
P26 to P20: To set the cycle of N line inversion.
The set value brings an inversion cycle. Set the value between 2 and 127.
P37: To set frame frequency in the idle mode.
0 : No division from oscillation frequency
1 : 2 divisions of oscillation frequency
P35 to P33: To set bias rate of LCD drive voltage.

P2	P1	P0	Bias Rate
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5

Note : This parameter value and external parts are changed according to bias rate.

P32: shows how the IC is installed on the panel.
0: IC is installed on top of the module.
1: IC is installed under the module.
The display's head and tail are determined by referencing this parameter.
Basically, P32 = "0" is recommended for use.

When installing the IC on top of the module (P32=0) When installing the IC under the module (P32=1)



P31: To set the column direction size of the RAM.
0 : 98×67 or 98×84
1 : 104×67 or 104×84
Note : The RAMDIV pin changes the page direction size.
P30: To set display duty.
0: 1/82
1: 1/67
P47 to P40, P67 to P60 : To set duty in 1/82 duty.
Set P47 to P40 = 84 and P87 to P60 = 82.
According to this parameter setting, the display line is set to 82 and the actual drive duty is set to 84.
The 2 horizontal intervals, which is the difference between the display line and the drive duty, are required for operating the IC. Between the 2 horizontal intervals, the segment output will be in non-display output (off line interval).
(Note) Do not rewrite this parameter while it is displayed.
P57 to P50, P77 to P70 : To set duty in 1/67 duty.
Set P57 to P50 = 69 and P77 to P70 = 67.
According to this parameter setting, the display line is set to 67 and the actual drive duty is set to 69.
The 2 horizontal intervals, which is the difference between the display line and the drive duty, are required for operating the IC. Between the 2 horizontal intervals, the segment output will be in non-display output (off line interval).
(Note) Do not rewrite this parameter while it is displayed.

***** After reset is done, values of registers become unstable. Perform initialization.
This command is restricted as follows:
S1D15G14D01B000: Do not rewrite the set value after resetting the set value of this command.
This restriction is not applied in S1D15G14D02B000.

(43) Temperature gradient set(TMPGRD)
This command is for setting temperature gradients of LCD drive voltage.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	1	1	B7

This command is executed as per the following sequence:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	0	1	1	1	B7
1	*	*	*	*	*	*	P11	P10	XX
1	P27	P26	P25	P24	P23	P22	P21	P20	XX
1	P37	P36	P35	P34	P33	P32	P31	P30	XX
1	P47	P46	P45	P44	P43	P42	P41	P40	XX
1	P57	P56	P55	P54	P53	P52	P51	P50	XX
1	P67	P66	P65	P64	P63	P62	P61	P60	XX
1	P77	P76	P75	P74	P73	P72	P71	P70	XX
1	P87	P86	P85	P84	P83	P82	P81	P80	XX
1	P97	P96	P95	P94	P93	P92	P91	P90	XX
1	P107	P106	P105	P104	P103	P102	P101	P100	XX
1	P117	P116	P115	P114	P113	P112	P111	P110	XX
1	P127	P127	P125	P124	P123	P122	P121	P120	XX
1	*	*	*	*	*	*	*	P130	XX
1	P147	P147	P145	P144	P143	P142	P141	P140	XX

P11 and P10: The average LCD driving voltage's temperature gradient shall be set as follows.
Please keep in mind are with tolerance in fact.

P11	P10	Average temperature gradient (%/°C)
0	0	-0.05
0	1	-0.1
1	0	-0.15
1	1	-0.2

P20 to P147: These are the parameter used for the IC test.
Always set P130 to "0". Other parameters should set to either "0" or "1".

* After reset is done, values of registers become unstable. Perform initialization.

(44) TEST mode
This command is for testing IC chips.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	0	0	0	B8

(45) REFSET
Input this command to set up status in the IC.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	0	0	1	B9

This command is executed in the following sequence.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	1	0	1	B9
1	*	*	*	*	*	0	0	0	XX

After reset is done, values of registers become unstable. Perform initialization.

(46) Voltage control (VOLCTL)
This command is for adjusting LCD drive voltage.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	0	1	0	BA

This command is executed as per the following sequence:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	0	1	0	BA
1	*	P16	P15	P14	P13	P12	P11	P10	XX
1	*	*	*	*	*	*	P21	P20	XX

P16 to P10: To set the electronic volume value.
P21 and P20: Always set this parameter to "1."

***** After reset is done, values of registers become unstable. Perform initialization.

(47) Common driver output select(COMOUT)
This command is for setting operations of the common driver.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	1	0	1	BD

This command is executed as per the following sequence:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	1	0	1	BD
1	*	*	*	*	P13	P12	P11	P10	XX

P13: To set the top common for interlace drive.
0 : The COM1 to COM41 side comes first.
1 : The COM42 to COM82 side comes first.
Note : Be sure to set 0 in case of 1/67 duty.
P12: To set interlace drive/Normal drive.
0 : Normal drive
1 : Interlace drive
The interlace drive means that common signals from the IC are arranged in comb shape on the LCD panel for driving.

P11, P10: To set shift direction of the common driver (output sequence of selection pulse).

① When the DISCTL command was used to set 1/67 duty :
P13=0 (Be sure to set it to "0"), P12=1

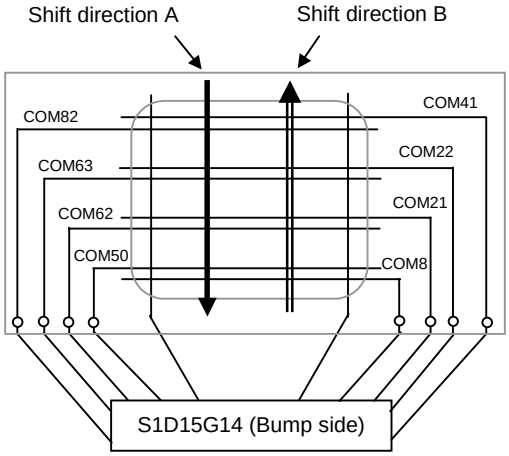
MADCTL Command B4=0 (Top → Bottom)

P11	P10	Order	Shift Direction
0	0	COM8,50··62,21→COM63,22··82,41	B
1	1	COM41,82··22,63→COM21,62··50,8	A

MADCTL Command B4=1 (Bottom → Top)

P11	P10	Order	Shift Direction
0	0	COM41,82··22,63→COM21,62··50,8	A
1	1	COM8,50··62,21→COM63,22··82,41	B

Note : Do not use COM1 to COM7 for 1/67.



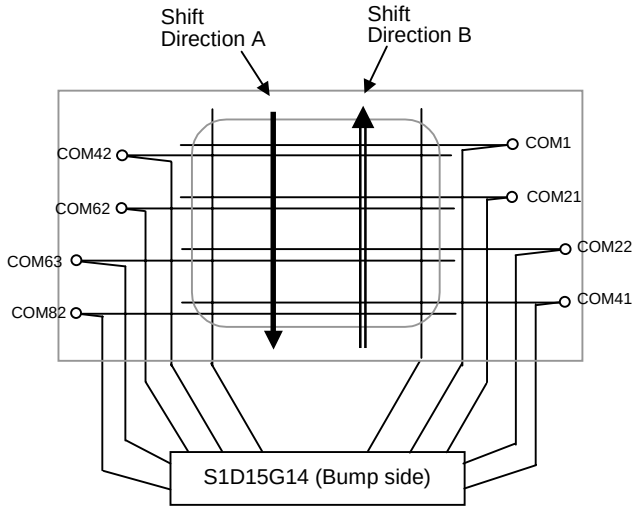
② If 1/82 duty is set by the DISCTL command:
P12=1

MADCTL command B4=0 (top→bottom)

P13	P11	P10	Order	Shift Direction
0	0	0	COM1,42··21,62→COM22,63··41,82	A
0	1	1	COM82,41··63,22→COM62,21··42,1	B

MADCTL command B4=1(bottom→top)

P13	P11	P10	Order	Shift Direction
1	0	0	COM82,41··63,22→COM62,21··42,1	B
0	1	1	COM1,42··21,62→COM22,63··41,82	A



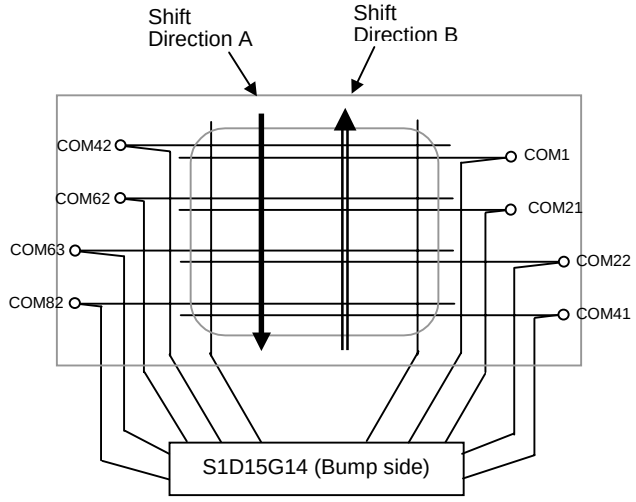
P13=1, P12=1

MADCTL command B4=0 (top→bottom)

P13	P11	P10	Order	Shift Direction
0	0	0	COM42,1··62,21→COM63,22··82,41	A
1	1	1	COM41,82··22,63→COM21,62··1,42	B

MADCTL command B4=1(bottom→top)

P13	P11	P10	Order	Shift Direction
0	0	0	COM41,82··22,63→COM21,62··1,42	B
1	1	1	COM42,1··62,21→COM63,22··82,41	A



(48) Power control (PWRCTL)
This command is for setting the power supply circuit.

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	1	1	0	BE

This command is executed as per the following sequence:

D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	1	1	1	1	1	0	BE
1	*	P16	P15	P14	P13	P12	P11	P10	XX

P16: To set boosting clock's timing to normal mode.
0: To generate the boosting clock with a different timing than the display clock.
Frequency of the boosting clock is set by P12, P11 and P10.
1: To generate the boosting clock with half a clock per selection period later than the display clock.

When the display or fluctuation of the LCD driving voltage, in sync with the display clock, is uneven, setting the parameter to "1" is recommended.

P15: This parameter must be set to "0" for internal setting of the IC.
P14: To switch internal/external resistance used for adjusting V_{1OUT} output voltage.
0: Internal resistance
1: External resistance
P13: To change the output driving capacity of V_{1OUT}.
0: High-power mode
1: Low-power mode

Although setting this parameter to the high-power mode saves current consumption by approximately100 μA, voltage fluctuation may affect the image quality due to the load of the LCD panel. Hence, we recommend that the high-power mode be used.

P12, P11 and P10: To set the frequency of the built-in boosting circuit. The frequency is set by the oscillation clock's division rate.
As indicated below, the frequency varies by the difference between the normal and idle display modes.

P2	P1	P0	Normal mode		Idle mode	
0	0	0	f_{OSC1}/512	1.6kHz typ.	f_{OSC2}/48	0.8kHz typ.
0	0	1	f_{OSC1}/256	3.3kHz	f_{OSC2}/24	1.6kHz
0	1	0	f_{OSC1}/128	6.6kHz	f_{OSC2}/12	3.3kHz
0	1	1	f_{OSC1}/64	13.1kHz	f_{OSC2}/6	6.5kHz
1	0	0	f_{OSC1}/32	26.3kHz	f_{OSC2}/3	13kHz

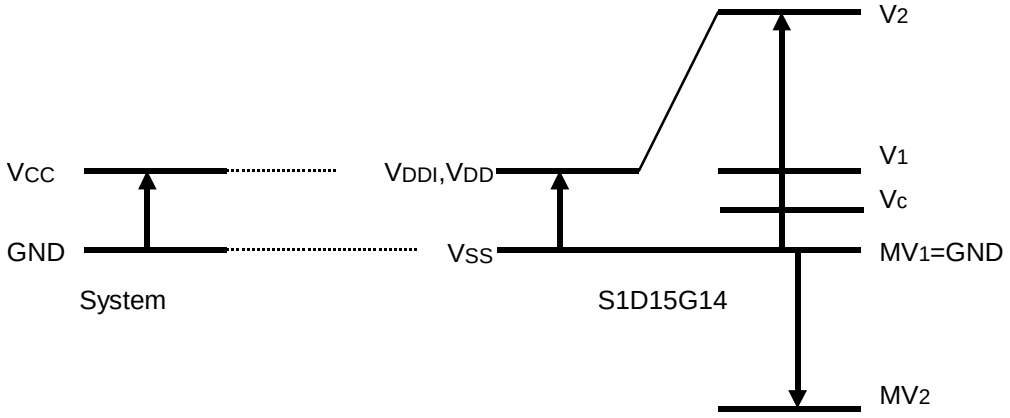
Despite load of the LCD panel, raising the boosting circuit's frequency makes the LCD driving voltage more stable. This increase, however, requires more current consumption. Adjust the value appropriately by checking the display of the LCD panel.

*After reset is done, values of registers become unstable. Perform initialization.

10. ABSOLUTE MAXIMUM RATING

Unless otherwise noted, GND = 0V.

Parameter		Symbol	Conditions	Unit
Power supply voltage (1)		V_{DDI}	-0.3 to +4.0	V
Power supply voltage (2)		V_{DD}	-0.3 to +4.0	V
Power supply voltage (3)		V_2	-0.3 to +16.0	V
Power supply voltage (4)		MV_2	-11.0 to GND	V
Power supply voltage (5)		V_1	-0.3 to V_{DD}	V
Input voltage		V_{IN}	-0.3 to V_{DDI}+0.3	V
Output voltage		V_O	-0.3 to V_{DDI}+0.3	V
Operating temperature		T_{OPR}	-40 to +85	°C
Storage temperature	Bare chip	T_{STR}	-55 to +125	°C



Notes and Conditions
1. Voltage $V_1 \geq V_C \geq GND \geq MV_2$ must always be satisfied.
2. If the LSI exceeds its absolute maximum rating, it may be damage permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.

11. ELECTRIC CHARACTERISTICS

11.1 DC Characteristics

GND = 0V, V_{DD} = 2.85V±10%, Ta = -40 to +85°C unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power supply voltage (1)	V_{DDI}	—	1.6	1.8	V_{DD}	V	V_{DDI}
Power supply voltage (2)	V_{DD}	—	2.35	2.8	3.6	V	V_{DD}
Power supply voltage (3)	V_2	V_2 to MV_2	10	—	25	V	V_2,MV_2
operational voltage	V_2	—	5.0	—	15.0	V	V_2
	V_1	—	1.8	—	3.6	V	V_1
	V_C	—	0.9	—	1.8	V	V_C
	MV_1	—	GND	—	GND	V	GND
	MV_2	—	-10.5	—	-5	V	MV_2
Reference voltage	V_{REG}	Ta=25°C	1.75	1.8	1.85	V	
HIGH-level input voltage	V_{IH}	—	0.7×V_{DDI}	—	V_{DDI}	V	All input
LOW-level input voltage	V_{IL}	—	V_{SS}	—	0.3×V_{DDI}	V	
HIGH-level output voltage	V_{OH}	I_{OH}=-0.3mA	0.8×V_{DDI}	—	V_{DD}	V	All
LOW-level output voltage	V_{OL}	I_{OL}=0.3mA	GND	—	0.2×V_{DDI}	V	input/output, All output,
Input leakage current	I_{LI}	—	-1.0	—	1.0	µA	All input, All input/output
Output leakage current	I_{LO}	—	-3.0	—	3.0	µA	All input/output, All output
LCD driver ON resistance (1)	V2RON	V_2=10.0V, Ta=25°C	—	500	3000	Ω	COMn
LCD driver ON resistance (2)	MV_2 RON	V_C=-7.0V, Ta=25°C	—	500	3000	Ω	COMn
LCD driver ON resistance (3)	V1RON	V_1=2.5V,Io=|0.1|mA Ta=25°C	—	500	1800	Ω	SEGn, V_1,MV_1
LCD driver ON resistance (4)	VCRON	V_C=1.25V, Io=|0.1|mA Ta=25°C	—	400	2400	Ω	SEGn COMn
LCD power supply output impedance (1)	V_{OUT}	1/5 bias, C=1.0µF, Ta=25°C	—	200	400	Ω	V_{OUT}
LCD power supply output impedance (2)	V_2		—	2000	4000	Ω	V_2
LCD power supply output impedance (3)	MV_2		—	1500	3000	Ω	MV_2
LCD power supply output impedance (4)	V_{1OUT}	I_{out}=±100µA, Ta=25°C	—	100	200	Ω	V_{1OUT}
Static current consumption	I_{DDQ}	Ta=25°C	—	0.5	5	µA	V_{DDI}, V_{DD}
	I2Q	V_2=15.0V, Ta=25°C	—	0.1	1	µA	V_2
	I1Q	V_1=2.5V, Ta=25°C	—	0.5	5	µA	V_1
Operating current consumption (1)	IDD	1/6 bias,	—	400	600	µA	
	IDDI	f_{FR}=85Hz, Vseg=3.3V, normal mode	—	1	10	µA	
Operating current consumption (2)	IDD	MPU access under status (1).	—	500	700	µA	
	IDDI	t_{SCYC}=1.5MHz 4096 colors, 15 fps equivalent	—	10	20	µA	
Operating current consumption (3)	IDD	1/6 bias,	—	300	500	µA	
	IDDI	f_{FR}=85Hz, Vseg=3.3V, idle mode	—	1	10	µA	
Oscillation frequency	f_{OSC1}	Ta=25°C	714	840	966	kHz	
	f_{OSC2}	Ta=25°C	33.0	39	43.5	kHz	

Relationship between oscillation frequency f_{OSC1} and frame rate frequency f_{FR}

$f_{FR} = f_{OSC1}$/(display duty)/(number of clock of per 1H)

Example: 840kHz/82/128 =80

Relationship between oscillation frequency f_{OSC2} and frame rate frequency f_{FR}

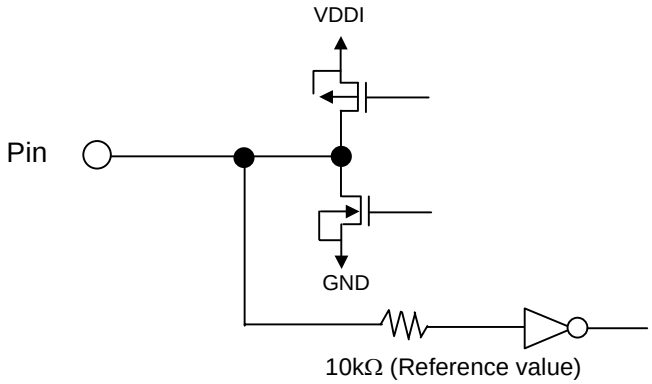
$f_{FR} = f_{OSC2}$/(display duty)/(Dividing ratio×3)

Example: 39kHz/82/(2×3) = 80

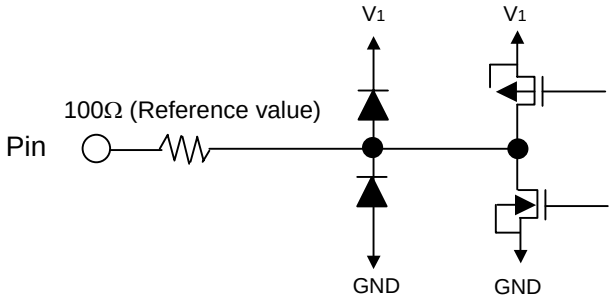
Display duty and number of clocks of per 1H are set up by DISCTL command.

11.2 I/O Circuit Diagram (For Reference)

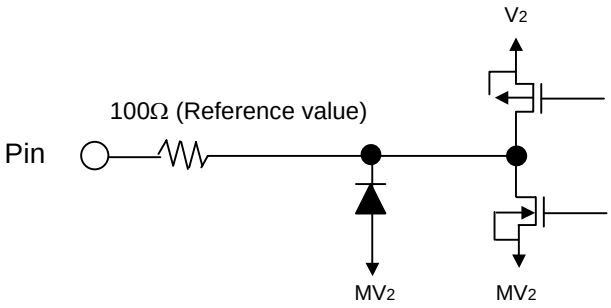
① I/O Pin (Both the input pin and the output pin are of the same structure.)



② Segment Driver

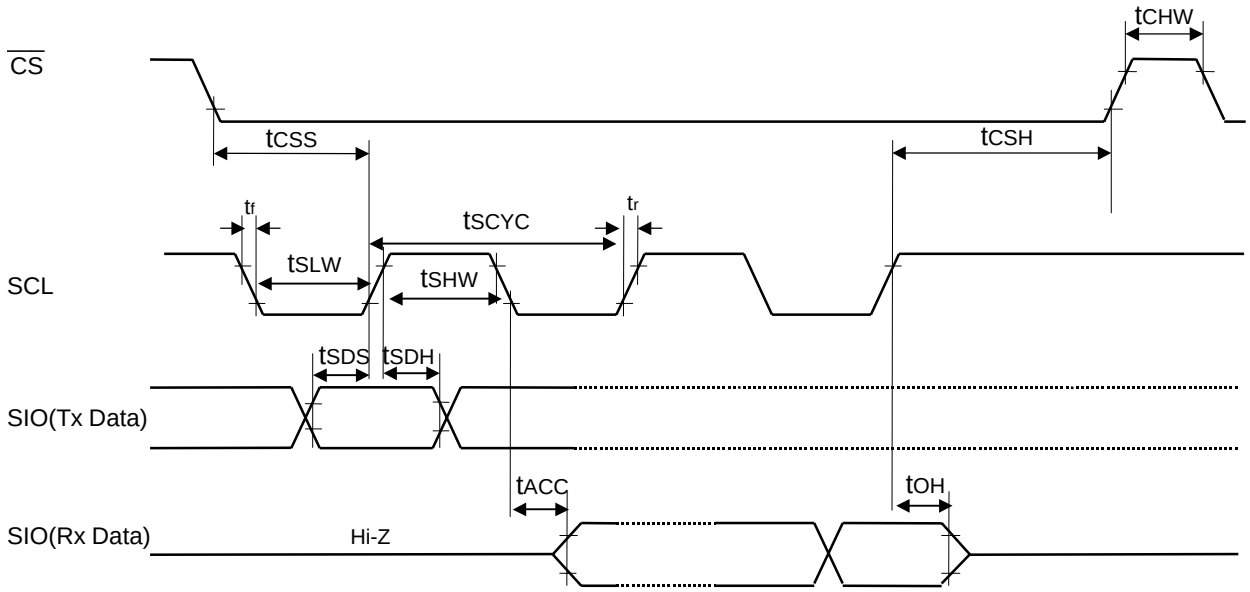


③ Common Driver



12. AC CHARACTERISTICS

12.1 9-bit Serial Interface



V_{DD} = 2.6 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		75	—	ns
Serial clock HIGH pulse width		t_{SHW}	—	30	—	
Serial clock LOW pulse width		t_{SLW}		30	—	
Data setup time	SIO	t_{SDS}		20	—	
Data hold time		t_{SDH}	—	20	—	
Data delay time (Hz-data)	SIO	t_{ACC}	C_L=30pF	—	100	
			C_L=100pF (reference)	—	150	
Data delay time (data-Hz)		t_{OH}	C_L=30pF	20	—	
			C_L=100pF (reference)	20	—	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		40	—	
		t_{CSH}	—	40	—	
		t_{CSHW}		40	—	

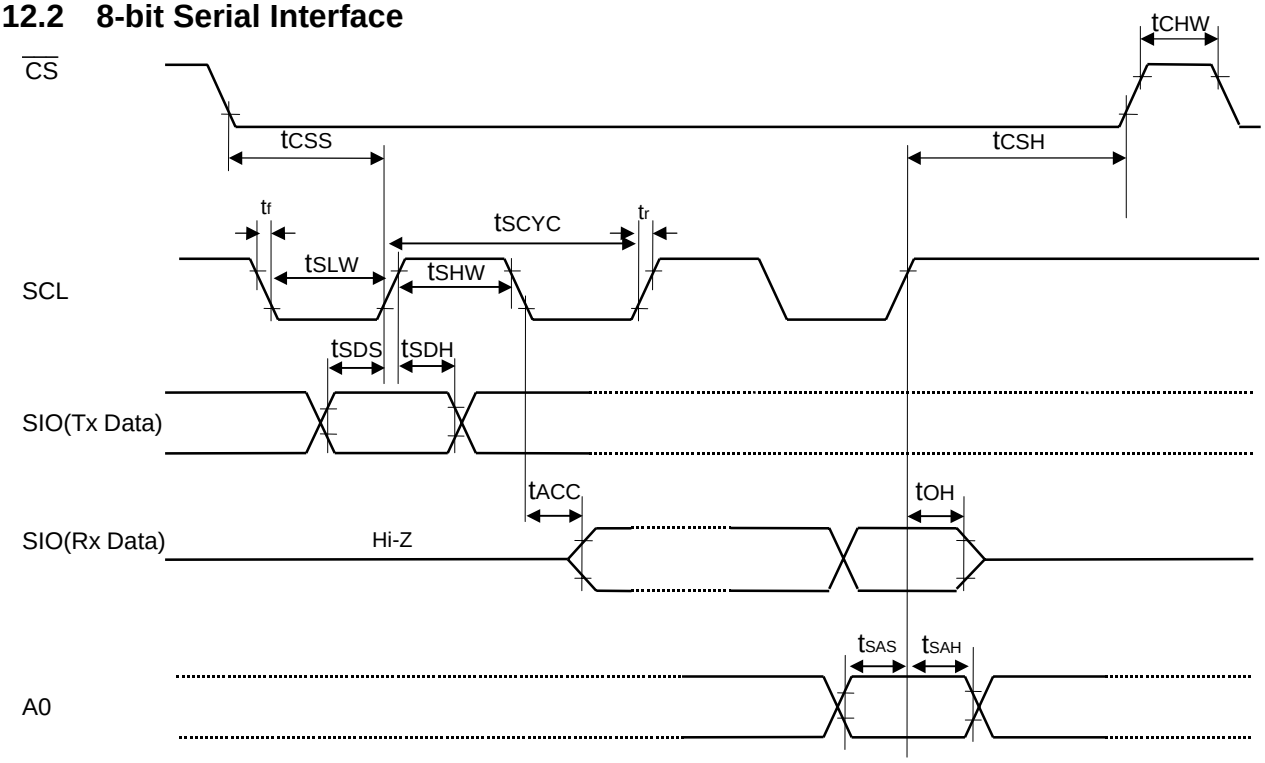
Note1 The rise and fall times (t_r and t_f) of the input signal area specigied for less than 10ns.
Note2 Every timing is specified on the basis of 30% and 70% of V_{DDI}.

V_{DD} = 2.35 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		110	—	ns
Serial clock HIGH pulse width		t_{SHW}	—	50	—	
Serial clock LOW pulse width		t_{SLW}		50	—	
Data setup time	SIO	t_{SDS}		25	—	
Data hold time		t_{SDH}	—	25	—	
Data delay time (Hz-data)	SIO	t_{ACC}	C_L=30pF	—	120	
			C_L=100pF (reference)	—	180	
Data delay time (data-Hz)		t_{OH}	C_L=30pF	25	—	
			C_L=100pF (reference)	25	—	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		50	—	
		t_{CSH}	—	50	—	
		t_{CSHW}		50	—	

Note1 The input signal rise time and fall time (tr, tf) are specified less than 10 ns.
Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

12.2 8-bit Serial Interface



V_{DD} = 2.6 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		75	—	ns
Serial clock HIGH pulse width		t_{SHW}	—	30	—	
Serial clock LOW pulse width		t_{SLW}		30	—	
Address setup time	A0	t_{SAS}	—	100	—	
Address holds time		t_{SAH}		30	—	
Data setup time	SIO	t_{SDS}	—	20	—	
Data hold time		t_{SDH}		20	—	
Data delay time (Hz-data)	SIO	t_{ACC}	C_L=30pF	—	100	
			C_L=100pF (reference)	—	150	
Data delay time (data-Hz)		t_{OH}	C_L=30pF	10	—	
			C_L=100pF (reference)	20	—	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		50	—	
		t_{CSH}	—	50	—	
		t_{CSHW}		50	—	

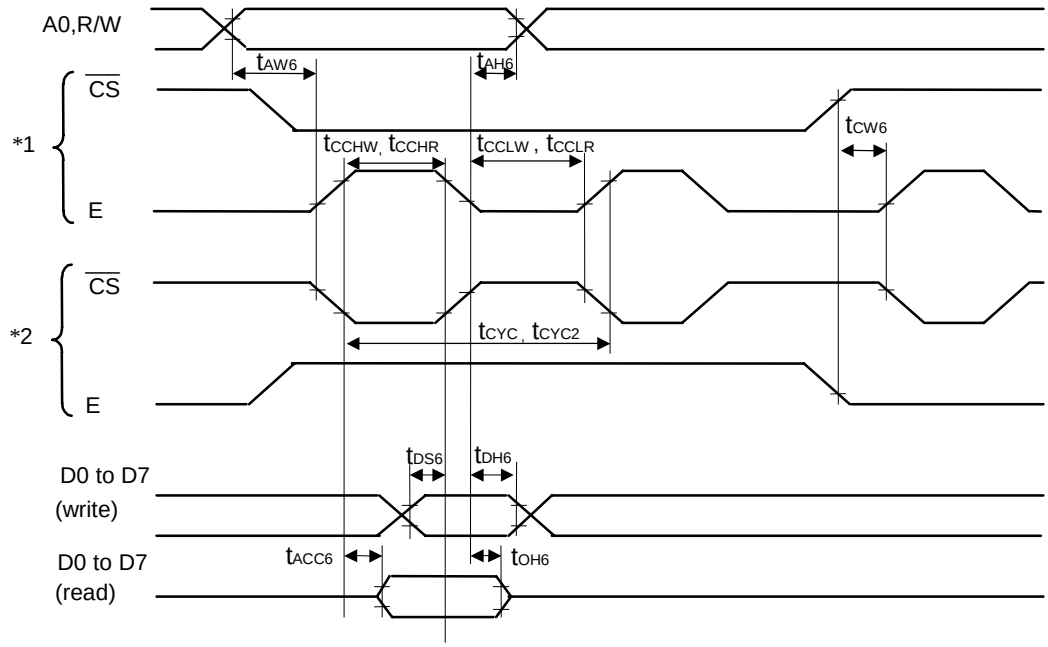
Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 10ns.
Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

V_{DD} = 2.35 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		110	—	ns
Serial clock HIGH pulse width		t_{SHW}	—	50	—	
Serial clock LOW pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}	—	120	—	
Address hold time		t_{SAH}		30	—	
Data setup time	SIO	t_{SDS}	—	25	—	
Data hold time		t_{SDH}		25	—	
Data delay time (Hz-data)	SIO	t_{ACC}	C_L=30pF	—	120	
			C_L=100pF (reference)	—	180	
Data delay time (data-Hz)		t_{OH}	C_L=30pF	15	—	
			C_L=100pF (reference)	25	—	
$\overline{CS}$ serial clock time	$\overline{CS}$	t_{CSS}		50	—	
		t_{CSH}	—	50	—	
		t_{CSHW}		50	—	

Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 10ns.
Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

12.3 68 Series Parallel Interface



*1 shows an access with E when $\overline{CS}$ is LOW. *2 shows an access with $\overline{CS}$ when E is HIGH.

V_{DD} = 2.6 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,R/W	t_{AH6}	—	10	—	ns
Address setup time		t_{AW6}		3	—	
Write cycle	E, $\overline{CS}$	t_{CYC}		190	—	
Read cycle		t_{CYC2}		250	—	
Control pulse LOW width (write)		t_{CCLW}		140	—	
Control pulse LOW width (read)		t_{CCLR}	—	70	—	
Control pulse HIGH width (write)		t_{CCHW}		40	—	
Control pulse HIGH width (read)		t_{CCHR}		170	—	
$\overline{CS}$-E time		t_{CW6}		5	—	
Data setup time	D0 to D7	t_{DS6}	—	10	—	
Data hold time		t_{DH6}		20	—	
Read access time		t_{ACC6}	C_L=100pF	—	200	
Output disables time		t_{OH6}		5	60	

Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 10ns.
Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

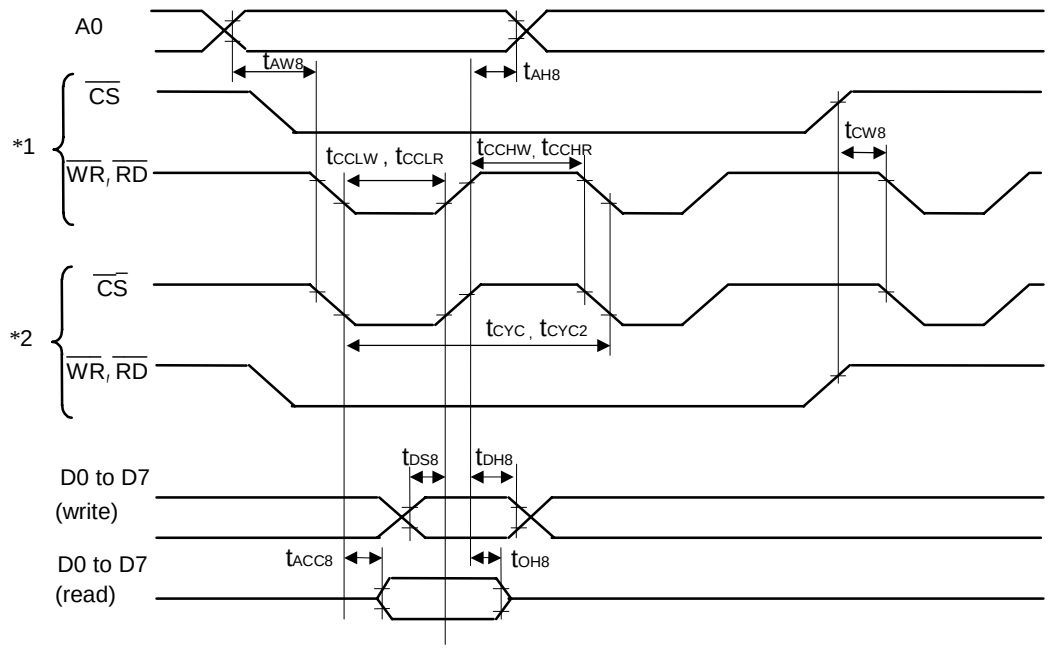
V_{DD} = 2.35 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,R/W	t_{AH6}	—	15	—	ns
Address setup time		t_{AW6}		5	—	
Write cycle	E, $\overline{CS}$	t_{CYC}		250	—	
Read cycle		t_{CYC2}		300	—	
Control pulse LOW width (write)		t_{CCLW}		170	—	
Control pulse LOW width (read)		t_{CCLR}	—	80	—	
Control pulse HIGH width (write)		t_{CCHW}		70	—	
Control pulse HIGH width (read)		t_{CCHR}		200	—	
$\overline{CS}$-E time		t_{CW6}		10	—	
Data setup time	D0 to D7	t_{DS6}	—	15	—	
Data hold time		t_{DH6}		25	—	
Read access time		t_{ACC6}	C_L=100pF	—	250	
Output disables time		t_{OH6}		10	70	

Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 10ns.

Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

12.4 80 Series Parallel Interface



*1 shows an access with $\overline{WR}$ and $\overline{RD}$ when $\overline{CS}$ is LOW. *2 shows an access with $\overline{CS}$ when $\overline{WR}$ and $\overline{RD}$ are LOW.

V_{DD} = 2.6 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}	—	10	—	ns
Address setup time		t_{AW8}		3	—	
Write cycle	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	t_{CYC}	—	180	—	
Read cycle		t_{CYC2}		280	—	
Control pulse LOW width (write)		t_{CCHW}		140	—	
Control pulse LOW width (read)		t_{CCHR}		70	—	
Control pulse HIGH width (write)		t_{CCLW}		40	—	
Control pulse HIGH width (read)		t_{CCLR}		200	—	
$\overline{CS}$-$\overline{WR}$, $\overline{RD}$ time		t_{CW8}		5	—	
Data setup time	D0 to D7	t_{DS8}	—	10	—	
Data hold time		t_{DH8}		20	—	
Read access time		t_{ACC8}	C_L=100pF	—	200	
Output disables time		t_{OH8}		5	60	

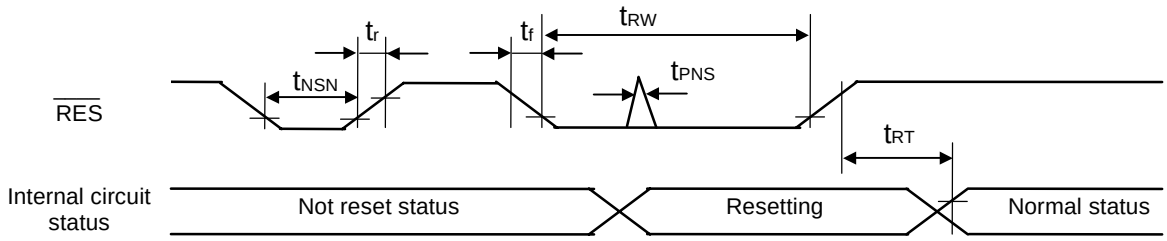
Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 10ns.
Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

V_{DD} = 2.35 to 3.6V, V_{DDI} = 1.6 to V_{DD}, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}	—	15	—	ns
Address setup time		t_{AW8}		5	—	
Write cycle	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	t_{CYC}	—	250	—	
Read cycle		t_{CYC2}		300	—	
Control pulse LOW width (write)		t_{CCHW}		170	—	
Control pulse LOW width (read)		t_{CCHR}		80	—	
Control pulse HIGH width (write)		t_{CCLW}		70	—	
Control pulse HIGH width (read)		t_{CCLR}		200	—	
$\overline{CS}$-$\overline{WR}$, $\overline{RD}$ time		t_{CW8}		10	—	
Data setup time	D0 to D7	t_{DS8}	—	15	—	
Data hold time		t_{DH8}		25	—	
Read access time		t_{ACC8}	C_L=100pF	—	250	
Output disables time		t_{OH8}		10	70	

Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 10ns.
Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

Reset Timing



V_{DD} = 2.6 to 2.9V, V_{DDI} = 1.6 to 2.0V, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Reset time	$\overline{RES}$	t_{RW}	—	3000	—	ns
Reset clear time		t_{RT}	—	—	500	
Insensible pulse width in negative direction		t_{NSN}	—	—	500	
Insensible pulse width in positive direction		t_{PNS}	—	—	10	
Rise and fall time		t_r, t_f	—	—	15	

V_{DD} = 2.35 to 3.6V, V_{DDI} = 1.6 to 2.0V, T_a = -40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Reset time	$\overline{RES}$	t_{RW}	—	5000	—	ns
Reset clear time		t_{RT}	—	—	1000	
Insensible pulse width in negative direction		t_{NSN}	—	—	100	
Insensible pulse width in positive direction		t_{PNS}	—	—	5	
Rise and fall time		t_r, t_f	—	—	15	

Note1 The input signal rise time and fall time (t_r, t_f) are specified less than 15ns.

Note2 All timing signals are specified on the basis of 30% and 70% of V_{DDI}.

Note3 The reset time's minimum reference value indicates that at least 3000ns is required to initialize the S1D15G14.

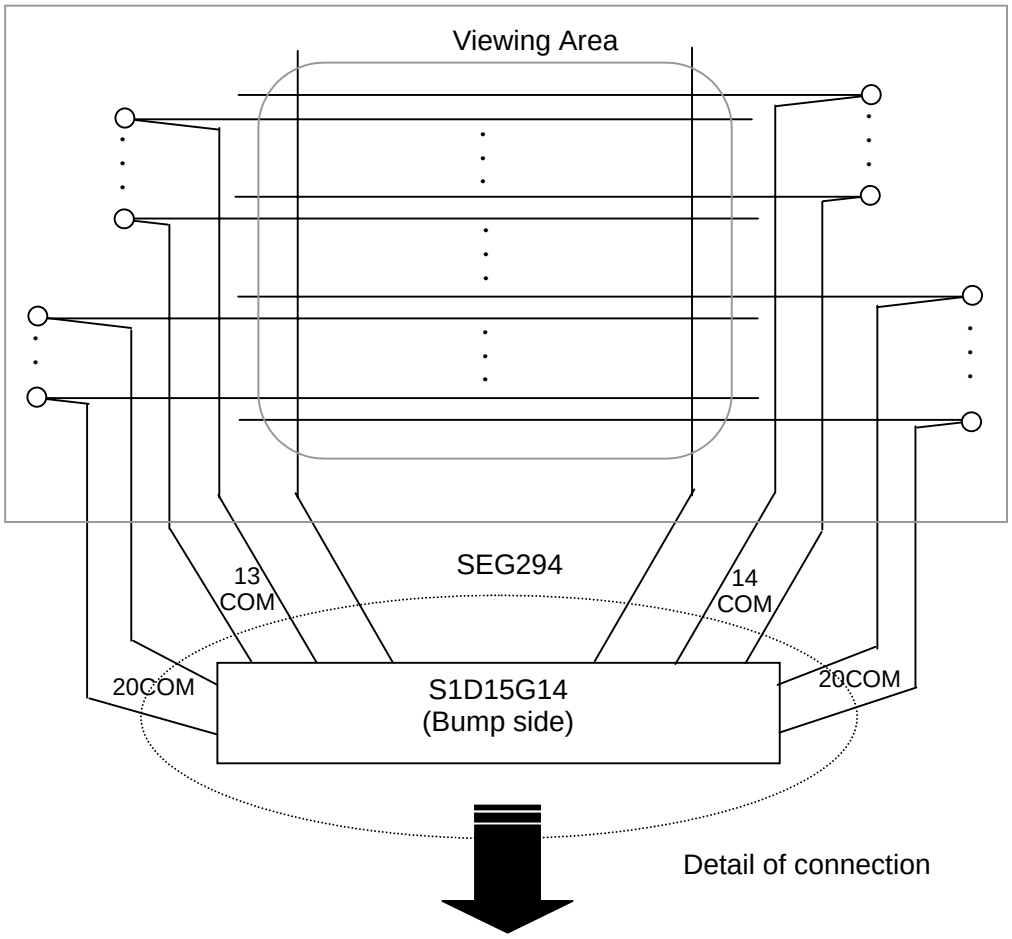
Note4 The maximum reference value of the insensible pulse width (in the positive direction) indicates that the S1D15G14 can maintain its reset status without any reaction even if there is a pulse of 10ns inputted to its RES pin (because of static electricity, etc).

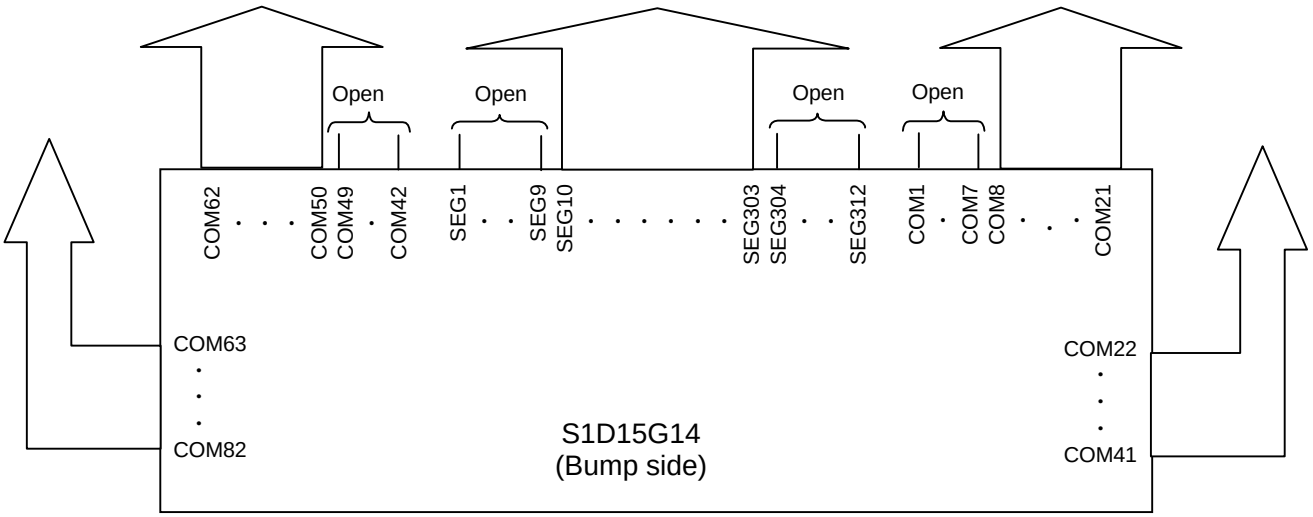
Note5 The maximum reference value of the insensible pulse width (in the negative direction) indicates that the S1D15G14 can maintain its operating status without any reaction even if there is a pulse of 500ns inputted to its RES pin (because of static electricity, etc).

13. CONNECTION BETWEEN LCD PANELS

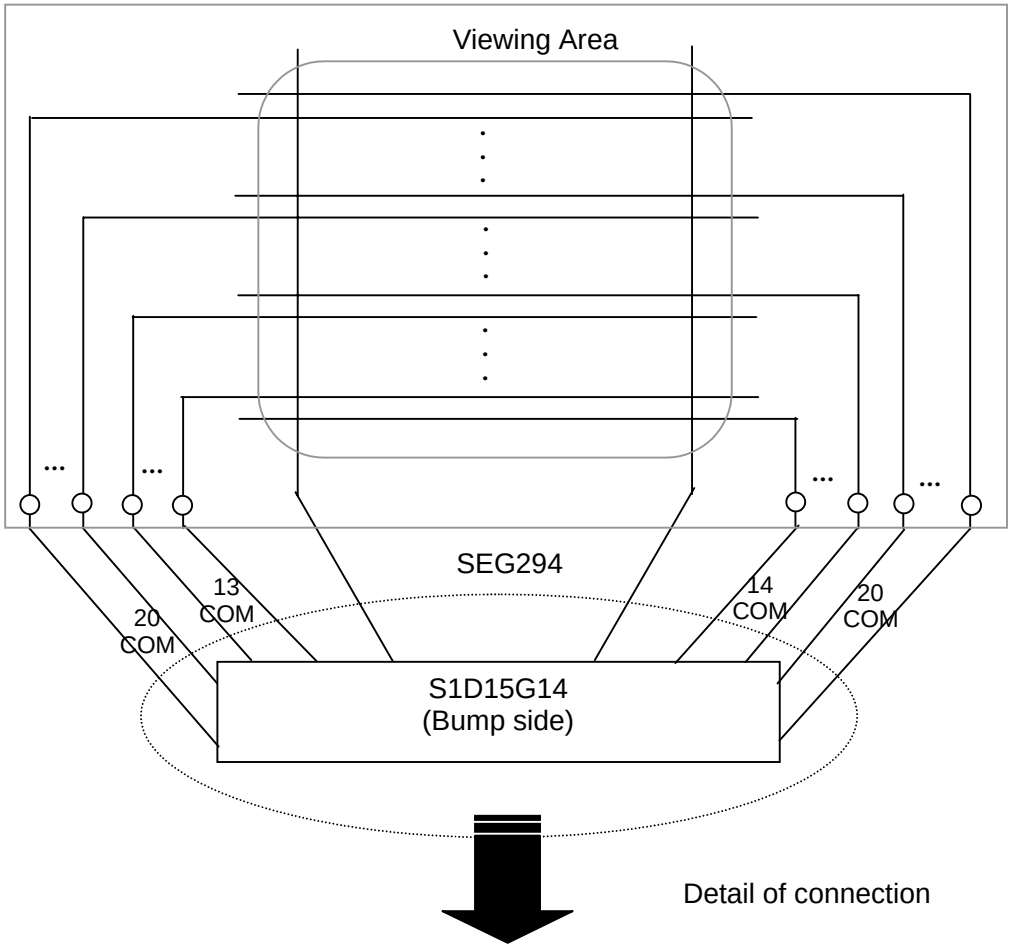
Panel size: 98RGB×67

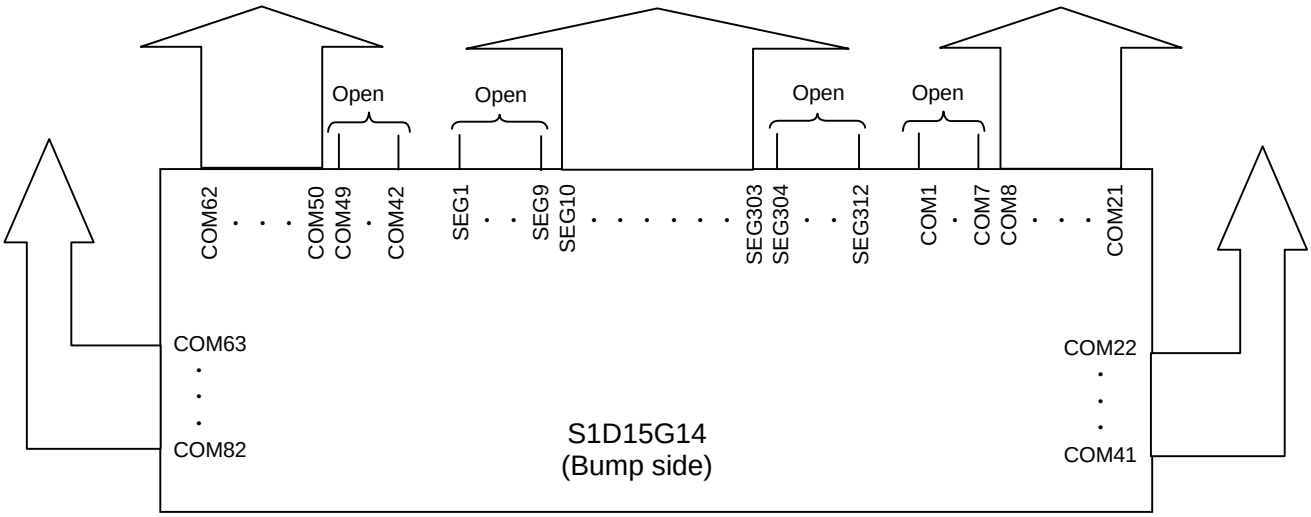
When through holes are arranged between the upper and lower glasses on the both sides of the panel,



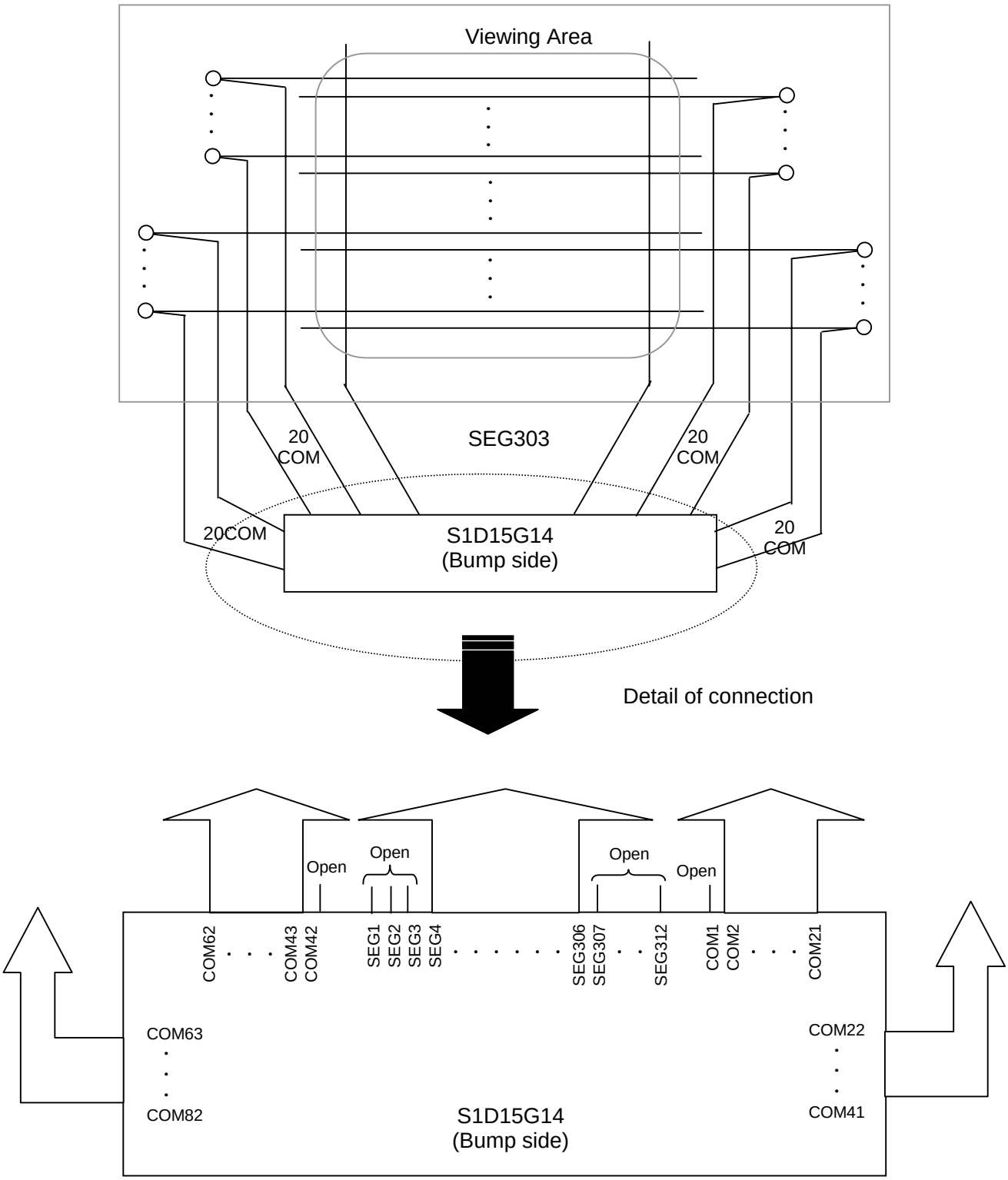


Panel size: 98RGB×67
When through holes are arranged between the upper and lower glasses on the both sides of the panel,

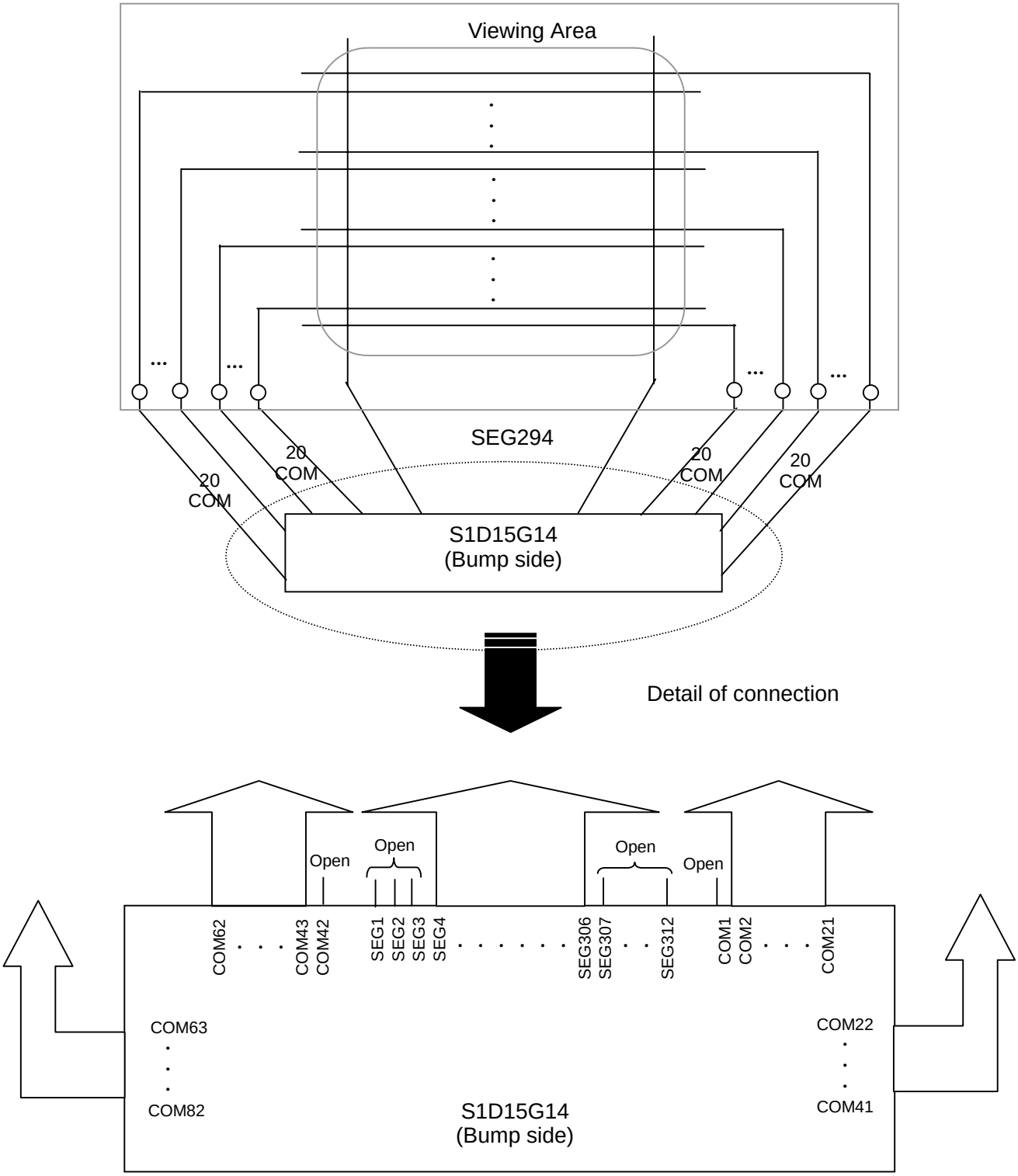




Panel size: 101RGB×80
When through holes are arranged between the upper and lower glasses on the lower side of the panel,

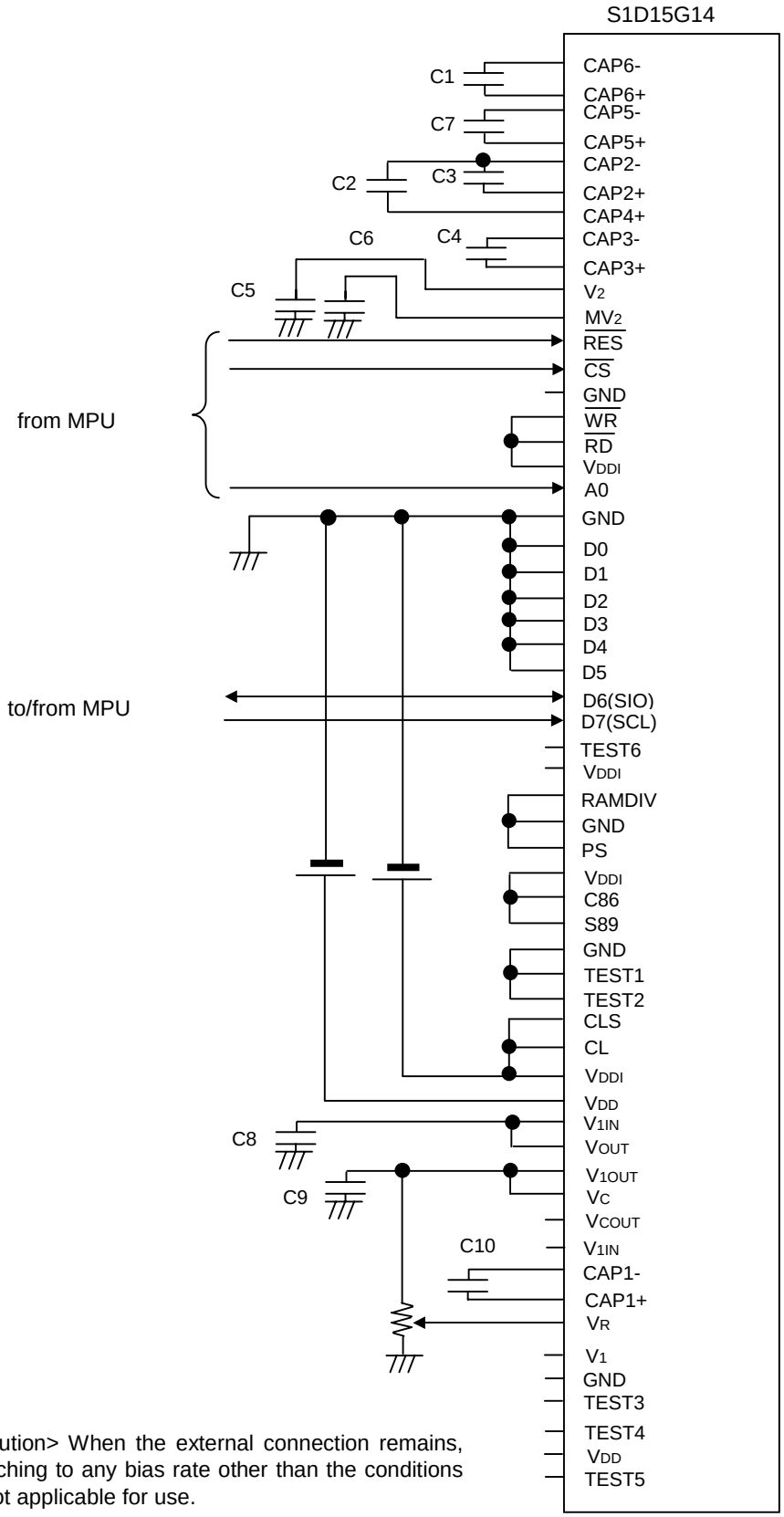


Panel size: 101RGB×80
When through holes are arranged between the upper and lower glasses on the lower side of the panel,



14. EXAMPLE EXTERNAL CONNECTION

1/9bias, 102RGB×82outputs are available.
8bits serial interface with Variable Resister.



Maximum volatage of Capacitors

C1: 9.8V
C2: 2.8V
C3: 2×2.8=5.6V
C4: 2.5×2.8=7.0V
C5: 4.5×2.8=12.6V
C6: 3.5×2.8=9.8V
C7: 3.5×2.8=9.8V
C8: 2.8V
C9: 1.4V
C10: 2.8V

Due to restriction of IC withstand voltage ($V_2 \leq 15V$, $MV_2 \geq -10V$), the V_{OUT} voltage is limited to below 2.8V.

Capacitors are used for the following purposes:

C1: For boosting V_2.
C2: For boosting MV_2.
C3: For boosting MV_2.
C4: For boosting MV_2.
C5: For smoothing V_2.
C6: For smoothing MV_2.
C7: For boosting MV_2.
C8: For smoothing V_1.
C9: For smoothing V_C.
C10: For boosting V_1.

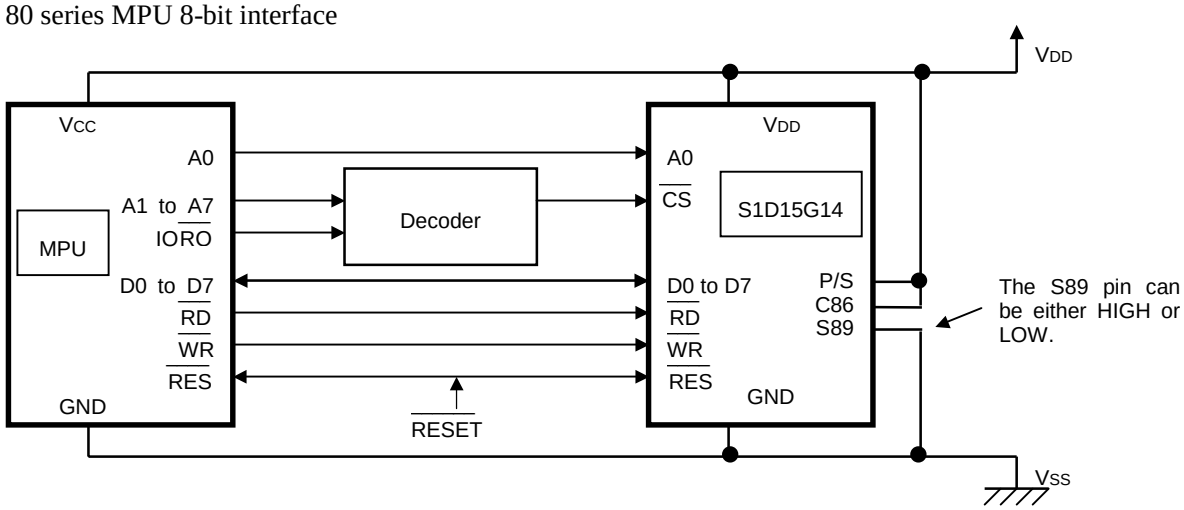
<Caution> When the external connection remains, switching to any bias rate other than the conditions is not applicable for use.

15. MPU INTERFACE

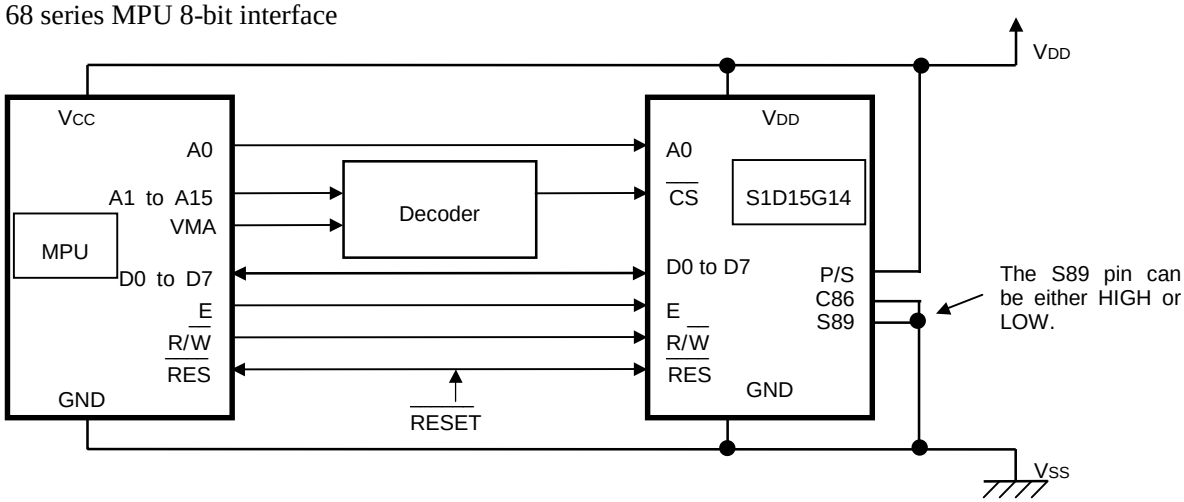
15.1 Examples of MPU interface connections

The S1D15G14 can be connected to the 80 series MPU and 68 series MPU. Use of the serial interface allows operation with fewer signal lines. In addition to the following (1), (2) and (3), connection with the 8-bit serial interface is possible.

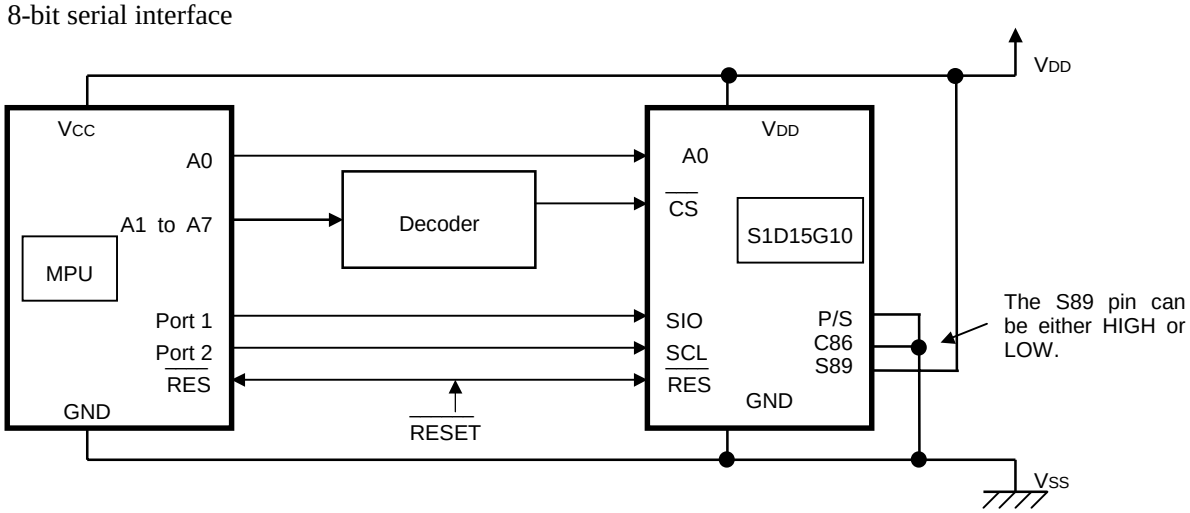
(1) 80 series MPU 8-bit interface



(2) 68 series MPU 8-bit interface



(3) 8-bit serial interface



15.2 Examples of software setup

Examples of Software setup are shown below. For commands whose default values after reset can be used without any change, the command input is not necessary in the following examples.

(1) Command input procedure for turning on the power
input the V_{DD} and V_{DDI}.
↓
Be sure to execute the power-on reset. ($\overline{RES}$ = LOW)
↓
Set the $\overline{RES}$ to be HIGH, and wait for 5 ms (internal operation stabilizing time)
↓
Software reset (01h) : Start the reset operation for the settings inside the IC.
↓
Wait for 5ms
↓
INIESC (C6h) : Initialize the settings inside the IC.
↓

<Display setup 1>

- REFSET(B9H)
  Set the states inside the IC.
- Display control (B6H)
  Set the 1H term, number of N-line reversion, idle mode frequency, LCD bias, RAM size, Display duty
- Gray scale position set (B3H,B4H)
  Set the gray scale specifications.
- Gamma curve set (B5H)
  Select the gray scale
- Common driver output select (BDH)
  Set the output position and sequence of the common driver outputs.

(The order of settings from Display control (B6H) to Common driver output select (BDH) can be changed)

<Power supply setup>

- Power control (BEH)
  Set the V_{1OUT} output drive capability, operating frequency of the built-in boosting circuit.
- Sleep out (11H)
  Built-in oscillation circuit operation
- Voltage control (BAH)
- Write contrast (25H)
  Set the LCD voltage.
- Temperature gradient set (B7H)
  Set the temperature gradient of the LCD voltage.
- Booster voltage ON (03H)
  Built-in power supply circuit operation

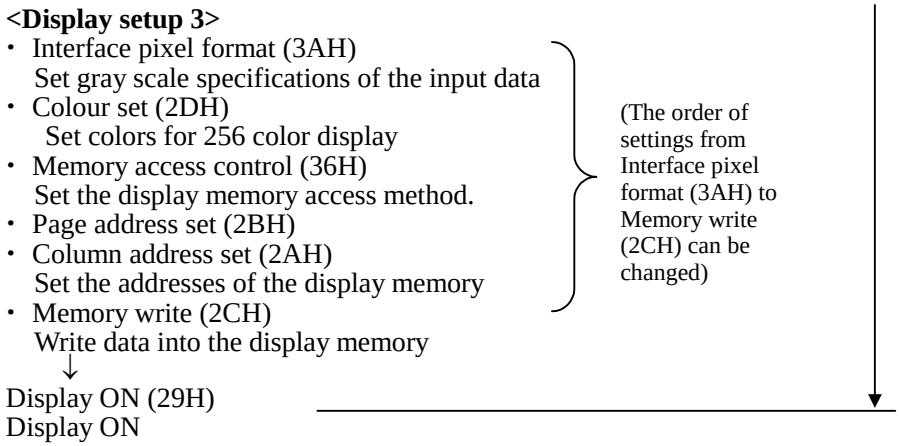
(The order of settings from Power control (BEH) to booster voltage ON (03H) can be changed)

<Display setup 2>

- Inversion ON (21H) or Inversion OFF (20H)
  Inversion/normal of display
- Partial area (30H)
  Set the partial display area.
- Vertical scroll definition (33H)
  Set the vertical scrolling specifications.
- Vertical scrolling start address (37H)
  Set the address of the vertical scrolling.

(The order of settings from Inversion ON(21H) or Inversion OFF (21H) to Vertical scrolling start address (37H) can be changed)

Power stabilization time as long as 40 ms or more must be secured from Booster voltage ON (03H) to Display ON (29H)



(2) Command input procedure for turning OFF the power
① When the $\overline{RES}$ signal is not used.

Display OFF (28H) : Display OFF
↓
Sleep in (10H) : Sleep in
↓
Turn OFF the V_{DD}-V_{DDI} power.

Note: In order to discharge the electric charge in capacitors connected to the LCD power supply circuit, execute the Sleep in command to set the IC to be in sleep state before turning of the power. When the output of the LCD power supply circuit becomes low enough, turn OFF the V_{DD}-V_{DDI} power.

② When the $\overline{RES}$ signal is used.

Execute the power ON reset ($\overline{RES}$ = LOW)
↓
Turn OFF the V_{DD}-V_{DDI} power.

Note: Turn OFF the V_{DD}-V_{DDI} power when the output of the LCD power supply circuit becomes low enough.

This IC uses the logic voltage of the V_{DD}-GND and V_{DDI}-GND power supply for control of the LCD output driver. Thus, if the power supply V_{DD}-GND, V_{DDI}-GND is turned OFF while voltage is still remaining on the LCD power supply circuit, the LCD output drivers (COM,SEG) can generate uncontrolled output. When the output of the LCD power supply circuit becomes low enough, turn OFF the V_{DD}-V_{DDI} power.

16. PRECAUTIONS

Pay attention to the following concerning the development specification:
1. The development specification is subject to change for improvement without advance notice.
2. The development specification does not guarantee to use industrial property right and other rights and does not provide any patent right.

Applied examples shown in the development specification are intended to help you understand the product, and the manufacturer shall not be responsible for any trouble arising from using such applied examples.

In operation of S1D15G14, pay attention to the following:

"Precautions on Light"

Properties of semiconductor devices are generally affected according to the principle of solar battery when they are exposed to light. Therefore, this IC may malfunction if exposed to light.

① When using this IC, design the structures of devices or mount the IC so that it is shielded from light.
② Design the structure of inspection process or mount the IC so that it is shielded from light.
③ Protect surfaces, rears and sides of IC chips from light.

However, reliability of the IC is not affected for a long time even if it is operated under slight light where it does not malfunction and their characteristics including current consumption are not influenced.

"Precautions on External Noise"

① Operating statuses of and display data in S1D15G14 are maintained by commands, but excessive external noises may affect its internal statuses. Take proper measures in mounting and arranging systems so that they can protected from external noises.
② We recommend you to assemble software so that the operating status can be periodically refreshed (by resetting commands and by re-transferring display data) against noises arising suddenly.

"Precautions on COG"

When mounting COG, you should consider resistance components caused by ITO wire between driver chips and external parts to be connected (capacitor, resister, etc.). These resistance components may cause troubles in LCD display and in high-speed operation of the MPU interface.

When mounting COG, design modules paying sufficient attention to the following three points:
1. Reduce resistances from driver chip pins to external parts as much as possible.
2. Reduce resistance in the power supply pins of the driver chips as much as possible.
3. Prepare a COG module sample by changing ITO sheet resistance, and use such a module with sheet resistance allowing sufficient operation margin.

Appendix-1

Revision History of Development Specification S1D15G14

Y/M/D Rev. No.	Page No.(Rev.)	Contents of revision
2002/06/05 Rev.0.1	All pages	New edition
2002/06/18 Rev.0.2	All pages	Revisions for correcting mistakes and adding explanations P2: 13. MPU Interface was added in the Contents. P3: Target value of consumption current was added to the Overview. P13: Errors in writing D7(SCL) and D6(SIO) were corrected. P22: Correction of errors in writing pin names: $V_C \rightarrow V_{COUT}$, $V_{CIN} \rightarrow V_C$ Revision of confusing description: Parts composition is minimized. → The step-up capacitor is not necessary. P23: Correction of error in writing pin name: $V_{CIN} \rightarrow V_C$ P24: Correction of error in writing pin name: $V_{OUT1} \rightarrow V_{1OUT}$ Error in writing Electronic Volume Function was corrected. P25: Correction of error in writing pin name: $V_{OUT1} \rightarrow V_{1OUT}$ P26: Correction of error in writing pin name: $V_{CIN} \rightarrow V_C$ P28: Correction of error in writing pin name: $V_{CIN} \rightarrow V_C$ P29: Addition of explanations. Addition of Setting Method of respective selection periods of Normal Mode and Idle Mode. P31: Addition of explanation concerning ON/OFF reset sequence. P32 to 59: Addition of explanation concerning command default statuses. P32: Correction of errors in writing non-operation command functions. "To go through the test mode for inspecting IC" → Deleted. P35: Correction of errors in writing RDDST B28. Functions of 1 and 0 were reversed. P39: Correction of errors in writing All Pixels Off Command. ON → OFF P40: Correction of errors in writing WRCNTR Command. Optimum contrast → Center value. P44: Correction of typing mistake of RAM data read Command. P47: Correction of errors in writing MADCTL Command B5 function. 1 and 0 had been reversed. P50: Change of TSTMOD Command function By NOP Command → By NOP2 Command P50: Addition of NOP2 Command function "To go through the test mode for inspecting IC" was added. P55: Addition of REFSET Command P55: Addition of explanation concerning VOLCTL Command. P56: Addition of explanation concerning COMOUT Command. Combinations of P10 to P13 were illustrated. The drawing of normal drive was inserted. P56 to P59: Addition of explanation The connection diagram of normal drive was added. P60: Change of PWRCTL Command. Change of division clock. P62: Correction of errors in writing f_{osc2} of DC characteristics (Clock count) → (Dividing ratio) Correction of errors in writing reference voltage V_{REG} 1.5V → 1.8V P64, P65: Addition of stipulation concerning Serial AC Timing Load Capacity. P66, P67: Addition of Parallel AC Timing Target Specification P68: Addition of explanations concerning Reset AC Timing, Negative Dead Pulse Width and Positive Dead Pulse Width P73 to P76: Addition of connection example with panel in normal drive. P78 to P80: Addition of explanation concerning MPU Interface.

Appendix-2

Revision History of Development Specification S1D15G14

Y/M/D Rev. No.	Page No.(Rev.)	Contents of revision
2002/10/19 Rev.1.0	All pages	Revision for changing specifications and adding explanations. P1: Model name: S1D15G14D00B000 → S1D15G14D01B000 due to change of specification. P2: Expansion of operating supply voltage range and entry of current consumption P11: Entry of precautions concerning pin. P12: Addition of explanation concerning Set-up Pin. P20, P21: The serial interface timing was changed from 8 bits to 9 bits. P22 to P31: Change of specification of and addition of explanation concerning Power Circuit. P35 to P61: Change of specification and addition of explanation concerning commands. P63: DC characteristics Addition of description concerning Operating Current Consumption and Power Supply Impedance. Correction of errors in writing oscillating frequency. The power supply operating voltage range was changed from 2.6V~ to 2.35V~. P65 to P72: AC characteristics Review of standard values so as to match each device. Addition of characteristic V_{DD}=2.35V~
2002/11/12 Rev.1.1	All pages	Revision for changing specifications and adding explanations. No. P5: Addition of explanation Chip thickness, Bump height (Reference) → (Reference value. For the detail, refer to the Delivery Specification.) No. P16, No. P17: Correction of errors in writing memory map. SEG pin position was reversed. No. P23: Correction of error in writing V_{COUT} connection at the time of external resistance. Variable resistor → Open. No. P37: Correction of error "B14 Horizontal scrolling on/off" was deleted. No. P41: Correction of error This °C → This command. No. P47: Addition of explanation. PLTAR Command default value was added. No. P50: Addition of explanation. MADCTL Command Addition of drawing showing correspondence with packaging pattern. No. P53: Correction of error in writing Test Mode. "To go through the Test Mode by the NOP Command" → "… by NOP or NOP2 Command." No. P55: Correction of error in writing DISCTL Command. Addition of explanation "The set value brings an invert cycle." to Setting of Parameters for N Line Inversion. No. P56: Addition of explanation concerning DISCTL Command. Addition of explanation "Basically, P32="0" is recommended for use." Addition of explanation concerning Duty Setting. No. P59 to P60: Correction of error in writing COMOUT Command. ② When the DISCTL Command was used to set to 1/82 duty, 0/1 of P13 were reversed for P13=1, P12=1 and B4=0. No. P63: Correction of error in writing DC characteristics Unit of LCD ON resistance KΩ → Ω No. P68 to P71: Change of specification, AC Characteristics of parallel interface t_{CW} 40ns → 5ns V_{DD}=2.6 to 3.6V 50ns → 5ns V_{DD}=2.35 to 3.6V No. P72: Correction of error in writing. Reset cancel time for V_{DD}=2.35 to 3.6V 100ns → 1000ns Addition of explanation. Addition of stipulation concerning tr and tf in Timing Chart. No. P77: Addition of explanation. Addition of purposes to use capacitors in External Connection Diagram.

Appendix-3

Revision History of Development Specification S1D15G14

Y/M/D Rev. No.	Page No.(Rev.)	Contents of revision
2002/11/27 Rev.1.2	All pages	Revision for changing specifications and adding explanations. No. P33: Change of specification C6h TEST mode → Initial escape No. P36: Addition of explanation Add the timing of parallel interface to the RDDST command. No. P48: Correction of error in writing Binary command code 01100000 → 00110100 No. P53: Change of specification TEST mode → Initial escape command No. P54: Correction of error in writing Binary command code 10110011 → 10110111 No. P63: Addition of explanation Add Operating current consumption (3) for idle mode. No. P79, No. P80: Change of specification Change the initialization sequence.
2003/3/14 Rev.1.2a	All pages	No. P1: Delete of explanation etc(programable) No. P2: Correction of error LCD → LCD power circuit genetrator → generator No. P9: Correction of error 86MPU interface → 80MPU interface No. P23: Correction of error 1.8V → 1.5V Add of explanation “Please be careful for the set-up value not to exceed operation voltage” No. P29: Correction of error Operation and Stop at Idle Mode are replaced. No. P55: Change of description “Do not rewrite...” → “Do not change...” “Other parameter may be...” → “Other parameters should...” “P1” → “P11”, “P0” → “P10” Add of explanation “Please keep in mind...” No. P75: Correction of error “C7, C8, C9” → “C8, C9, C10”

Appendix-4

Revision History of Development Specification S1D15G14

Y/M/D Rev. No.	Page No.(Rev.)	Contents of revision
2003/4/23 Rev.1.3	All pages	Addition of D2B slice and explanations and change in specification No.2: Addition and correction of the model list page; correction of chapter number beyond Chapter 6. No. P3: Change of reference for die No. No. P7: For page insertion No. P8: Addition of model list No. P24: Change of voltage control command parameter value 63 → 127 No. P32: Division of the command list table into 2 parts No. P32: Division of the command list table into 2 parts No. P33: Addition of command process time and execution time No. P34: Addition of command process time and execution time No. P44: Correction of error SC → SP, EC → EP No. P50: Addition of comment No. P53: Change of TEST mode value (32) 70 → DE No. P57: Addition of restrictions on the DISCTL command No. P63: Addition of comment Change of value Example: 840k/82/64=160 → 840k/82/128=80 No. P65: Timing change in serial interface No. P66: Timing change in serial interface No. P65, P66, P68, P70: Correction of error V_{DD} ... to 3.3V → to 3.6V
2003/5/12 Rev.1.4	All pages	No. P1: Change of power supply value $V_2 – MV_2$ = 10.0V to 25V → 10.0V to 25.5V Correction of error No. P24: Correction of error 1.5 → 1.8V No. P63: Change of value V_{REG} 1.46 → 1.75, 1.5 → 1.8, 1.54 → 1.85 Min of MV_2 -10→ -10.5