ECE 370: Digital Systems-Logic Design

Sample Test: Chapter 7-Part 3: Counters
Spring 2005

Understanding Counters

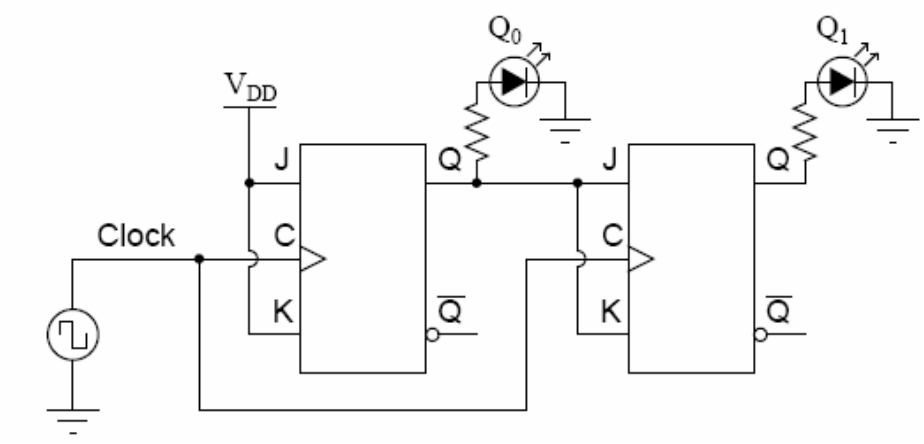
1. Answer the following questions.
   (a). Describe the general form of an asynchronous counter. Which Flip-Flops make the design of asynchronous counters easy?
   (b). How many Flip Flops are needed to design a modulo-*n* counter? Up to what value does a modulo-*n* counter count to? Derive an equation that relates the modulus to the number of Flip-Flops used.
   (c) What does it mean for a counter to recycle?
   (d) What is a UP counter? What is a DOWN counter?

Asynchronous (Ripple) Counters

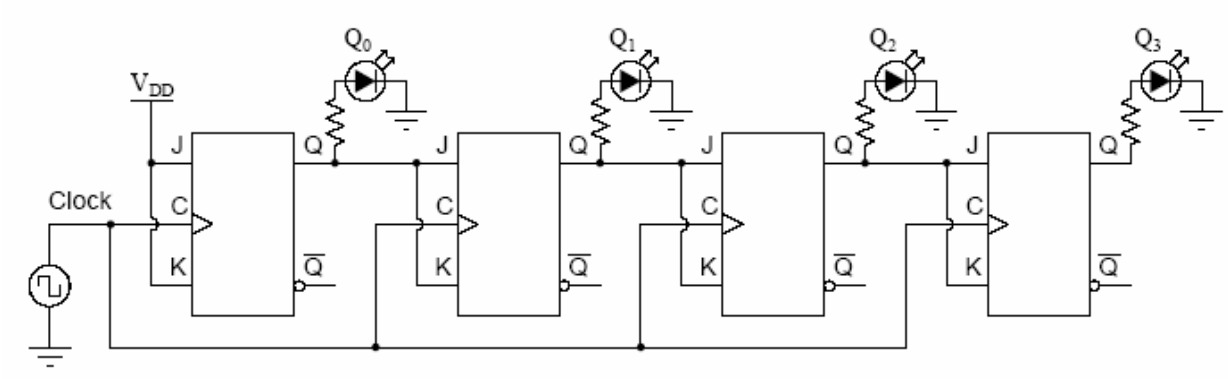
2. Show the schematic of a modulo 8 counter using J-K Flip-Flops. Repeat the design using T Flip-Flops. Verify each design by drawing out waveforms for each input and output to the counter.
3. Design a modulo 6 counter using T Flip-Flops. Repeat the design using D-Flip-Flops. Verify each design by drawing out waveforms for each input and output to the counter.
4. Design a modulo 20 counter using J-K Flip Flops that detects the following counts. 4, 8, and 17.
5. Given a 200 MHz clock signal, design a circuit that produces a 100 MHz clock signal, a 50 MHz clock signal, a 25 MHz clock signal, and a 12.5 MHz clock signal. Design your system using D-Flip Flops.
6. Design a 4-bit ripple counter with a control input $DOWN/\overline{UP}$ that controls the counters count sequence. If the control input is asserted, then the counter is an UP counter. Otherwise, the counter should be a DOWN counter. Create two different designs for this circuit using T-Flip-Flops. *Hint: Think back on how we designed a 2's complement adder/subtractor two different ways.*

Synchronous Counters

7. A student just learned how a *2-bit* synchronous binary counter works, and he/she is excited about building his/her own. He/she does so, and it works perfectly.



Then, the student tried to expand on his/her success by adding more flip-flops, following the same pattern as the original *2-bit* synchronous counter. Was the student successful in his/her new design? Analyze the circuit below to find out!



8. By now, you should have noticed the above student was not successful. However, you decide to help, but realize that you are also not well informed about synchronous counter design. You decide to draw the tables below showing 2, 3, and 4-bit counting sequences in order to help your knowledge of synchronous counter design. After careful exception and analysis of the tables below, answer the following questions.

   (a) Design a *2-bit*, *3-bit*, and *4-bit* synchronous counter using J-K Flip-Flops.
   Hint: Examine when Q_{i+1} is related to Q_i in terms of when Q_{i+1} "toggles."

   (b) Your task now is to explain your findings to the student based on part (a) above. Use the structures of the three counters to generalize the design of an *n-bit* synchronous counter using J-K Flip-Flops and explain to the student how you came up with your findings.

   (c) If using T Flip-Flops to design the above synchronous counters, derive a general expression for the T_i in terms of all of the *present state* outputs. For example, $T_0 = 1$ since Q_0 always toggles.

(d) Using the equations from part (c) from above, re-write the equations assuming D Flip-Flops are used to design the synchronous counters instead. *Hint: Use the characteristic equations of the T and D Flip-Flops to aid in your derivation.*

Q_1	0	0	1	1
Q_0	0	1	0	1

Q_2	0	0	0	0	1	1	1	1
Q_1	0	0	1	1	0	0	1	1
Q_0	0	1	0	1	0	1	0	1

Q_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Q_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Q_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Q_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

9. Using the knowledge gained from Problem 7, design a synchronous BCD counter that drives a BCD-to-7-segment display decoder using T-Flip-Flops. Show the schematic of your design.

General Synchronous Counter Design

10. Design a modulo-3 binary counter using D Flip-Flops. Show the State Graph, State Table, and the final schematic in your design. Verify your design performing a timing analysis of your design.

11. Design a counter that counts in the sequence shown below using J-K Flip-Flops. Show the State Graph, State Table, and final schematic of your design. Verify your design performing a timing analysis of your design.

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{0,2,1,4,3,6,5,8,7,0...}
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Gray code is another type of binary code. Below is a table of a 3-bit Gray Code count and its corresponding value in binary and decimal. Use the table to answer the following two questions.

Dec	Binary	Gray Code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

12. (a) Draw a State-Graph for a 3-bit gray code counter.
(b) Draw a Stage-Table for the 3-bit Gray code counter
(c) Design the gray code counter using T Flip-Flops.

13. Design 3-*bit* counter that has an input called $GRAY / \overline{BINARY}$. When input $GRAY / \overline{BINARY}$ is low, the counter counts in a normal binary sequence. When input $GRAY / \overline{BINARY}$ is high, the counter counts in Gray Code. Show a State-Graph, State Table, and the final schematic of your design.

14. Design a synchronous counter with a control input *Y*. The following describes how the counter behaves based on input *Y*.
    - If *Y = 1*, then the counter is an UP counter.
    - If Y = *0*, then the operation of the counter is determined by the current state.
        - If the current state is an even state, the counter stops counting,
        - If the current state is an odd state, the counter counts by 2.

Counter Applications

15. Parallel data is data that appears all at once on *n* input lines. Serial data is data that appears one at a time using 1 input line. Therefore, to transmit parallel *n-bit* data, it takes only 1 clock cycle. To transmit *n-bit* data serially, it takes *n clock cycles*, since after each clock cycle, *1-bit* of data is transmitted. Sometimes in digital systems, parallel data needs to be converted into serial data. Use a *3-bit* synchronous counter to convert 8-bit parallel data to serial data that can be transmitted 1-bit at a time at each clock edge. *Hint: Use the most important topics from Chapter 6 to aid in your design.*