ECE 370: Digital Systems-Logic Design

Sample Test: Chapter 7-Part 1: Flip Flops
Spring 2005

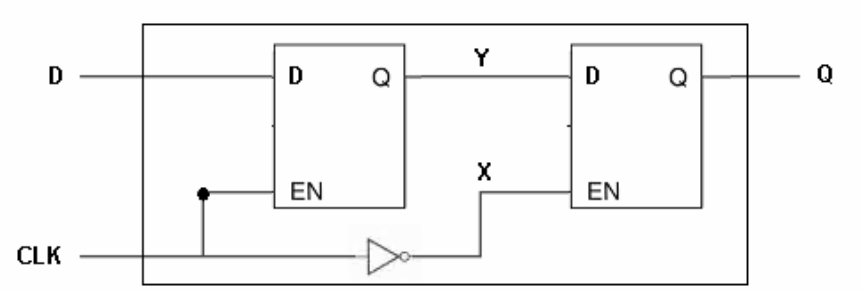
Flip-Flops vs. Latches

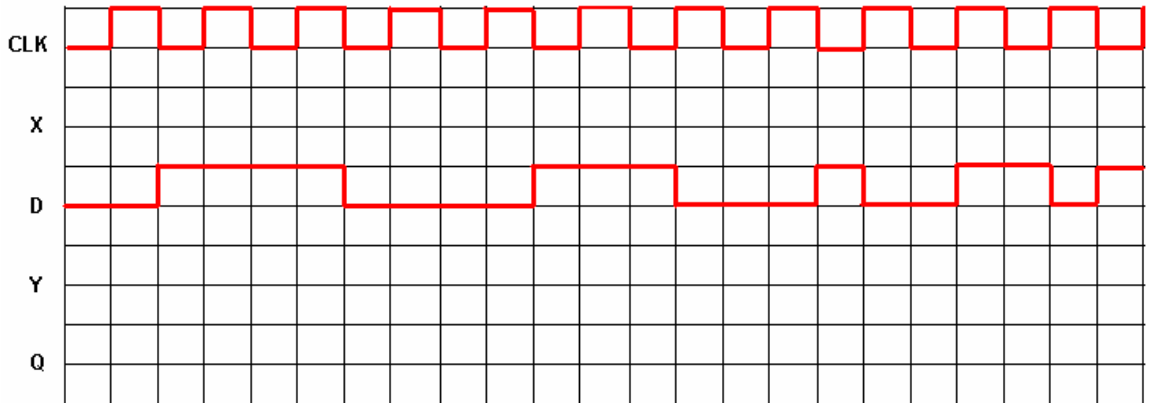
1. What is the main goal for using latches and/or flip-flops?

2. What kind of improvements, if any, do flip-flops offer over gated latches?

3. What is the difference between a positive-edge triggered flip-flop and a negative edge-triggered flip-flop? How does this differ from a gated latch?

4. Given the following configuration of transparent (Data) **Latches** and input waveforms, draw the output waveforms and comment on how this configuration effects the operation of the whole system?



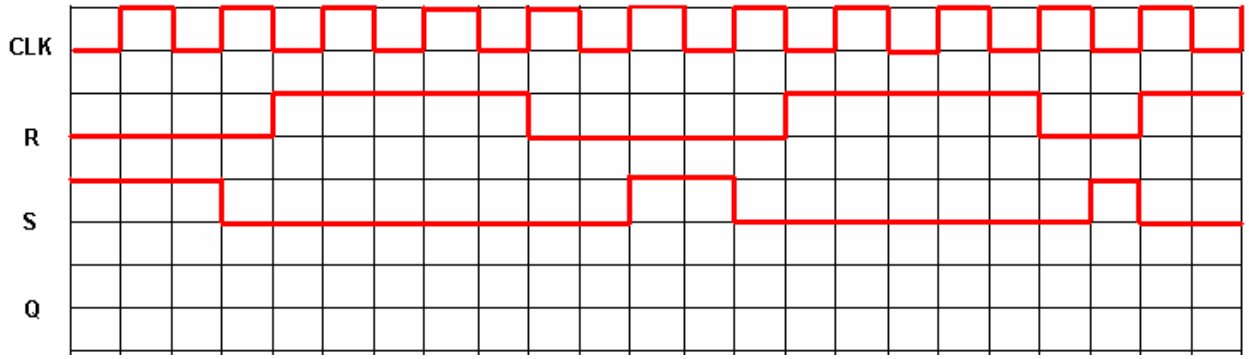


5. Define the term *synchronous* and *asynchronous* as it pertains to digital systems. What makes a digital system *synchronous* or *asynchronous*? Give basic examples of each type of circuit.

6. What are the purpose of the *PRESET* and *CLEAR* inputs of flip-flops. Are these inputs usually *synchronous* or *asynchronous*?

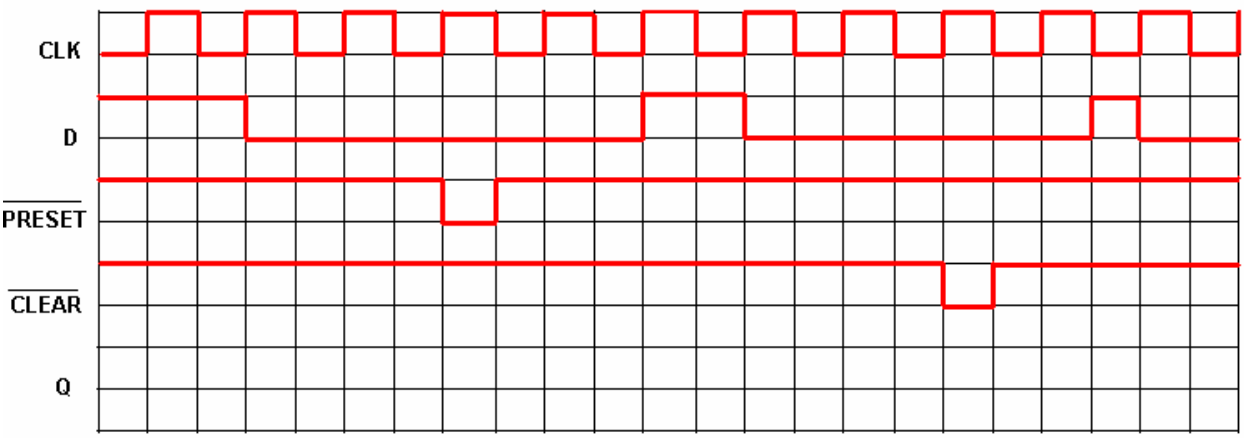
S-R Flip-Flops

6. Given the following timing diagram, draw the waveform for the *next state* output for a negative edge-triggered S-R Flip-Flop. Assume the initial state of the flip-flop is *set*.



Transparent (Data)-Flip-Flops

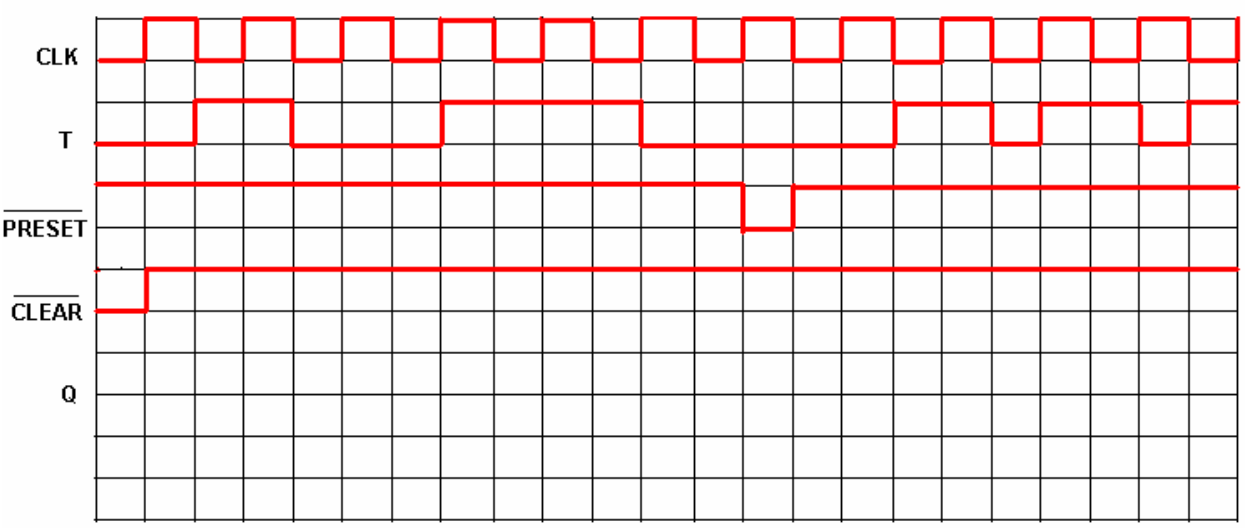
7. Given the following timing diagram, draw the waveform for the *next state* output for a positive edge-triggered D Flip-Flop with *asynchronous* active low *PRESET* and *CLEAR* inputs. Assume the initial state of the flip-flop is $Q = 0$. Repeat the problem, given the *PRESET* and *CLEAR* inputs are *synchronous*. Compare and contrast the two *next-state* outputs.



8. Design a D Flip-Flop using an S-R Flip-Flop and any extra combinational logic.

Toggle Flip-Flops

9. Given the following timing diagram, draw the waveform for the *next state* output for a negative edge-triggered T Flip-Flop with *asynchronous* active low *PRESET* and *CLEAR* inputs. Assume the initial state of the flip-flop is $Q = 0$. Repeat the problem, given the *PRESET* and *CLEAR* inputs are *synchronous*. Compare and contrast the two *next-state* outputs.



10. Design a T Flip-Flop using a J-K Flip Flop and any extra combinational logic.

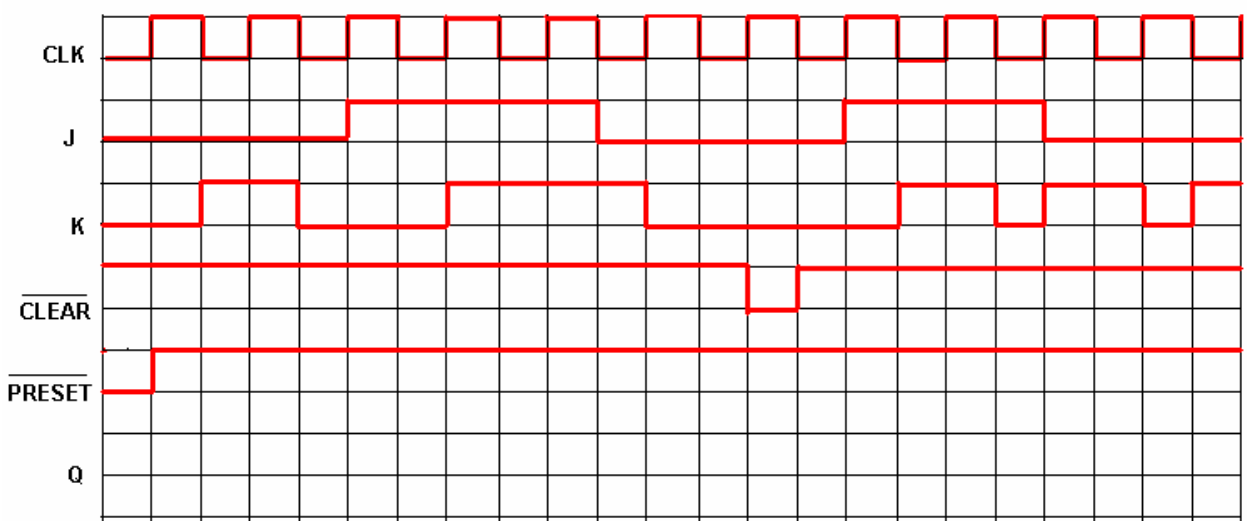
11. Design a D Flip-Flop using a T Flip-Flop and any extra combinational logic.

J-K Flip-Flops

12. Design a J-K Flip Flop using an S-R Flip-Flop and any extra combinational logic.

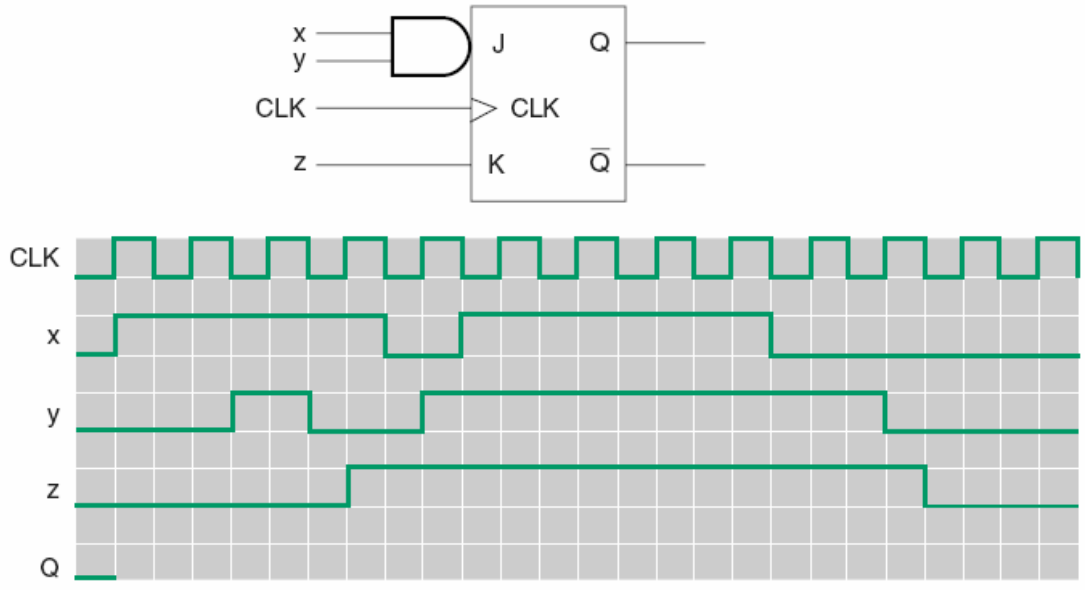
13. Design a J-K Flip-Flop using a T Flip-Flop and any extra combinational logic.

14. Given the following timing diagram, draw the waveform for the *next state* output for a negative edge-triggered J-K Flip-Flop with *asynchronous* active low *PRESET* and *CLEAR* inputs. Repeat the problem, given the *PRESET* and *CLEAR* inputs are *synchronous*. Compare and contrast the two *next-state* outputs.

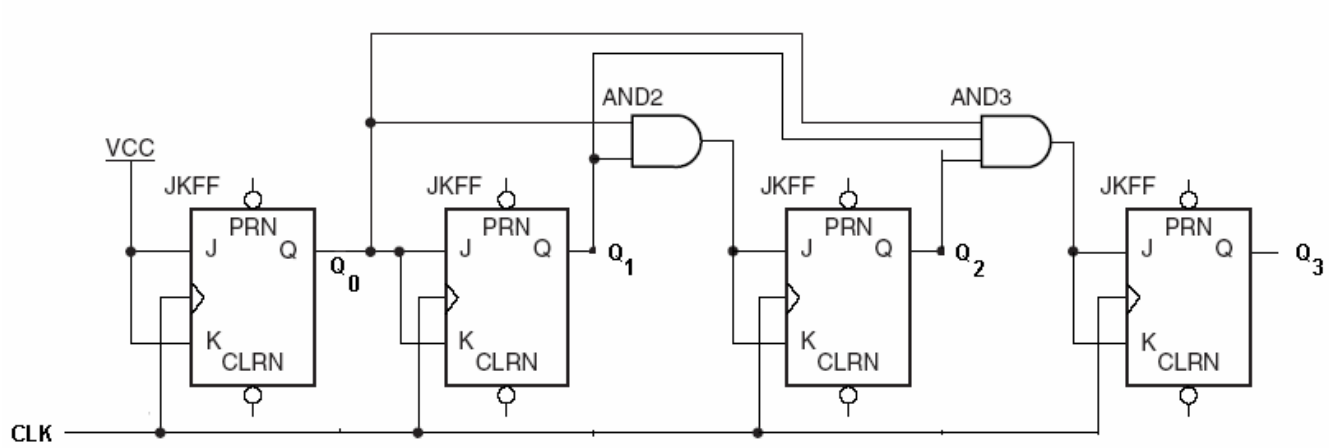


Flip-Flop Circuit Analysis

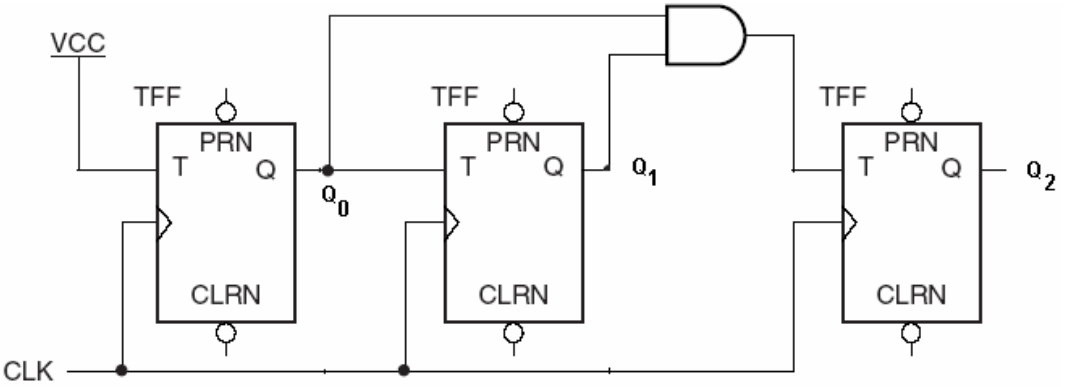
15. Given the following flip-flop circuit, draw the *next state* output for the circuit. Does this circuit perform any use function? Is this circuit *synchronous* or *asynchronous*?



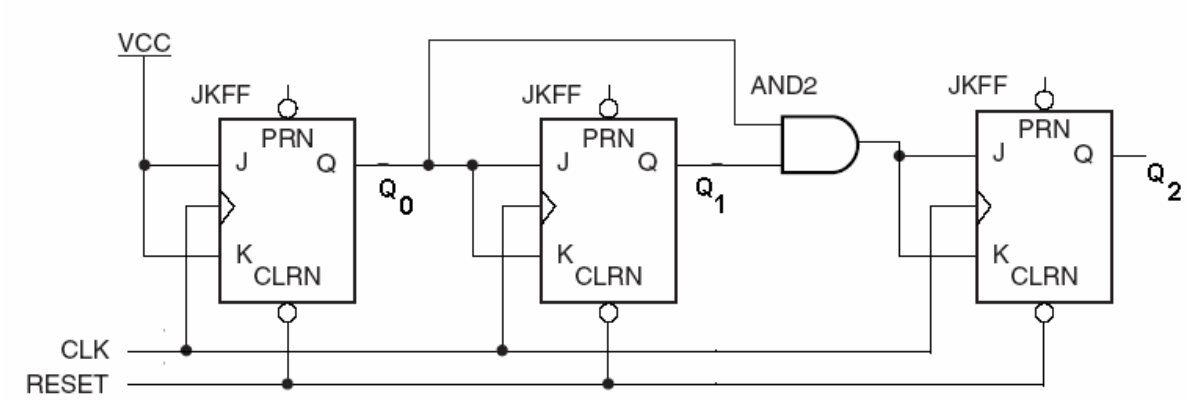
16. Assume all flip-flops in the following circuit are initially in the reset state. Analyze the circuit for the first 16-clock cycles of the CLK input.
    (a) Is this circuit synchronous or asynchronous? Why?
    (b) Make a table to show the sequence of states $Q_3Q_2Q_1Q_0$ after each cycle.
    (c) Draw a timing diagram showing the sequence of states for the 16 clock cycles.
    (d) Does this circuit perform a specific function? If so, what is it?

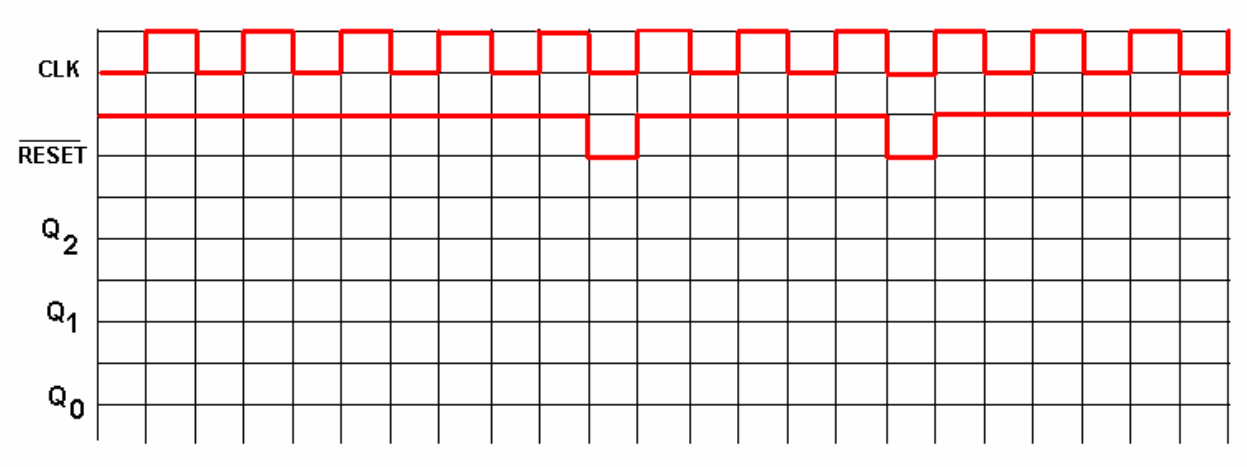


17. Assume all flip-flops in the following circuit are initially in the reset state. Analyze the C circuit for the first 8 clock cycles of the CLK input.
    (a) Is this circuit synchronous or asynchronous? Why?
    (b) Make a table to show the sequence of states $Q_2Q_1Q_0$ after each cycle.
    (c) Draw a timing diagram showing the sequence of states for the 8 clock cycles.
    (d) Does this circuit perform a specific function? If so, what is it?

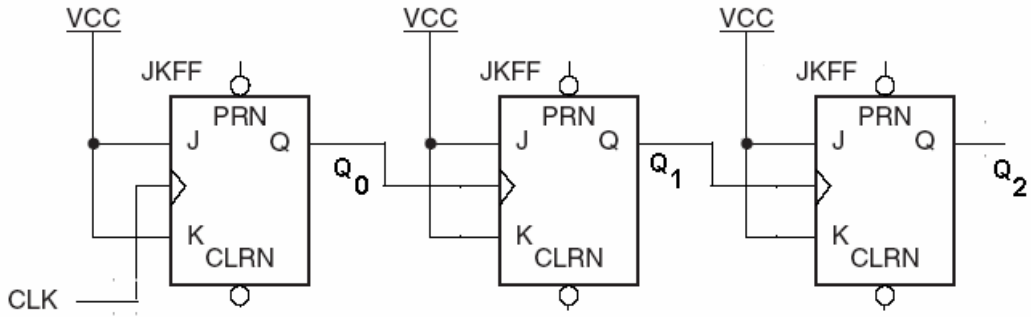


18. Assume all flip-flops in the following circuit are initially in the reset state. Analyze the circuit for the first 8 clock cycles of the CLK input.
    (a) What part of the circuit is asynchronous? What part is synchronous? Why?
    (b) Given the waveforms for RESET below, draw the output waveform for this circuit.
    (c) Draw a timing diagram showing the sequence of states for 8 clock cycles assuming the *RESET* input is a LOGIC HIGH.
    (d) Does this circuit perform a specific function? If so, what is it?





19. Assume all flip-flops in the following circuit are initially in the reset state. Analyze the C circuit for the first 8 clock cycles of the CLK input.
    (a) Is this circuit synchronous or asynchronous? Why?
    (b) Make a table to show the sequence of states $Q_2Q_1Q_0$ after each cycle.
    (c) Draw a timing diagram showing the sequence of states for the 8 clock cycles.
    (d) Does this circuit perform a specific function? If so, what is it?



20. Below is a flip-flop circuit that is called a 4-bit up counter. An *n-bit* up counter counts up to 2^n*-1* and then returns to 0. The counter is connected to a 4-to-2 priority encoder. Determine the counting sequence, $Q_3Q_2Q_1Q_0$ of the circuit below given that it is initially cleared. Assume the up-counter contains a *synchronous* clear.