Homework Assignment #6

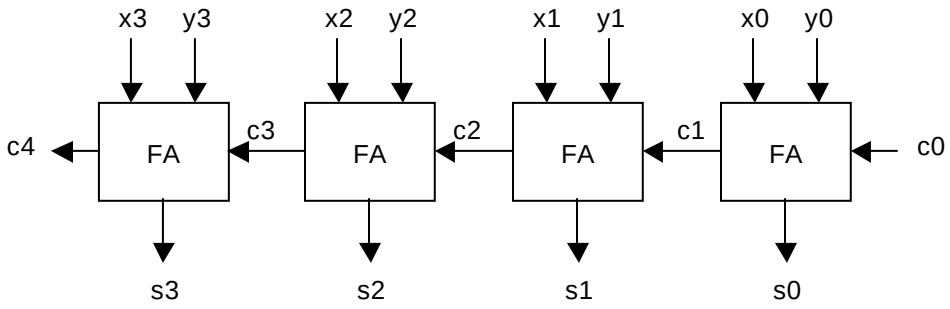
Assigned Thursday, March 3, 2005
Due Thursday, March 10, 2005

(Note – Solutions are posted on the course web site after the due date)

1. (30 pts) You are to design a circuit which inputs a two's complement binary number between –7 and +7. Its output is the absolute value (abs(-5) = abs(5) = 5, etc.). Derive reduced expressions for each output signal. Be sure to take advantage of any "don't care" combinations to simplify the circuit.

2. (20 pts) A circuit adds two 4-bit numbers (x3,x2,x1,x0) and (y3,y2,y1,y0) to produce a 4-bit sum (s3,s2,s1,s0) and a carry out bit c4. Design another circuit to detect a two's complement overflow and output a logic HIGH if an overflow occurs. Use only the signals listed above.

3. (20 pts) The following diagram shows a ripple adder that adds two 4-bit numbers, x = (x3 x2 x1 x0) and y = (y3 y2 y1 y0), and a carry-in bit c0. Consider the inputs x = 1010, y = 1110, c0 = 1.



   (a) Give the binary values for the sum s = (s3 s2 s1 s0) and carry-out bits c = (c4 c3 c2 c1).
   (b) Give the decimal values of x, y, and s if the numbers are 4-bit unsigned numbers. Is there overflow?
   (c) Give the decimal values of x, y, and s if the numbers are 4-bit two's complement numbers. Is there overflow?

4. (30 pts) Consider a 4-bit carry-lookahead adder.
   (a) Write the equations to compute the carry out bits (c1,c2,c3,c4), following section 5.4 in the text.
   (b) Draw the complete circuit for this adder (you can use Quartus).
   (c) Determine the number of gates needed to implement the 4 bit carry-lookahead adder, assuming no fan-in constraints. Note that your total should include the four 3-input XOR gates needed to generate the sum bits. (Hint: the total is greater than 25 but less than 30.)