ECE 370: Digital Systems-Logic Design

Sample Test: Chapter 5-Part 3
Spring 2005

Designing and Implementing Digital Arithmetic Hardware

1. What is the detailed schematic of a 4-bit ripple-carry (also known as a parallel adder) adder design? Use four 1-bit Full Adder components to design the system.

2. The figure below shows a 1-bit implementation of a two's complement adder/subtractor unit. Answer the following questions.

   a) What is the purpose of the XOR gate?
   b) The $\overline{ADD}/SUB$ control signal tied to the CIN input port of the 1-bit Full Adder. Describe why the system is designed in this manner.
   c) Part of the unit is not functioning properly. What is wrong with the unit and how must one modify the design to produce the correct output? Use truth table to aid in your understanding of how the design works and based on the table. Based on the table, describe the problem with the design.

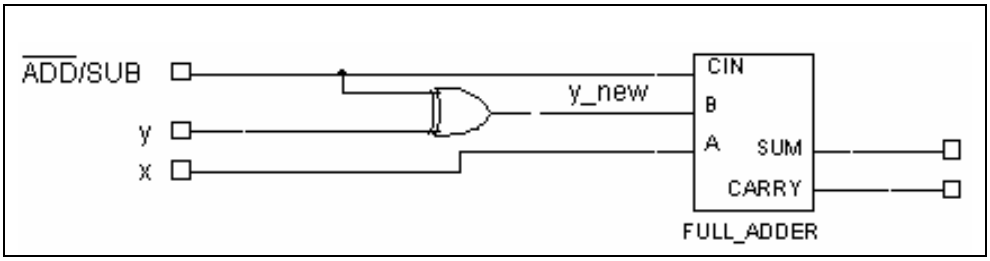

Figure 1: 1-bit Adder/Subtractor Unit for Problem 2

3. Use the corrected design from problem 2 to extend the 1-bit adder/subtractor unit to a 3-bit adder/subtractor. Also, design your unit to detect arithmetic overflow. Provide a detailed schematic of your design.

4. Design a 3-bit one's complement adder/subtractor system using three, 1-bit Full Adder components and any extra gates. Keep in mind the steps needed to perform addition and subtraction using one's complement. Think about how to handle the negative/positive result of zero and design accordingly. Why is this design not practical when it comes to modern digital hardware?

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5. Determine the logic equations for the carry out signals produced for a 3-bit carry look-ahead adder system. Given the carry-look ahead system, use the hierarchical design principle to design a 3-bit carry look-ahead adder system. Make your carry out system a "block" and show a detailed schematic of how all necessary connections to realize the design. What is the benefit of this design over a 3-bit ripple carry adder? What is the drawback, if any?

6. Design a 1-bit Half Subtractor, 1-bit Full Subtractor, and a 1-bit Full Subtractor Using 2 1-bit Half Subtractors. (Hint: Process is similar to 1-bit Adder designs).