GC University, Faisalabad
Mid-Term Exam, Fall Semester-2019

Program: EET 5th Semester
Course: EET-
Semester: 5th
Course Teacher: Engr. Farhan Khalid

Marks: 50
Course Title: Industrial Drives & PLC
Time Allowed: 60 minutes

NOTE:

- **Answer the following questions in order.**
- **All questions are mandatory.**
- **Borrowing anything or discussion with anyone is NOT allowed**.

Sr N0	Question statement
Q#1 (10 marks)	**1- PLC symbol ----|/|---- is called** i-Normally open ii-Normally Closed iii-Coil iv-Relay **2- PLC stands for _____ logic controller** i- Programmable ii-Peripheral iii-Periodic iv-Pneumatic **3- PLC symbol ----( )---- is called** i-Normally open ii-Normally Closed iii-Coil iv-Relay **4- 1 byte of memory consist of** i-1 bit ii-8 bits iii-4 bits iv-2 bits **5- _____ Timer provides pulse signal of desired time:** i-On-Delay Timer ii-Off Delay Timer iii-On-Delay Ext Timer iv-Pulse Timer **6- Output of Q0.0 in PLC will be** i-Boolean ii-False iii-True iv-None **7- Write a short note of Memory addressing in PLC?** **8- Define Count up Counter with Block Diagram?** **9- Write difference between Integer & double number in PLC?** **10- Short Note on Off-Delay Timer with block Diagram.**
Q#2. (10 marks)	Write a short note on PLC. Draw block diagram of PLC & explain different its parts?
Q#3. (10 marks)	Define following functions with diagram, i-Move instruction ii- Memory Addressing of PLC iii- On-Delay Timer iv- Count down counter v- Comparator (==1)
Q#4 (10 marks)	Draw Ladder Logic for following functions i-And Gate ii-NOR Gate iii-Y = A+A.B iv- Flip Flop v-XOR Gate
Q#5 (10 marks)	Draw Ladder Logic for two way traffic light signal.