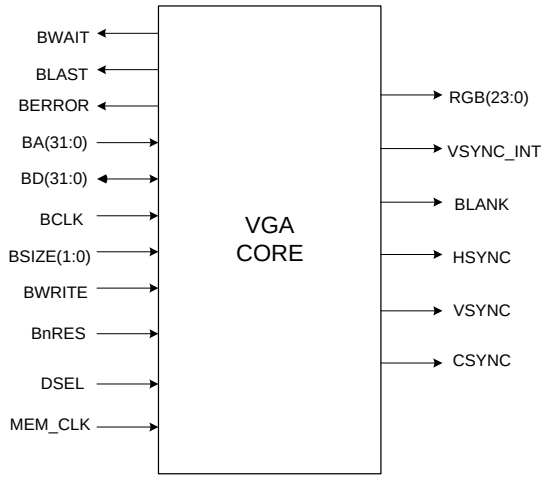
VGA CONTROLLER

FEATURES

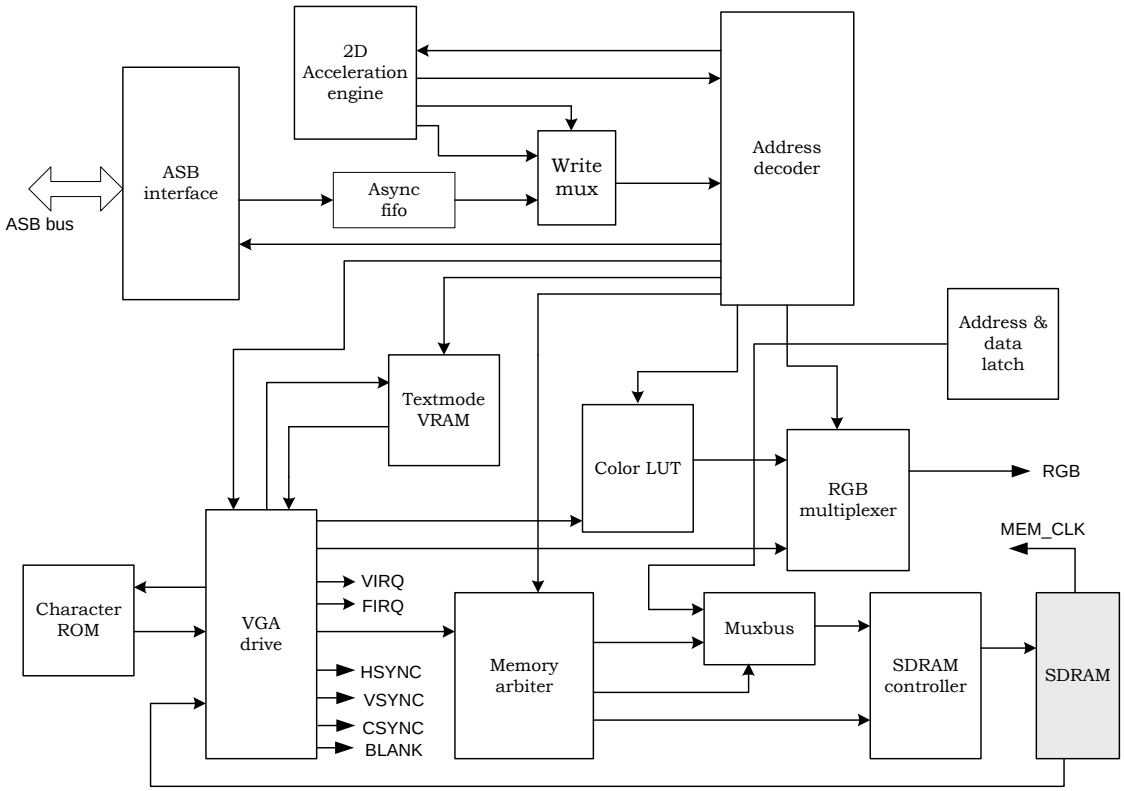


• VHDL source code
• Slave interace to AMBA ASB bus
• Synchronous design, single clock edge
• Graphic mode 640x480.
• Text mode 80x30 (one char 8x8 pixels).
• 8 bit pseudo color (256 colours from palette of 16777216)
• 16 bit high color (5-6-5 XGA 65535 colors)
• Screen refresh 80 Hz.
• 1 MB Video RAM (external SDRAM).
• 7.5 kB textmode RAM (internal FPGA)
• Simple 2D hardware acceleration of line drawing and box filling
• Double buffering (only in 8 bit pseudo color mode).

OTHER:

• VESA DPMS Power Management support.
• programmable color lookup table 256x24.
• char generator supporting ASCII
• hardware cursor in text mode.
• hardware character inversion in text mode
• input FIFO 256x64 bit
• AMBA cycle 1 wait state minimum, 4 maximum
• max core frequency f_{MEM_CLK} = 72 MHz on VirtexE
• Two clocks: BCLK(20 MHz) from AMBA and MEM_CLK(33 MHz) from HES board.
• ROM and text RAM as well CLUT are Virtex Block RAMs. (18 out of 160)
• Graphic memory is 64Mbit SDRAM (32 bit, CAS latency 2, burst size 8).
• Vertical blanking interrupt.
• Programmable I/O registers.
• Peak fill rate for 2D: 19 Megapixels/s for pseudocolor, 9 Mpixels/s for 16 bit high color.
• Number of SLICEs: 1500 out of 19200 7%
• Number of BLOCKRAMs: 18 out of 160 11%

3. **Block Diagram**



Project for my master thesis, for more details please contact me at mikel262[at]REMOVESPAMgmail.com