Miguel R. Corazao

2407 Falmer Court
Cedar Park, Texas 78613

512-249-0524 / 512-745-9488
mcorazao@yahoo.com

EDUCATION

University of California, Berkeley, 1992 – 1994.

- *Degree*: M.S.E.E., May 1994 (*Specialization*: Computer-Aided Design of VLSI).
- *Research*: Retargetable synthesis/compilation (*Advisor*: Jan Rabaey).

University of Texas at Austin, 1987 – 1992.

- *Degree*: B.S.E.E., May 1992 (*Specialization*: Computer Engineering).

ACHIEVEMENTS

Timing Analysis

- Led chip-level timing analysis for a semi-custom microprocessor using Primetime.
- Facilitated PrimeTime/Pathmill block-level timing debug and maintained instantaneous timing databases.

Logic Verification

- Owned logic verification sign-off of a block in a network bridge device and developed much of the test bench IP for chip-level sign-off using Versity Specman and Synopsys VCS.
- Developed and maintained automated chip-level verification regression infrastructure.
- Created a custom random assembly code generation tool for a digital signal processor.

Logic Design

- Developed and supported dual macro libraries consisting of RTL and netlists.
- Implemented macro test cases and helped in design debug.

Physical Integration

- Owned floorplanning, placement, and routing of multiple blocks of a VLIW microprocessor.
- Acted as chip-level integrator for final cleanup for processor tape-out using custom Skill development.

Design Automation

- Developed a tool suite for modeling sleep FET voltage waveform for cell-based timing/noise.
- Created PrimeTime/Pathmill-based timing flow for semi-custom microprocessor core.
- Developed an interactive, multi-user, chip-level timing query system (daemon/client system).
- Implemented a tool suite for incremental, automatic buffer insertion for timing optimization.
- Designed a methodology for automatic datapath layout based on user constraints / regularity extraction. Enables rapid re-implementation after substantial netlist changes.
- Developed a datapath logic design flow for writing Verilog netlists with RTL-like simplicity.
- Implemented a tool to generate RTL, Specman models, and docs for complex register banks.
- Developed LEC-based formal equivalence methodology for chip sign-off.
- Created tool set for analyzing netlists for ERC (e.g. loops, min. logic stages, naked flops, etc.).

Embedded Software

- Developed an embedded Cisco IOS-like command-line interpreter for network management (10,000+ lines of C++). Created a custom interpreter generator for rapid enhancement.
- Designed and implemented an OO database library and kernel interface API for management of an IA32-based network bridging system. 7000+ lines of C++ with BerkeleyDB.
- Created diagnostic boot test firmware for an x86-based network bridge (mem tests, PCI, etc.).

SKILLS

- **Programming Languages**:
  Recent: C++, C, Perl, Java, Tk, TCL, Skill.
  Previous: Specman E, Python, Lisp, Visual Basic, Scheme, Pascal, Fortran, Awk.
- **Networking Protocols**:
  Gigabit Ethernet, InfiniBand, TCP/IP.
- **VLSI CAD Software**:
  PrimeTime, Cadence DFII, LEC, Einstimer, Design Compiler, Pathmill, SmartCell, Specman, VCS, Debussy, Silicon Ens., IC Compiler/Apollo, HSpice, Calibre, PDP, ClearCase, Synchronicity, CVS.

Miguel R. Corazao

EXPERIENCE

Advanced Micro Devices, Inc., Austin, TX, 2007 - 2008.
Organization develops microprocessors for desktop/laptop markets.
CAD Engineer.

- Developed software for modeling sleep transistor timing effects throughout clock cycle.
- Implemented tool suite for maintaining all timing models (Liberty, SDC, Einstimer) over multiple corners as single format.
- Provided internal customer mentoring and training.
- Owned and delivered third-party cell libraries including software for porting to AMD flows.

Texas Instruments, Inc., Wireless Business Unit, Austin, TX, 2004 – 2007.
Organization develops parts for the wireless consumer electronics industry.
Integration Engineer.

- Team developed a high-performance, semi-custom ARM processor core for OMAP products.
- Led top-level timing analysis with PrimeTime for timing closure through tape-out.
- Developed complete PrimeTime/Pathmill-based timing flows as well as general EDA support.

Silicon Laboratories, Inc., Austin, TX, 2003 – 2004.
Corporation develops mixed-signal parts supplying consumer electrics industries.
CAD Engineer.

- Provided primary front-end digital design support: NC-Verilog, DC, PrimeTime, LEC, etc.
- Developed Silvaco-based cell characterization flow and delivered custom cell libraries.

OmegaBand, Inc., Austin, TX, 2001 – 2003.
Corporation develops data center I/O consolidation systems using Infiniband/Ethernet.
Software Engineer.

- Created a diagnostic test tool suite for an IA32-based network bridge.
- Implemented an embedded Cisco-like command-line interpreter for network management.
- Developed a kernel-access and database API library for network management tools.
- Designed kernel-mode /proc driver firmware for interfacing to network subsystem.

Verification Engineer.

- Owned logic verification sign-off of scheduling unit in network processor using Specman/VCS.
- Created RTL/verification model generation software for register banks.
- Implemented chip-level verification IP including packet models, stim. generators, and monitors.
- Developed and maintained automation for regressions and design database maintenance.
- Provided general EDA software development services to the design team.

Intel Corporation, Microprocessor Products Group, Austin, TX, 1999 – 2001.
Organization develops high-performance IA32 desktop microprocessors.
Methodology Engineer.

- Designed/developed a buffer insertion tool suite for timing optimization.
- Designed/developed front-to-back tool suite for semi-custom datapath layout.
- Mentored junior colleagues on multiple projects and provided customer training.

Previously: **Equator Technologies, Inc.**, **Motorola Inc.**.

PUBLICATIONS

- M. Corazao, M. Khalaf, L. Guerra, M. Potkonjak, J. Rabaey: "*Instruction Set Mapping for Performance Optimization*", ICCAD, 1993.
- M. Corazao, M. Khalaf, L. Guerra, M. Potkonjak, J. Rabaey: "*Perf. Opt. Using Template Mapping for Datapath-Intensive High-Level Synthesis*", IEEE Trans. on CAD, 1996.

REFERENCES

- David Artz, Senior Design Engineer, NVidia, (512) 517-5148, davidartz@earthlink.net.
- Ziad Sadi, Integration Lead, Texas Instruments, (512) 468-9575, ziad@ti.com.
- Mayur Mehta, Vice President, D2 Audio, (512) 506-1297, mayur@ieee.org.