Analysis of Ground Bounce Induced Substrate Noise Coupling in a Low Resistive Bulk Epitaxial Process:

Design Strategies to Minimize Noise Effects on a Mixed-Signal Chip

Matt Felder, *Member, IEEE,* and Jeff Ganger, *Member, IEEE*

Motorola- Wireless Subscriber Systems Group- Semiconductor Products Sector

ABSTRACT

The industry trend towards system-on-chip solutions continues to push the limits of mixed-signal design. Increasing the integration of analog and digital circuitry causes a struggle to maintain analog signal integrity. Digital switching noise coupling through the common substrate is both difficult to measure and difficult to control. This paper introduces and applies a practical first-order simulation methodology for performing a substrate noise analysis in a low resistive bulk process. Although this subject has been analyzed in numerous journal articles, few have applied their analysis method to a whole-chip design. This SPICE model will allow mixed-signal designers to determine design variables that will minimize substrate noise. This work elaborates on key aspects of substrate noise that available references do not handle adequately including: sources of substrate noise, determination of power rail and bulk resonance frequencies, and alternatives for bulk biasing. The new model is used to analyze Motorola's 56824, the latest low cost 16 bit DSP design. The analysis includes the determination of: 1) the on-chip bus and I/O bus noise coupled to the substrate, 2) the dominant resonant frequencies in the chip, and 3) the best bulk biasing alternative.

1. Introduction

The lower cost and reduced power consumption of single chip solutions motivates technology improvements in mixed-signal design. Mixed signal design is characteristically plagued by crosstalk occurring between the noisy digital and sensitive analog portions of the circuit. Fast digital switching transients couple to the sensitive analog circuitry through interconnect parasitics and through the silicon substrate. Interconnect crosstalk can be partially controlled through specialized place and route tools. However, substrate crosstalk is not handled as easily. Highly doped bulks used in low-cost CMOS designs are especially prone to substrate crosstalk.

Much of the previous substrate noise work focused on complex substrate parasitic mesh extractions [3,4]. It is

proposed in this work that a complex substrate extraction is not required for a first-order analysis of substrate coupled noise in a low resistive epitaxial process. However, it will be shown that the package pin model and the chip-wide power rail parasitic capacitances greatly effect the characteristics of the substrate noise. These effects must be included in any meaningful substrate noise analysis.

This first order substrate noise model will allow mixed-signal designers to analyze high-level design performance trade-offs including: choosing the number of power and ground leads, isolating noisy and quiet power and ground buses, selecting bulk biasing alternatives, tweaking noise conduction by adding on-chip capacitance, adjusting the digital transition times, and analyzing the power supply resonance frequencies. This substrate noise model will reduce both overdesigning and design iterations- leading to lower cost and improved time-to-market.

This substrate noise analysis is applied to the DSP56824, the latest low cost 16 bit DSP being released by Motorola. The architecture and instruction set makes it suitable to replace both uP and DSP functions in low cost, moderate performance systems. The core clock frequency is adjustable from 20MHz to 35MHz. The 16 bit DSP core architecture is a four phase system, and the PLL clock or main clock is twice the core clock. A design target of 8% of the cycle time of the main clock was allowed for peak cycle to cycle jitter, for a 40MegHz to 70MegHz clock this leads to a minimum cycle to cycle jitter performance of approximately 1nS.

The main noise sources in the 16 bit DSP test chip are large busses which are highly capacitively loaded, such as memory busses, peripheral busses, and instruction and data busses. The I/O busses deliver the greatest disturbance to the PLL clock and required a separate analysis and simulation.

The block which dominates cycle to cycle jitter in the PLL is the VCO. PLL loop dynamics require that the VCO have high gain and high bandwidth which makes it a prime target for coupling noise into a DSP system. The noise coupled into the VCO to the PLL clock has a high pass characteristic which means there is little cycle-to-cycle jitter noise suppression. The reduction in cycle-to-cycle noise for a PLL on a DSP chip can only be controlled by the designer by improving PSRR, reducing ground bounce, or reducing substrate coupling. Since PSRR techniques are well understood this paper examines the ground bounce induced noise coupled through the substrate into the sensitive analog circuit of the PLL which is the VCO.

The substrate noise simulations show that some intuitive attempts to reduce substrate coupled noise may actually increase it. For instance, a designer might guess that disconnecting the analog ground from the bulk would decrease

the coupling of substrate noise into the analog circuitry. The model shows that for the 16 bit DSP test chip, disconnecting the analog ground from the bulk can increase the substrate noise coupled into the analog rails by 73%.

The best bulk biasing alternative is highly dependent on design parameters such as the chip size, the ratio of analog-to-digital chip area, the number of Vdd and Vss supply leads, the size of on-chip decoupling capacitors, and the type of noise that is most problematic. Designers should perform adequate high-level substrate noise simulations, adjusting each of the above parameters to minimize performance degradation caused by substrate coupled noise.

2. Analysis Concept

Every switching transient injects noise into the bulk. For inverting CMOS logic, there is approximately one falling edge for every rising edge. This provides an amount of noise cancellation in the substrate. When a group of transistors switch simultaneously to the same logic level, poor cancellation can result in a significant noise spike. The worst-case noise can be approximated by assuming that all lines of the largest bus driver switch from one logic level to the other [3].

Some of the previous work used a single noise source to represent the worst case noise [3-5]. This is adequate for on-chip bus drivers, where all bit drivers can be lumped into a single large driver and a single load. However, this approach will not be sufficient to model I/O drivers. The load for each bit is a package pin and board capacitance that cannot be lumped into a single simple load. The package pins should be kept separate to reflect the mutual inductance and capacitance effects.

Some of the previous work ignored or misrepresented the whole-chip power rail parasitic capacitance effects[2]. Only the parasitic capacitance of the noise source and sensor were modeled. It has been determined that including the whole-chip power rail parasitic capacitance is necessary for a reasonably accurate noise signature [3,6].

Whole-chip capacitances greatly affect capacitive coupling from the bulk to the power and ground rails. The junction capacitance into one MOSFET source is very small, but the parallel summation of the junction capacitances for all MOSFET sources connected to the same power or ground bus can be quite large. The chip-wide Nwell junction capacitances are even larger. The nature of substrate noise conduction requires that the chip-wide capacitances be included between all power rails, ground rails, and the bulk.

The parasitic capacitances of the power and ground rails form multiple resonance circuits with the lead inductances. Any noise injected into the power rails, ground rails, or bulk will take-on the resonance frequency of that

node. This will further affect propagation of noise throughout the circuit.

It is good practice to determine the resonant frequency of the Vss rails, Vdd rails, and the bulk. The impedance to AC ground (board ground) will be the highest at the resonant frequency of the ground and power rails. Digital switching that produces harmonics that coincide with the bulk, power rail, or ground rail resonant frequencies should be avoided [3,6].

3. Process Technology

In the CMOS epitaxial process, a highly doped substrate is used to increase latch-up immunity. Unfortunately, the highly doped substrate provides a very efficient conduction path for substrate noise. The p+ buried layer collects and distributes noise throughout the integrated circuit. The good news is that it is easy to generate a sufficient SPICE model for the substrate. The low-resistive buried layer can be modeled as a single node [3].

Since the majority of the substrate noise conducts through the low resistive bulk, separating the sensitive and perturbing nodes of the circuit provides little or no improvement in noise immunity (Figure 1). If two nodes are separated by more than four times the thickness of the epitaxial layer ($d>4T_{epi}$), then the resistance between the nodes is independent of distance [3]. When the vertical resistance (R_2) of the epitaxial layer is much less than the horizontal resistance (R_1), the horizontal distance no longer affects the effective resistance between the two nodes. Complex and expensive isolation techniques like SOI and junction isolation show some promise for future generations of mixed-signal design. This paper describes a number of design alternatives for the current epitaxial process technology that can limit the effect of substrate noise without drastically affecting the cost of production.

Reference articles on substrate noise commonly confuse substrate noise reduction methods for low-resistive versus high-resistive bulk processes. For the low resistive epitaxial process n+ guard ring diodes provide no effective reduction in substrate noise, and p+ guard rings provide up to a 30% noise reduction ONLY when they are biased by a dedicated ground pin [4,5]. Dedicated ground pins are generally not an option for low cost DSP design. It is possible that greater overall noise reduction could be achieved by using the extra pins to lower the power rail inductance.

The resistance from the bulk biasing lead into the p+ buried layer is very small. The parallel summation of many contact resistances reduces the effective resistance to a nearly negligible amount. This means that for a first order

approximation of substrate noise we can treat the bulk biasing lead and the p+ buried layer as a single node. The substrate noise analysis will involve accounting for all mechanisms of noise coupling into and out of this single node.

4. Substrate Noise Conduction Pathways

4.1. Digital-to-Bulk Coupling Mechanisms

Noise is injected into the bulk by three mechanisms: resistive coupling, capacitive coupling, and impact ionization (Figure 2) [7]. First, if the bulk is biased with a switching ground bus, switching transients will couple resistively into the bulk through the p+ bulk contacts. The parallel summation of all of the bulk contacts and epitaxy resistances provides a very low impedance path (nearly a short) to the p+ buried layer.

The second biggest source of noise is capacitively coupled through substrate pn junctions. The MOSFET source and drain form a pn junction with the bulk. The junction capacitance for one transistor is fairly small. However, many NMOS sources are connected to the same Vss rail. The total source-to-bulk junction capacitance for all NMOS devices with the source tied to the same Vss rail is significant (273 picofarads for the quiet digital Vss on the 16 bit DSP test chip). If the source and bulk are tied together, then the junction capacitance is effectively shorted and can be ignored.

Each Nwell introduces a fairly large pn junction with the bulk- this causes a large capacitance between the Vdd rail biasing the Nwells and the Vss rail biasing the bulk. Depending on the size of the chip and the process technology, the parasitic junction capacitance between Vdd and Vss rail can range from fempto-farads to nanofarads. The largest power rail junction capacitance for the test chip is 1.43 nanofarads.

The least significant source of substrate noise is impact ionization current generated at the pinch-off point of the NMOS transistors. Impact ionization causes a hole current (positive transient) in the bulk. Although the impact ionization current is included in the simulations, this current is an order of magnitude less than the resistive or capacitive coupled current. For other process technologies, the impact ionization may be more significant.

4.2. Bulk-to-Analog Coupling Mechanisms

There are three bulk-to-analog coupling mechanisms (Figure 3). First, if the bulk is biased with the analog ground rail, then substrate noise will couple resistively through the p+ bulk contacts. Second, the Nwell junction capacitance and the source-to-bulk junctions capacitively couple substrate noise into the analog circuit power and

ground rails. Third, if the bulk is not biased by the analog ground rail, then the body effect will couple substrate noise into the analog circuit.

If the analog Vss is not connected to the bulk, a negative bulk transient will increase the depletion region between the source and bulk. This depletes the channel of charge carriers and increases V_t. The total effect is a sporadic decrease in the I_{ds} current. The easiest way to limit the body effect is to tie the analog Vss to the bulk. When the analog Vss follows the bulk voltage, the body effect is eliminated.

If the analog Vss cannot be tied to the bulk, then increasing the analog Vss capacitance to the bulk will lower substrate noise effects in two ways. First, the bulk-to-source voltage transients will be lowered, thereby reducing the body effect. And second, since the Nwell capacitance is usually much higher than the source-to-bulk capacitance, adding capacitance from the analog Vss to the bulk will help balance the coupling into each rail. This "balanced coupling" will reduce the effective noise seen across the analog power rails.

4.3. Other Digital-to-Analog Coupling Mechanisms

Although this work primarily deals with substrate coupled noise, it necessary to include some additional mechanisms for digital-to-analog coupled noise. Correct analysis of capacitive coupling blurs the distinction between substrate coupled noise and interconnect coupled noise. The parasitic interconnect capacitance of the Vss rail that biases the bulk can be a significant pathway for injecting substrate noise. In the 16 bit DSP test chip, the interconnect capacitance between the digital Vdd and Vss is especially large due to intentional overlapping in the layout. The digital power rail interconnect capacitance of 290 picofarads helps to reduce digital switching noise as will be explained later in this paper.

Chip designers place diodes between power and ground buses to clamp potentially damaging voltage spikes caused by electrostatic discharge. The test chip has an ESD diode from the quiet digital Vdd to each of the other Vdd and Vss rails. These diodes contribute to the total capacitance between the power rails. The parasitic interconnect and ESD junction capacitances for the entire chip can be quite significant and should not be overlooked.

5. Simulation Circuit Elements

5.1. Package Leads

Accurate substrate noise modeling requires accounting for all AC paths to the board ground. All of the Vdd and Vss rails are coupled either resistively or capacitively to the bulk. Therefore all Vdd and Vss rails affect the impedance path to the board ground. The 16 bit DSP test chip has five separate Vdd and Vss rails. Even if a specific simulation only involves devices connected to two of the five rails, all of the rails must be included in the simulation. The resistive and capacitive connections of these power rails to the bulk can drastically affect the bulk impedance.

The package pin model used should be accurate for all frequencies of interest. Substrate noise simulations can produce noise frequencies around one gigahertz. To maintain accuracy up to the low gigahertz range, the leads for the 100 TQFP test chip package are modeled with two lumps- one for the wirebond and one for the pin (Figure 4).

The resistance of the leads slightly increases at high frequencies due to the skin effect. The simulations in this work use a constant resistance of 0.1Ω- only slightly above the 50 MHz resistance of 0.07Ω. The simulations will slightly underestimate the dampening of high frequency noise; however, the skin-effect resistance does not affect the peak noise amplitude. The two-lump SPICE model for the package leads is reasonably accurate up to 2GHz. Simulations with frequencies above 2GHz demand a more accurate lumped parameter interconnect model.

If the substrate noise simulation involves the I/O drivers, then all of the I/O pins must be included in the SPICE model. Also, all of the significant capacitive and inductive coupling terms should be included for the I/O pins. The package pin subcircuit for this work included all coupling terms that were at least 5% of the adjacent pin coupling term. This simplification increases the simulation speed without significantly impacting simulation accuracy.

If only the on-chip drivers are being simulated, then only the Vdd and Vss pins need to be included. This assumes that each pair of Vdd and Vss pins are separated by enough pins that only the adjacent pin mutual inductance and capacitance is significant.

5.2. Junction Diode

Each junction diode has an inherent series resistance corresponding to the contact resistance and the silicon resistance. In the current Motorola process (Table 4), for frequencies below 10GHz, the contribution of the resistance to the impedance is negligible compared to the junction capacitance. A 10ff junction capacitance has approximately 40Ω of series resistance. Each Vdd power rail has a large number of Nwell-to-bulk diodes and each Vss power rail has a large number of source-to-bulk diodes. These diodes contribute a significant amount of power rail to bulk parasitic capacitance that must be included in the substrate noise simulations.

The junction diode depletion capacitance is dependent on the reverse bias voltage. As the reverse bias increases, the depletion region increases, and the depletion capacitance decreases. The parasitic capacitance extraction tool provides the junction diode size and an equivalent capacitance from the layout. However, the capacitance value provided is not necessarily the same capacitance for the bias point in the substrate noise simulation. It is good practise to place the extracted junction diode (not the junction capacitance) into the substrate noise simulation circuit to determine the junction capacitance at the correct bias point. If voltage transients do not cause the diode to turn on, the junction diode can be modeled by the equivalent capacitance.

5.3. Power and Ground Rails

The 16 bit DSP test chip has 5 separate Vdd and Vss power rails: quiet digital (referred to as “digital” for most of this paper), analog, data I/O, address I/O, and other I/O. The quiet digital power rail is only for logic circuitry and on-chip bus switching. The I/O rails are only off-chip bus switching. The analog power rails are mostly for non-switching circuitry.

An ideal power or ground rail can be modeled as a single node. Unfortunately, true power rails have a finite resistance and capacitance that cause some power loss and time delay. Using the pi model to account for the rail non-ideality requires that it be broken into n segments of series resistance and m parallel capacitances (where m=n+1).

For the quiet digital supply, the junction capacitances will be non-uniformly distributed along the rail (Figure 5). This model would be difficult to generate from the layout. Using a simpler single-lump pi-model is more appropriate (Figure 6). Although this model is less accurate, it is very simple to include in the substrate noise simulations and accounts for some line loss.

The junction capacitances for the I/O supply rails will be distributed uniformly along the power rail (spaced by the physical distance between each I/O pad). Therefore, it is reasonable to use the distributed capacitance model with a segment for each I/O pad. The resistance R/n will be the rail resistance between two I/O pads. The I/O rail subcircuit will look like Figure 5, but there will be a C/m and a CJ/m between each R/n.

6. Power Rail and Bulk Resonance

The most important aspect of substrate noise conduction is the resonant frequencies present in the circuit. The noise signature in any particular node is dependent on the injected noise and the frequency response of that node.

The frequency response of each node is dependent on the LC resonant pathways through that node. Multiple power and ground rails can introduce a number of resonant pathways that yield a complex frequency response. The 16 bit DSP test chip has five separate power and ground rails and a total of 45 resonant pathways through the supply and ground leads. The easiest way to determine the dominant resonance frequencies is to plot the frequency response of the impedance (Figure 7). This plot of the 16 bit DSP test chip bulk impedance shows that the dominant resonance frequencies in the bulk are 173MHz and 3.7GHz. There is much less noise energy produced at 3.7GHz, so 173MHz is the resonance frequency that will be most significant.

When the bulk resonance frequency corresponds with the first or second harmonic of the digital switching frequency, the substrate noise level can increase significantly. The test chip simulations show a 50% increase in the peak substrate voltage when the bulk resonance (173MHz) is the first or second harmonic of the digital switching frequency. The third harmonic showed no significant increase. The 35MHz core clock does not approach the bulk resonance until the fifth harmonic. Therefore, the digital switching frequency should not cause a dramatic increase in the substrate noise.

Figure 8 shows the substrate and power rail noise for the test chip with a 35MHz digital switching clock driving an on-chip bus load. For this simulation, only the Digital Vss biases the bulk. All but the last two signals are with respect to the board ground. The digital rails resonate at the same frequency as the bulk (173MHz) because the digital Vss is biasing the bulk and there is a very large Nwell capacitance (~1nF) between the digital Vdd and digital Vss. The analog power rails resonate at a higher frequency (1.15GHz) due to much smaller Nwell capacitance (~5pf). The analog Vdd rail also has a 173MHz component that capacitively couples through the ESD diode connected to digital Vdd and the Nwell junction connected to the bulk.

The designer should avoid digital switching that produces first or second harmonic frequencies that correspond to the bulk resonance frequency. Unfortunately, even if this kind of analysis is performed, capacitance extraction errors and process variations might shift the expected bulk resonance to the frequency the designer wished to avoid. It is theoretically possible to design a circuit with adjustable bulk capacitance (Nwell or NMOS source junctions) that can be used to "tune" the bulk resonance to a harmless frequency. However, this solution will likely be cost prohibitive because of the required IC real estate. Forbes mentioned that forward-biased guard ring diodes can be used to "tune" the bulk resonance [5]. One disadvantage of this solution is that large forward biased diodes will cause a power drainage that is unacceptable for many applications.

7. The Nature of Digital CMOS Switching Noise

The second most important aspect to understanding substrate noise is the signature of digital CMOS switching noise. For large CMOS circuits there is on average one falling edge for every rising edge [3]. This provides an amount of noise cancellation in the substrate. However, it will be shown in this section that depending on the bulk biasing scheme used, either the rising edge or falling edge of digital switching produces more noise.

There are two types of CMOS switching that produce distinctly different substrate noise signatures: on-chip bus switching and I/O bus switching. It was found during this analysis that in the 16 bit DSP test chip the substrate noise due to on-chip bus switching is an order of magnitude smaller than the I/O bus switching noise. Although it is a less significant source of noise, it is important to analyze and understand the noise coupling mechanisms for on-chip switching. The coupling mechanisms for on-chip switching noise will lead to insights for reducing the overall noise.

7.1. Digital CMOS On-Chip Bus Driver Noise

An important factor in simulating CMOS on-chip bus driver noise is correctly modeling of the typical bus load. Some of the previous work in substrate noise analysis mistakenly placed the full capacitive load to the digital Vss. This will give misleading simulation results. A typical on-chip bus capacitive load was calculated from the test chip parasitic capacitance extraction program (Table 1).

Seventy percent of the capacitive load is interconnect capacitance with the bulk. The remaining 30% is connected to the inputs and outputs of tri-state buffers (Figure 9). The tri-state inputs add gate capacitance, and the tri-state outputs (PMOS and NMOS drains) add junction capacitance. Since the PMOS transistors are approximately 2.5

times larger than the NMOS transistors in the 16 bit DSP test chip, the non-interconnect load is dominated by capacitance to Vdd.

The digital circuit Nwells are always biased by the digital Vdd, so any load capacitance to the Nwell is shown as Vdd capacitance. The p+ bulk contacts, however, can be connected to digital Vss, analog Vss, both analog and digital Vss, or a non-power carrying Vss. The load capacitance to the bulk is modeled as capacitance to the bulk biasing Vss rail.

7.2. On-Chip Bus Driver Noise with Digital Bulk Biasing

Capacitance between the digital Vdd and Vss rails serves two beneficial purposes. First, it acts as a decoupling capacitance so that the Vdd and Vss rail voltages tend to follow each other. This will reduce the rail noise by keeping the Vdd to Vss potential difference relatively stable. Second, the capacitance between digital Vdd and Vss will have a charge sharing effect with the on-chip bus load (explained in detail later). This charge sharing effect will limit the peak noise voltage caused by on-chip bus driver switching.

Interconnect capacitance and ESD junction capacitances between the digital Vdd and Vss rails are typically much smaller than the digital Nwell junction capacitance. Using the digital Vss to bias the bulk adds the large Nwell junction capacitance to the effective digital decoupling capacitance. The designer may also choose to add an extra digital decoupling capacitor to the IC chip package [3]. This extra capacitance can also be used to tune the power rail resonance frequency away from a harmonic of the digital switching frequency.

Figure 10 shows a simplified schematic for the on-chip bus driver in the 16 bit DSP test chip with digital bulk biasing- the digital Vss node is the same as the bulk node. The power and ground leads are shown as only inductances to simplify the figure. All sixteen lines of the bus are lumped into a single inverter and capacitive load. With the digital Vss connected to the bulk, 78.5% of the bus load is coupled to digital Vss and 21.5% is coupled to digital Vdd. The effective digital decoupling capacitor is the sum of the interconnect, ESD, and Nwell capacitances. There is no added decoupling capacitor in the test chip package.

When the on-chip bus load is driven high, the PMOS transistor shorts capacitor A. The PMOS transistor also places capacitor B (with no initial charge) in parallel with the precharged capacitor C. Capacitor C shares its large charge with the relatively small capacitor B. Alternatively, when the on-chip bus is driven low, the NMOS transistor shorts capacitor B. The NMOS transistor also places Capacitor A (with no initial charge) in parallel with the pre-

charged capacitor C. Capacitor C shares its large charge with the relatively small capacitor A.

The worst-case on-chip Vdd drop can be estimated by:

$$VddDrop = Vdd \cdot \frac{C_{load}}{C_{load} + C_{decouple}} \quad (1)$$

The worst-case Vdd drop assumes that no current is supplied by the power leads while the transistors are switching (the digital transition time is zero). In the physical circuit, the digital switching will occur in a finite amount of time that will allow some charging current to be supplied by the digital power rails. Therefore, the slower the digital transition time, the lower the on-chip Vdd drop.

Given that C_{load} is much less than $C_{decouple}$ the equation shows that the on-chip Vdd drop is roughly proportional to C_{load} and inversely proportional to $C_{decouple}$. Since the capacitive load is larger on the rising edge (B is larger than A), the charge sharing on the rising edge will cause a larger on-chip Vdd drop. Using this equation, the worst-case test chip Vdd drop for the rising and falling edges are 59.7mV and 16.9mV respectively. With transition times of approximately 2.5ns the simulations show drops of 50mV and 15.2mV respectively.

7.3. On-Chip Bus Driver Noise without Digital Bulk Biasing

When the digital Vss is not connected to the bulk, the effective decoupling capacitance is greatly diminished (Figure 11). Also, disconnecting the digital Vss from the bulk complicates the discharge of capacitor B on the falling edge. The capacitor is no longer shorted by the NMOS transistor. For the following switching noise analysis, the 1.5% bus load to the digital Vss is ignored to simplify the description. The bulk is biased by either Analog Vss or a Kelvin contact (non-power carrying Vss).

When the bus load is driven high, the PMOS transistor shorts capacitor A. The PMOS transistor also places capacitor B (no initial charge) in parallel with precharged capacitor C and the series capacitance D and E. Since the Nwells provide the largest capacitance (five times larger than both the interconnect and the source junction capacitance), the effective decoupling is only slightly less than with the digital bulk biasing. Therefore, the rising edge noise is approximately the same as with digital bulk biasing.

When the bus load is driven low, the NMOS transistor places precharged capacitor B in parallel with capacitor E (no initial charge) and the series capacitance D and C. Therefore, instead of shorting the charge as with digital bulk

biasing, the charge is shared with the other capacitors. Meanwhile, the NMOS transistor also places capacitor A (no initial charge) in parallel with precharged capacitor D and the series capacitance C and E. The effective decoupling capacitance is now greatly reduced because the large Nwell capacitance is in series with the smaller source junction capacitance. Therefore, on the falling edge without digital bulk biasing, there is noise created by discharging capacitor B and noise created by charging capacitor A.

Disconnecting the digital ground from the bulk barely effects the rising edge noise, but the falling edge noise is made much worse. Without digital bulk biasing, the falling edge noise is worse than the rising edge noise.

7.4. Digital CMOS I/O Bus Driver Noise

The switching noise created by I/O drivers is very different from the on-chip bus drivers. The difference is caused by larger drivers, less decoupling capacitance, and a series lead inductance with the capacitive board load.

The 16 bit DSP test chip does not have any significant decoupling capacitance between I/O Vdd and I/O Vss. Since the load of the I/O driver is coupled to the board ground, not to the on-chip rails, a decoupling capacitor on the I/O supply would not have the beneficial charge sharing effect that on-chip bus loads have. Since there is effectively no decoupling capacitance, the power rail voltage excursions will be larger. Smaller capacitive loads have faster transitions (larger di/dt) and more I/O supply noise (L di/dt).

The I/O supply noise will couple into the bulk through three significant pathways: Nwell capacitance, source-to-bulk capacitance, and ESD capacitance (Figure 12). The bulk noise is then coupled into the analog circuitry through similar mechanisms.

Figure 12 shows only a single bit of the bus driver. The worst case noise analysis should include all sixteen bits switching simultaneously. The sixteen drivers cannot be combined into a single driver because the combined output load would produce different noise frequencies and would lose the coupling terms between the I/O package leads.

It is possible that the large I/O rail noise could cause a junction diode to turn on. If I/O Vdd differs from digital Vdd by Vt, then the ESD diode between these nodes will turn on. Also, if I/O Vss drops below digital Vss minus Vt, the source-to-bulk junction diode will turn on. These diodes clamp the I/O rail noise, but will couple more high frequency noise into and out of the bulk. The test chip substrate noise simulations have voltage transients that nearly

reach the diode turn-on point. If a voltage transient exceeds the turn on point of a junction diode, it is necessary to have the junction diode (not just the junction capacitance) in the simulation.

8. Bulk Biasing in Mixed Signal Circuits

There is some dispute over the most effective way to bias the bulk in mixed signal circuits. Schmerbeck says that a dedicated Vss pin(s) tied to a backside contact is the most effective method to reduce substrate noise [3]. Extra packaging effort and expense can provide a very low impedance backside contact to ground. This will make the p+ buried layer act as a "pseudo-ground plane." Schmerbeck describes the difficulty and expense in using a backside contact- the wafer must be backside ground to less than the skin depth for the entire the noise frequency range and the contact pad must be metallized. Finally, the backside contact must be attached to the bulk ground through a very low inductance connection. This requires a special package and additional PC board attach difficulty.

The 16 bit DSP test chip has significant substrate noise up to the gigahertz range. The skin depth of the p+ buried layer at one gigahertz is approximately 150 microns. Due to fragility, the minimum mechanical thickness of the substrate is 200 microns. Therefore it is not possible to thin the wafer to the necessary thickness to achieve the "pseudo-ground plane".

Top-side contacts should provide nearly as good a connection to the p+ buried layer as the backside, without the extra trouble or expense. However, without the low impedance bulk biasing lead, the bulk will not act as a "pseudo-ground plane." Although the top-side contacts will have slightly higher resistance to the p+ buried layer due to the epitaxy, the large number of bulk contacts will reduce the effective resistive to the p+ buried layer to a negligible value.

Schmerbeck claims that a dedicated bulk biasing pin (Kelvin pin) is the best option since it doesn't require either the analog or digital ground to be tied resistively to the bulk. However, the test chip simulations of substrate and power rail noise caused by on-chip drivers (Table 2) show contradictory results. Removing the digital resistive connection to the bulk greatly increases the digital switching noise, and thereby increases the total noise coupled to the bulk. When the digital ground is connected to the bulk, the large Nwell junction capacitance helps to decouple the digital switching noise. In the test chip, disconnecting the digital bulk contacts reduces the effective decoupling capacitance by a factor of three.

Schmerbeck also claims that the next best alternative is to bias the bulk with the analog (non-switching) ground. Using the analog ground to bias the bulk will reduce the body effect in the analog circuitry. However, this is the worst alternative for the 16 bit DSP test chip. The large bulk noise caused by the reduction in the digital decoupling effectiveness is now coupled directly into the analog ground. The best alternative for the test chip is to bias the bulk with both the analog and digital ground. This keeps the digital noise quieter, reduces the bulk impedance, and reduces the body effect in the analog circuitry.

There are two significant design differences between Schmerbeck's chip and the test chip. First, Schmerbeck's mixed signal chip area appears to be about 50% digital and 50% analog. The 16 bit DSP test chip is 99.5% digital and 0.5% analog. Second, Schmerbeck's chip uses an added digital rail decoupling capacitor that is much larger than the Nwell capacitance. The large decoupling capacitor and the smaller amount of digital circuitry make removing the digital bulk connection a viable alternative. His chip doesn't see the explosion in digital switching noise when the digital ground no longer biases the bulk.

9. Simulation Results and Discussion

9.1. On-chip bus switching

Figure 8 shows a transient simulation for on-chip bus switching with only digital bulk biasing. Similar circuit simulations were performed for various bulk biasing configurations to determine which configuration caused the least amount of analog rail noise (Table 2). The dedicated bulk pin simulation uses an additional modeled Vss lead and Kelvin contacts (non-power carrying) to bias the bulk [3]- none of the chip Vss supplies are tied resistively to the bulk. The "Single Supply" simulation shorts analog Vdd to quiet digital Vdd and uses both Vss supplies to bias the bulk.

This type of transient simulation is not as thorough as an analysis of the noise frequency sensitivities of the analog circuitry. However, the transient simulation does show the most significant noise frequencies generated and how this noise couples into the bulk and the analog rails. With this information the designer can estimate the frequency

and magnitude of the bulk and power rail noise. The designer is then able to select analog circuit configurations that are less sensitive to this type of noise.

For on-chip switching on the 16 bit DSP test chip the best bulk biasing strategy is digital biasing only. However, this is not the case for I/O switching (explained in the next section). Disconnecting the digital Vss from the bulk causes a large increase in digital rail noise and an increase in the bulk noise. This is caused by decreased digital rail decoupling. Connecting the analog Vss to the bulk increases the noise coupling into the analog rail. Although the analog rail noise is the smallest with only the digital bulk biasing, it should be noted that the body effect will be more significant since the analog source does not follow the bulk.

9.2. I/O Bus Switching

Simulations were performed for substrate noise caused by I/O switching with two bulk biasing alternatives: 1) digital only and 2) both digital and analog. Figure 13 shows the transient analysis with digital and analog biasing. All signals except the last three are with respect to board ground. The peak voltage deviations for each plot are labeled. The I/O Vss high frequency noise on the falling edge causes the most noise in the analog circuitry. The cause of the high frequency spike in the I/O Vss plot has not been determined. Table 5 shows the results of the I/O bus switching simulations. The last column is a simulation with an added one nanofarad analog rail decoupling capacitor. The effect of this capacitor can be viewed in two ways. First, it lowers the resonance frequency of the analog Vdd node. Second, it allows the analog Vdd to follow the analog Vss. Figure 14 shows a transient analysis with an added 2nf analog rail capacitor. Notice the lower resonance frequency of the Analog Vdd node. Also, notice that Analog Vdd tracks Analog Vss. To effectively decrease the analog rail noise, this capacitor must be much greater than the analog Nwell junction capacitance (~5pf for the test chip). Larger analog rail decoupling capacitors can further reduce the analog rail noise (Table 3).

10. Conclusions

A substrate noise simulation was developed and applied to a new 16 bit DSP chip design. It was shown that a complex substrate mesh extraction is not necessary for a first order simulation in a low resistive epitaxial process. However, the package and power rail parasitics play a significant role in the analysis. Modeling the package and chip-wide power rail parasitics allows the designer to see the effects of ground bounce induced noise, bulk biasing

alternatives, digital switch decoupling, and power rail and bulk resonance.

It was determined that the 16 bit DSP test chip bulk resonance frequency was much higher (~5X) than the digital switching frequency. Therefore, the chip should not see the adverse effects of increased substrate noise caused by high bulk impedance at the resonance frequency.

It was also determined that the worst case substrate noise in the test chip is caused by I/O switching- an order of magnitude larger than on-chip bus switching. With the I/O switching noise source the substrate noise coupled into the analog rail circuitry was minimized by biasing the bulk with both the analog and quiet digital Vss supplies. Designs with a greater percentage of analog circuitry will likely find the least noise when the bulk is biased with only the analog Vss or with Kelvin contacts (non-power carrying Vss).

The simulations also showed that an on-chip analog rail decoupling capacitor can be used to significantly reduce the analog rail noise. To be effective this capacitor has to be much greater than the parasitic analog Vdd to Vss capacitance.

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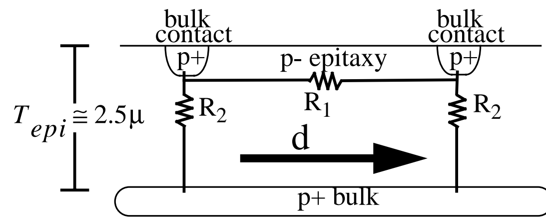

Fig. 1. Low resistive bulk epitaxial process

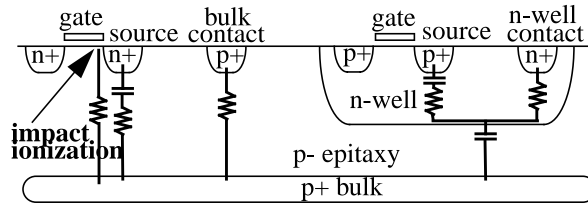

Fig. 2. Digital-to-bulk coupling mechanisms

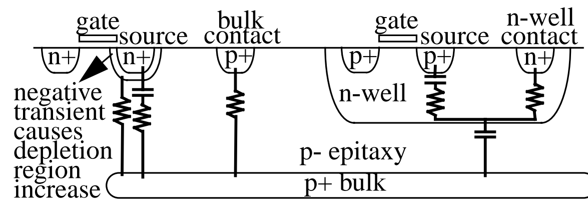

Fig. 3. Bulk-to-analog coupling mechanisms

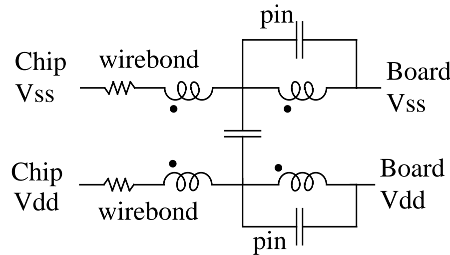

Fig. 4. Package pin subcircuit

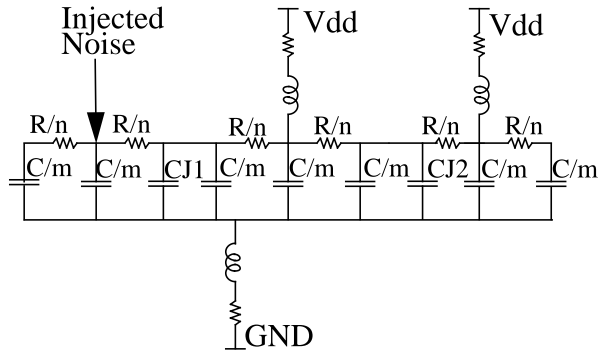

Fig. 5. Complex model of distributed power rail parasitic capacitance

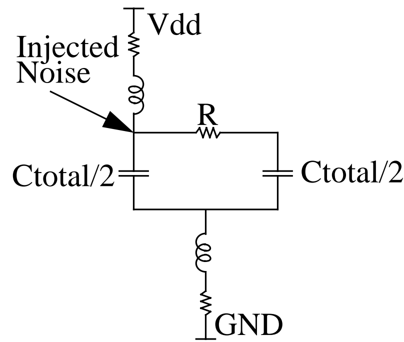

Fig. 6. Lumped pi model of power rail parasitic capacitance

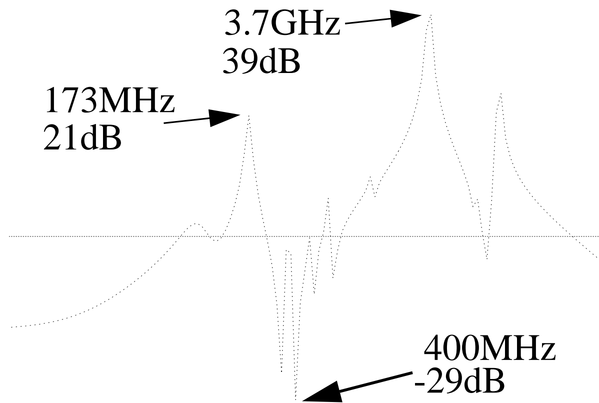

Fig. 7. 16 bit DSP test chip bulk impedance

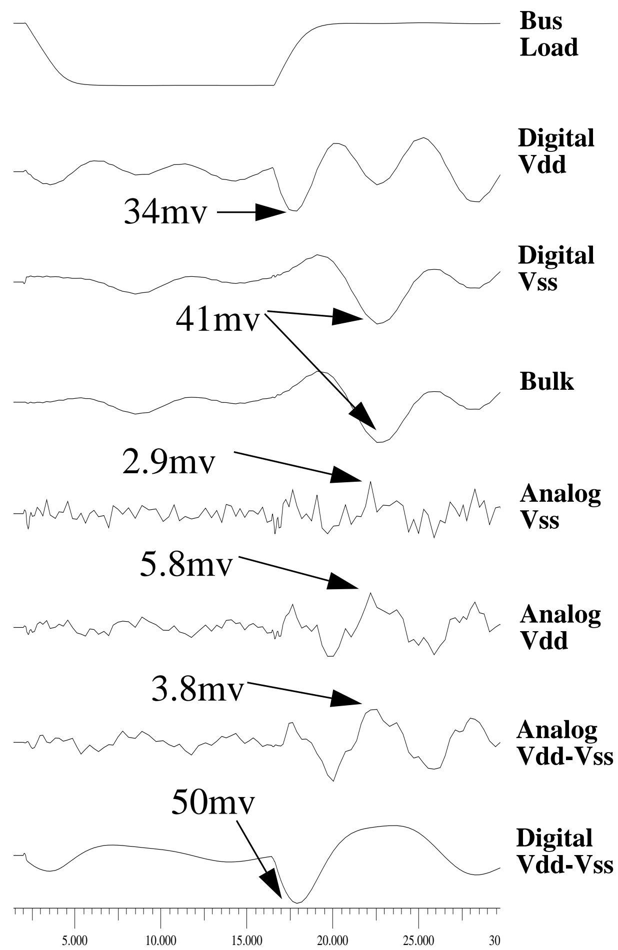

Fig. 8. 16 bit DSP substrate noise caused by on-chip switching

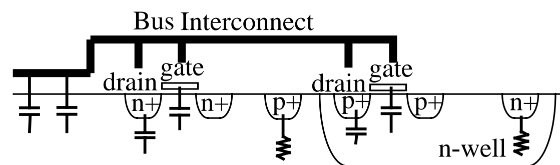

Fig. 9. On-chip bus load

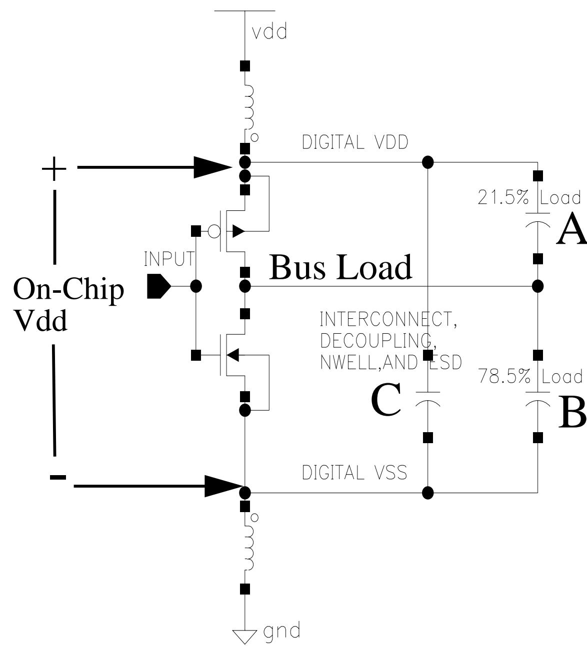

Fig. 10. Digital decoupling capacitor and on-chip bus load for 16 bit DSP with digital bulk biasing

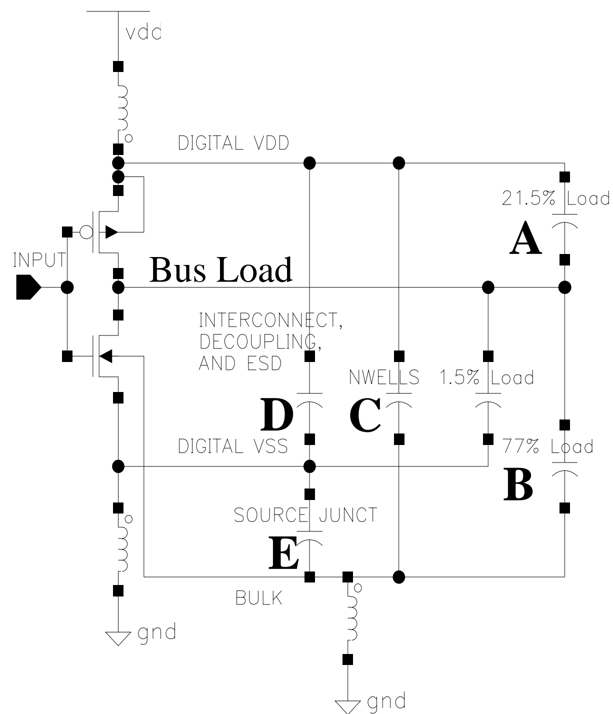

Fig. 11. Digital decoupling capacitor and on-chip bus load for 16 bit DSP without digital bulk biasing

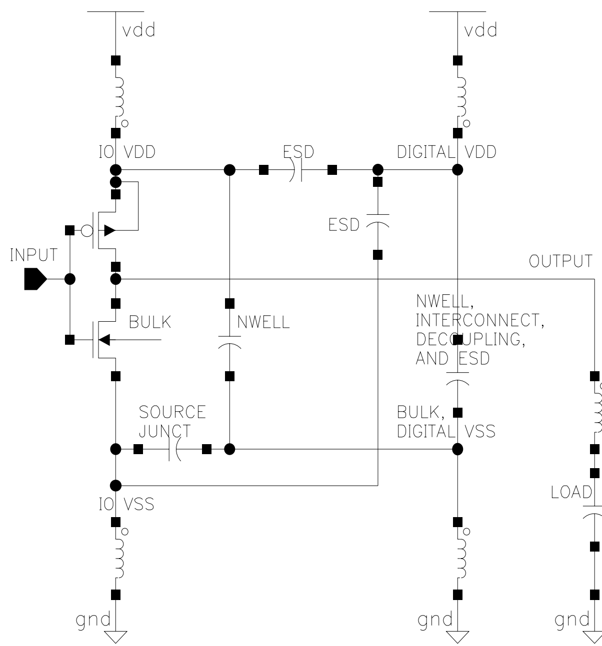

Fig. 12. Partial schematic for substrate noise from I/O bus switching for 16 bit DSP

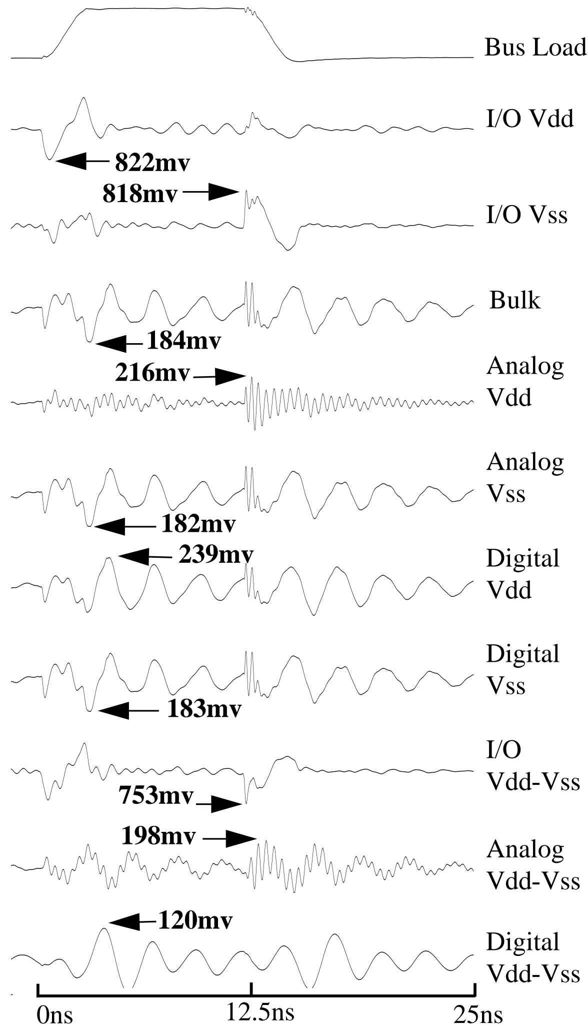

Fig. 13. 16 bit DSP with analog & digital bulk biasing substrate noise caused by I/O switching

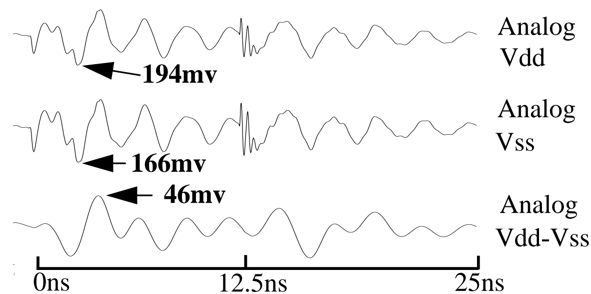

Fig. 14. Noise caused by I/O switching for 16 bit DSP with analog and digital bulk biasing and 2nf analog rail capacitor

Table 1. On-chip Bus Load in 16 bit DSP

Type of Capacitance	Connected To	Percent of Load
Interconnect	Bulk	70.0
P Junction	Vdd	17.5
N Junction	Bulk	7.0
Gate	Vdd	4.0
Gate	Bulk	1.5

Table 2. Peak voltage deviation caused by on-chip bus switching for bulk biasing conditions (mv)

	digital	both	analog	Kelvin	single supply
digital Vdd	34	43	78	73	33
digital Vss	41	36	80	80	41
digital Vdd-Vss	50	53	102	102	46
bulk	41	35	60	62	40
analog Vdd	5.8	11	19	11	41
analog Vss	2.9	35	59	3.4	46
analog Vdd-Vss	3.8	25	43	8.7	40
analog Vss-bulk	0.006	0	0	0.01	0

Table 3. Peak voltage deviation caused by I/O bus switching for analog decoupling capacitances (mv)

Vdd-Vss	None	250pf	1nf	2nf	3nf
I/O	753	705	706	717	706
Quiet	120	102	99	101	102
Analog	198	147	94	46	31

Table 4. Process and Packaging Information

Parameter	Value
Process	CDR1
Gate Oxide Thickness	90Å
Minimum Channel Length	0.4u
Metal Layers	3
Nominal Vdd	3.0v
Worst Case Vdd (used in sims)	3.6v
Package	100 TQFP

Table 5. Peak voltage deviation caused by I/O bus switching for bulk biasing conditions (mv)

	Digital	Both	Both with 1nf analog decoupling
I/O Vdd	808	822	829
I/O Vss	797	818	791
Bulk	206	184	161
Analog Vdd	377	216	220
Analog Vss	243	182	162
Digital Vdd	254	239	212
Digital Vss	205	183	161
I/O Vdd-Vss	740	753	706
Digital Vdd-Vss	153	120	99
Analog Vdd-Vss	342	198	94

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