Mahesh Chandramouli Shastry

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Department of Electrical and Electronics Engineering,
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(Formerly called Karnataka Regional Engineering College, Surathkal)

Areas of Interest

Digital Signal Processing, Information Theory, Data Compression and Video Codecs, Embedded Systems, Nonlinear Systems and Chaos Theory

Academic Background

- Currently in 8^{th} Semester (4^{th} Year) in **B.Tech** degree program.
  - ➢ B.Tech CGPA 7.63/10 (till 6^{th} Semester)
- ETS Scores
  - ➢ GRE : 730/800 (Verbal), 800/800 (Quantitative), Writing Score - 6/6;
  - ➢ TOEFL iBT: 106/120;

Publications

- *M C Shastry, N Nagaraj, P G Vaidya*, **The B-Exponential Map: A Generalization Of The Logistic Map And Its Applications In Generating Pseudo-Random Numbers**, *Arxiv.org Preprint Archive arXiv:cs.CR/0607069 v1 14 Jul 2006*
  Abstract
  Full Text

  *Abstract:*A 1-dimensional generalization of the well known Logistic Map is proposed. The proposed family of maps is referred to as the B-Exponential Map. The dynamics of this map are analyzed and found to have interesting properties. In particular, the B-Exponential Map exhibits *robust chaos* for all real values of the parameter $B \geq e^{-4}$. We then propose a pseudo-random number generator based on the B-Exponential Map by chaotically hopping between different trajectories for different values of B. We call this BEACH (B-Exponential All-Chaotic Map Hopping) pseudo-random number generator. BEACH successfully passes stringent statistical randomness tests such as ENT, NIST and Diehard. An implementation of BEACH is also outlined.
- *M C Shastry, N Nagaraj, P G Vaidya*, **A Generalization of the Logistic Map and Its applications in Generating Pseudo-Random Numbers**, accepted for presentation at *International Conference on Mathematical Modelling and Computer Simulations 2006, Jaipur, India Dec.* 12^{th} - 17^{th}

Projects

- **Control of Brushless DC Motor using Digital Signal Processor DSP56F805, Ongoing**
- **The B-Exponential Map: A Generalization Of The Logistic Map And Its Applications In Generating Random Numbers:** We came up with a continuous unimodal iterative map which exhibits the phenomenon of robust chaos, characterized by the absence of attracting periodic orbits for an infinite number of values of the parameter. This is a counter example for

the conjecture made in 1999 by Yorke, et al. We used this property of robust chaos to come up with a pseudo-random number generator(PRNG). This PRNG passes some of the most stringent statistical randomness tests.
Advisor: **Prof. P G Vaidya,** *School of Natural Sciences, National Institute of Advanced Studies, IISc Campus, Bangalore.*
Abstract
Full Text

- **VLSI Design of 8-bit Multiply-Accumulate Unit with sign extension(ongoing):** This project is a part of the VLSI course work. I have to design the integrated circuit layout, using MAGIC Layout editor, of an 8-bit multiply-accumulate unit. The design is to be tested using SPICE. We are using a Braun Multiplier with modifications for accommodating signed arithmetic. The result is to be stored in a 24-bit register, with 9 guard bits.

- **Analysis (time-frequency) Of Signals From INSAT-3A To Determine Its Velocity Along The Line Of Sight:** INSAT-3A is a geo-synchronous satellite. We subjected signals from INSAT 3-A to time-frequency analysis to determine its "wobble" velocity along the line of sight. The rate of change of phase of particular frequencies over time is related to the speed of the satellite along the line of sight (Doppler Effect).
Advisor: **Prof. C R Subrahmanya,** *Radio Astronomy Lab, Raman Research Institute, Bangalore.*
Report

- **A Mathematica Module Demonstrating Image Compression Using DCT:** The Electrical Department had newly acquired the Mathematica Package. This project involved learning and eventually writing a small introductory tutorial to Mathematica. Along with the tutorial, I wrote a Mathematica module to demonstrate image compression using DCT.
Advisor: **Prof. Jora M Gonda,** *Department of Electrical and Electronics Engineering, NITK Surathkal.*

Relevant Courses

Course	Grade	Course	Grade	Course	Grade
Digital Signal Processing	AB	Embedded Systems	AB	Signals and Systems	AB
Micro-processors	BC	Concrete Mathematics	AB	Data Structures and Algorithms	AA
VLSI	*Awaited*	Graph Theory	BB	Linear Algebra	BB

Computer Proficiency

Languages, scientific computing and simulation software:
C , MATLAB , SPICE, MAGIC, Assembly Level 8051, Mathematica.

Operating Systems:
Linux, Embedded Linux, Windows NT and XP.

Work Experience

- **Summer Intern:** (2006 May-Aug) School of Natural Sciences,
National Institute of Advanced Studies, Indian Institute of Science Campus, Bangalore.

- **Summer Student:** (2005 May-Aug) Radio Astronomy Lab,
Raman Research Institute, Bangalore.

- **Convenor :** IEEE NITK Students' Chapter

- **Joint Convenor :** Engineer 2007, All India Tech-Symposium Conducted by NITK Surathkal

- **Secretary :** 2005-06, NITK Students' Union

Awards and Achievements

- **National Talent Search Scholar (NTSE) instituted by the National Council for Education, Research and Training, 2001:** This is a scholarship given by the Government of India to 1000 exceptional students from all over India who pursue studies in the field of Physical Sciences and Engineering. I was ranked 11th in the state of Karnataka.
- **Recipient of the Dirubhai Ambani Scholarship, instituted by the Dirubhai Ambani Foundation, 2003:** This scholarship is given to about 100 students from all over the country in recognition of their academic and other achievements from a fund set up by the late entrepreneur and philanthropist Dhirubhai Ambani.
- **Represented the state of Karnataka in the All India Prof. Brahm Prakash Memorial Materials Science Quiz, 2002**
- **Runners Up in National Level Matlab/VHDL/Hardware Design Contest held at NITK Surathkal as part of a national level tech symposium**
- **Ranked in the top 2.5% in the country in the IIT-JEE Examination for admissions to the Indian Institutes of Technology**

Personal Information

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