A CMOS RFID transponder

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Abstract

An implementation of a single-chip CMOS Radio Frequency Identification (RFID) transponder based on a 13.56MHz carrier system is presented. The 64-bit read-only RFID employs zener-zap one-time programmable ROM to store the ID. The design is optimized for a very low power operation maximizing the coupling distance between the transponder and the reader unit. The multi-access using anti-collision scheme is incorporated. The RFID transponder occupies 5.95 mm^2, consumes 42 μA of current and is fabricated using a 0.8μm double-poly double-metal CMOS process.

1. Introduction

The increased demands in premises security and electronic automation systems make identification system more important and necessary. Among many wide varieties of the electronic identification systems such as barcode and smartcard, the contactless smartcard system has many advantages over the other systems in terms of flexibility, robustness, ease of use, and reliability under different environmental conditions. Owing to the utilization of radio frequency signal for the transfer of power and data, the contactless smartcard system is typically called RFID system. The basic RFID system consists of two devices: reader unit and transponder unit. The reader contains a radio frequency module, control unit, and a coupling element to communicate (read or read/write) with the transponder. The transponder or tag, which represents the data-carrying device of the RFID system, is typically a passive or battaryless device and consists of a coupling element and ID generating module. The transponder operates by the energy supplied from the reader unit while, at the same time, sends back the ID via mutual coupling mechanism between their coils as shown in Figure 1. In this paper, an RFID transponder design targeted for a read-only object identification, such as animal ID or asset tracking ID, is presented. The transponder is implemented in a standard CMOS technology for the availability of a low-cost transponder. The details of the transponder design are described in Section 2. Section 3 shows simulation results from the design. And finally, the conclusion is given in section 4.

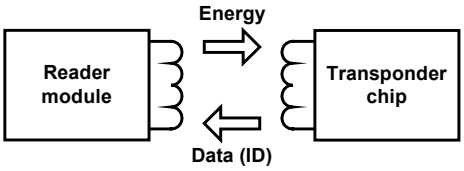

Figure 1. The reader and the transponder system.

2. The Transponder Design

Figure 2 shows a block diagram of the proposed transponder. The transponder is divided into two sections: (I) RF interface section and (II) Baseband section. The RF interface consists of analog circuits that performs power conversion through a full-wave rectifier and extracts the system clock from the incoming RF signal. The data from the Baseband section corresponding to a unique ID from the one-time PROM is encoded and sent back to the reader via a load modulation scheme. In this system, the

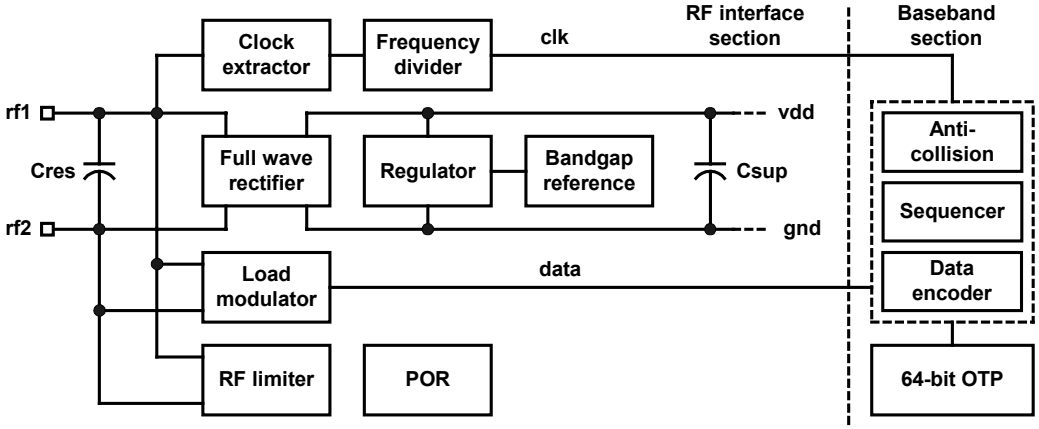

Figure 2. Block diagram of the transponder.

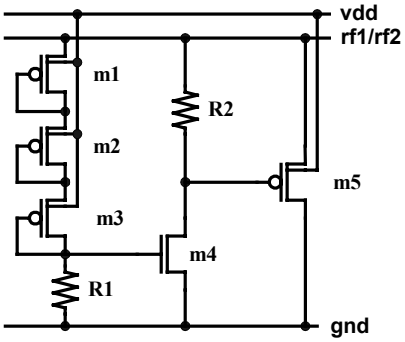

Figure 3. RF limiter.

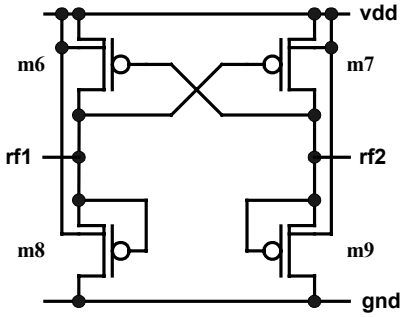

Figure 4. Full-wave rectifier.

transponder is designed to support multiple accesses with an Anti-collision feature. The RF resonant coupling elements use 13.56MHz signal as a carrier frequency. The details of each sub block in the transponder are described below.

2.1 RF Interface Section

2.1.A RF Limiter

In order to protect damages caused by CMOS gate-oxide breakdown due to an excessive coupling voltage from the reader for a shot distance operation, the RF limiter in Figure 3 [1] is utilized. The limiter senses the RF signal on both sides of the pins, rf1 and rf2, by stacked diode voltage referenced to ground (substrate) of the chip. When the instantaneous incoming RF signal is larger than this voltage, the limiter's shunt PMOS, m5 is turned on, hence, reducing the effective load of the resonator.

2.1.B Full-Wave Rectifier

A rectifier, where the employed circuit shown in Figure 4, is used to convert the RF signal for the entire system power supply. A full-wave rectification is accomplished by using a PMOS bridge circuit [2]. The PMOS bridge is chosen to avoid the creation of a latch-up during an inevitable small forward bias of the drain-bulk junction. Transistors m8 and m9 are connected in a basic diode configuration while m6 and m7 are connected in a switching configuration. This arrangement helps reduce the voltage drop and minimize the forward bias of drain-bulk junctions in the devices.

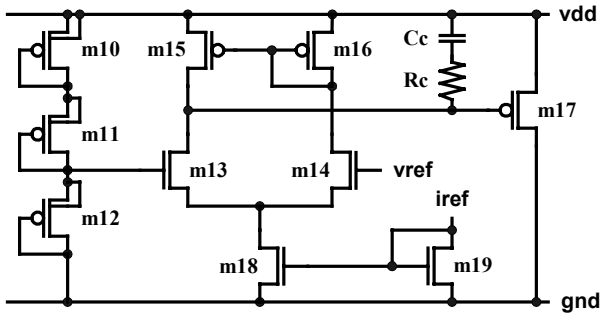

Figure 5. Supply regulator.

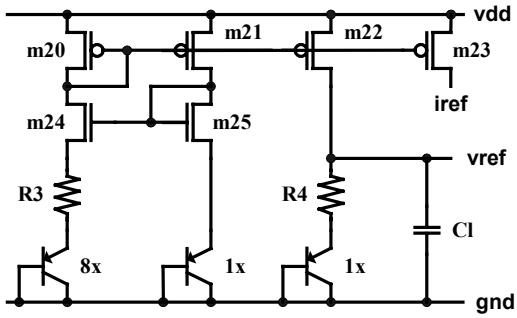

Figure 6. Bandgap reference.

2.1.C Power Supply Regulator

Because the power supply level is dependent on the mutual coupling voltage with respect to the distance of operation between the two coils, the supply level then can substantially reduce or increase by hand movement. The supply regulator aims to remove a low-frequency power-supply voltage variation and to stabilize the voltage to a constant level for the entire chip usage. The regulation scheme functions similarly to the RF limiter. It compares the supply sensing voltage derived from a portion of the vdd with the bandgap reference voltage, and controls the effective load of the regulator shunt's PMOS, m17. The different of these two schemes, however, is that the regulator requires a low bandwidth to suppress the hand movement effect and allows load modulation to occur without attenuation, while the RF limiter must be able to operate at the carrier frequency.

2.1.D Bandgap Reference

The reference voltage sets the global power supply voltage and vref is derived from a low-power bandgap reference in Figure 6. This circuit offers a temperature-independent reference voltage and a reference current for biasing the power supply regulator circuit. The bandgap voltage is set at 1.2 volts.

2.1.E Clock Extractor & Frequency Divider

The transponder's clock is readily acquired by using the RF signal as an input clock. A simple wave shaper circuit such as a Schmitt trigger inverter as shown in Figure 7 is therefore sufficient for the clock extraction function. The extracted clock is subsequently divided by a factor of 32

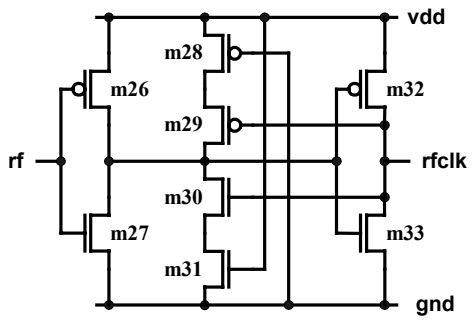

Figure 7. Schmitt trigger inverter.

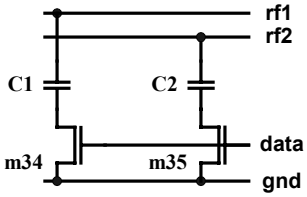

Figure 8. Load modulator.

in order to minimize the Baseband power utilization. The frequency divider is simply constructed by using standard D flip-flops arranged as a divide-by-32 ripple counter.

2.1.F Load Modulator

The transmission of the returned ID data from the transponder to the reader unit is achieved by using a capacitive load modulation technique as shown in Figure 8. The additional capacitors C1 and C2 during 1-logic data detune the resonant frequency only slightly to create a discurved envelope voltage across the resonant circuit at the reader unit. The reader then can discriminate the envelope by demodulating and processes the ID data.

2.2 Baseband Section

2.2.A Sequencer & Data Encoder

The sequencer and the data encoder provide signals to address the memory array and to encode the output data, respectively. The data is composed of a 9-bit header, 88-bit raw data (64-bit programmable, 24-bit constant), a 16-bit checksum and a 1-bit trailer as shown in Figure 9. For every byte of the raw data and the associated checksum, the stuffing bit (0-logic) is also inserted to avoid the chance of the "111111111" header pattern duplication. Before transmission, all bits are coded in Manchester coding format. The coding data rate is at 69.89 kbit/s and thus requires 1.8 ms for one complete transmission.

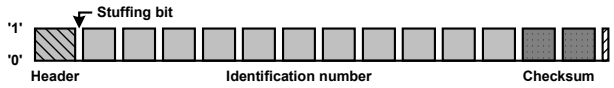

Figure 9. Data structure.

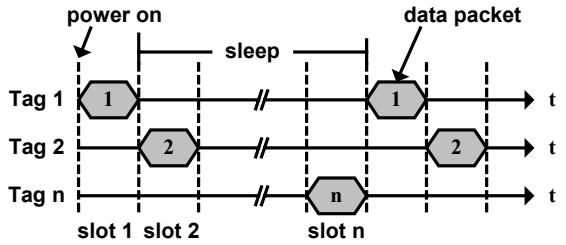

Figure 10. Anti-collision scheme.

2.2.B Anti-collision

In order to read multiple transponders simultaneously, the Anti-collision feature presented in Figure 10 is applied. The transponder starts transmission of the data packet after receiving its power in a different time slot selected randomly by each ID itself, then goes into sleep mode after sending a data packet. Because a 100ms sleep interval is inserted between each ID transmission, more than 32 transponders can be read concurrently in the same field. Though the maximum of the transponder could also depend on the environment factor.

2.2.C One-Time PROM

The 64-bit one-time PROM (OTP) is constructed by a zener-zap technology which provides an opportunity for programming an OTP at waferprobe or in-the-field programming after chip packaging. The OTP requires two dedicated external power input pin for each of 32-bit OTP in order to program the ID data.

3. Simulation Results

The prototyped transponder is designed in a 0.8μm double-poly double-metal CMOS technology. Figure 11

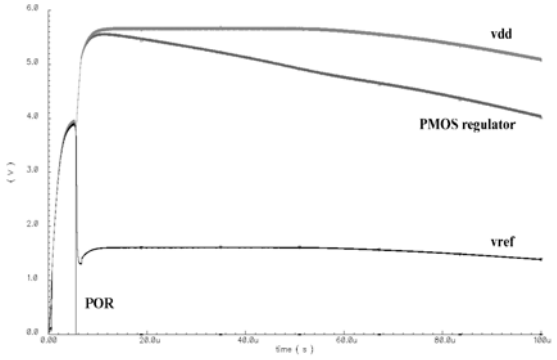

Figure 11. RF interface unit response after power on.

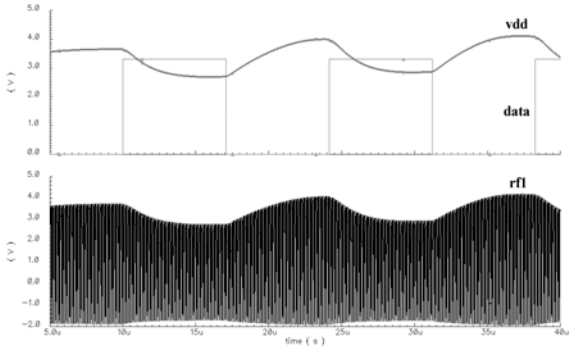

Figure 12. RF interface unit response while modulation.

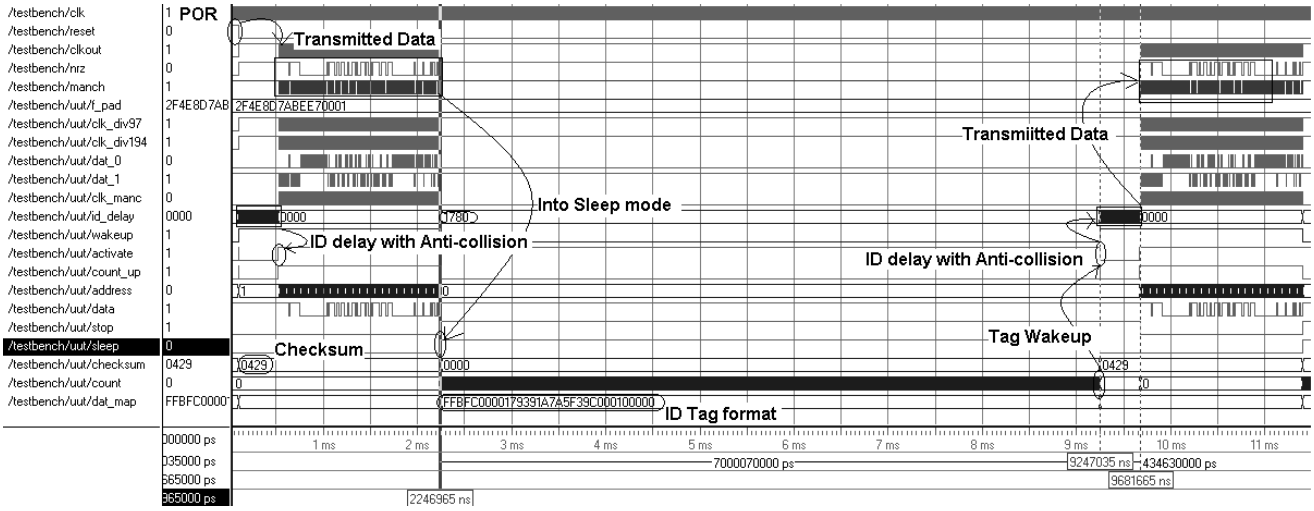

Figure 13. Timing diagram of the Baseband unit operation.

shows the simulation results of the RF interface section at the beginning when the transponder is entering the field. First, the power-on reset starts up and lasts for a few microsecond. Once the reset is inactive, the power supply rises to the limited voltage set by the RF limiter. Note that the supply regulator does not response for stabilizing the power supply yet because of its low bandwidth. The power supply decreases to a certain level in a few hundred microsecond when the supply regulator enters the operation. The level of modulation depends on the detuning range of the carrier frequency, however, this effect will also cause the power supply to track that of the transponder vdd's ripple due to the modulating data as shown in Figure. 12. Therefore, the supply filtering capacitor must be chosen by steering a compromise between the power supply ripple and modulation level (or modulation index).

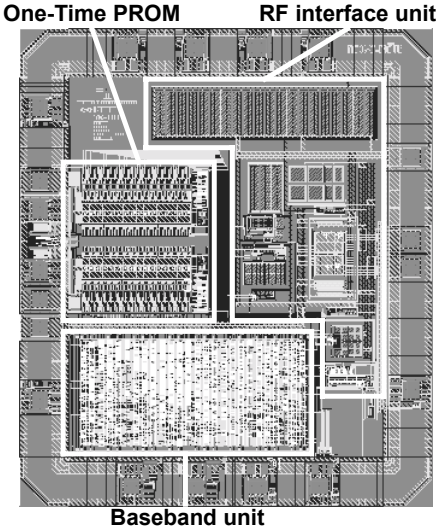

Figure 14. The RFID transponder chip's layout.

The timing diagram of the Anti-collision scheme is illustrated in Figure 13. The time slot delay and the sleep mode period are down scaled for compact simulations. The total transponder chip area is 5.6 mm^2 and approximately consumes 42 μA of current.

4. Conclusion

The design and implementation of a single-chip read-only RFID transponder has been described. The ID of each transponder is set by using 64-bit one-time PROM. The transponder chip is implemented in a standard 0.8μm double-poly double-metal CMOS process. An anti-collision feature is built in for multi-access capability. The transponder is designed to utilize low power consumption in order to maximize the distance of operation.

5. Reference

[1] U. Kaiser and W. Steinhagen, "A Low-Power Transponder IC for High-Performance Identification Systems", IEEE J. of Solid-State Circuits, Vol. 30 No. 3, March 1995, pp. 306-310.

[2] P. Rakers, L. Connell, T Collins, and D. Russell, "Secure Contactless Smartcard ASIC with DPA Protection", IEEE J. of Solid-State Circuits, Vol.36, No. 3, March 2001, pp. 559-565.

[3] Application Note: Easyzapp, Austria Mikro Systeme, Austria, August 1999.