Plasma Induced Wafer Surface Voltage and Its Electrochemical Corrosion in Tungsten Plug Process

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Abstract

It has been reported that occasionally Tungsten plug core can be electrochemically corroded after metal etching and solvent stripping. The reason is possibly due to an electrical charging phenomenon. This has brought up concerns for misaligned contacts and vias. In this report we have investigated the effects of etching parameters on Tungsten plug loss. Plasma source power, gas flow ratio, pressure and bias power were varied in this experiment. The plasma potential and the plug loss level were measured. The results show similar trends between plasma potential and W plug loss

Introduction

Tungsten (W) plug is often used in multilevel interconnect structures such as contacts and vias. It has been reported that under certain circumstances severe W plug loss occurs after post-metal etch treatment [1,2]. Fig.1 shows an example in which the entire W plug disappears after solvent stripping. Researchers have reported that the electrochemical potential causes the dissociation of W and AlCu metals, and this electrochemical potential can be induced by plasma charges on specific metal patterns.

In this study we have investigated the effects of wafer surface voltage on the W plug loss. This surface voltage, called Vdc, is built up inside an etching chamber to perform anisotropic etching. Its magnitude and uniformity depends on process condition. Important parameters include plasma source power, chemical gas flow ratio, pressure and bias power. These parameters were varied in this experiment to check the effects of surface voltage on the W plug loss. The level of W plug loss correlates well with via resistance.

Experiment

In the experiment double metal test structures were used. First metal layer, via and W plug were formed by conventional 0.25 μm technology on the test wafers. After W plug formation the second metal layer was deposited with Ti/TiN/AlCu/Ti/TiN stack, the second metal layers is then patterned with coated BARC and DUV photoresist. A commercial metal etcher from Applied Materials was used to carry out all the etching experiments. This etcher has a decoupled plasma source (DPS) with independent ion flux and energy control [3]. Due to its large process latitude we can select a wide range of process parameters to monitor the effects easily. Inside the etcher the plasma potential Vpp was recorded. Vpp is the peak to peak potential between the ground electrode and the wafer. It can be related to Vdc by the following equation:

$$Vdc \sim -0.29\ Vpp \qquad (1)$$

A three level L9 design experiment is adopted. Variations were made on the source power, Ws, with power level of 600W, 1200W, 1800W, the chamber pressure, P, with pressure level of 6mT, 12mT, 18mT, the Cl_2/BCl_3 gas flow ratio with ratio level of 60/60 sccm, 80/40 sccm, 90/30 sccm and the bias power, Wb, with power level of 100W, 200W, 300W.

The wafers after etching process were stripped with commercial EKC 270A solvent for 30 min. and then the exposed W plugs (when metal layer is misaligned) were examined by in-line SEMs to check the extent of W plug loss caused by an electrochemical reaction. The value of via resistance was also measured.

Results and Discussion

The results show that Vpp, W plug loss and via resistance have similar trends. In order to determine the effects of each parameter on the W plug loss, we have divided the extent of plug loss into five levels, as shown in Fig.2. Table.1 shows the levels of each parameter and its effects on Vpp and W plug loss. After calculation, the effects of individual parameter were plotted in Fig.3. As shown in Fig.3, Vpp and W plug loss follow similar trends. Both Vpp and W plug loss level slightly increase with pressure, while decrease with Ws, Wb and gas ratio. Among the four investigated parameters, the source power Ws has the most significant impact on Vpp and W plug loss. Fig.4 shows via resistance as a function of plug loss level. It clearly indicates that the resistance increases dramatically with plug loss.

Also shown in table.1, most of the process condition has plug loss level below 4. Via resistance shows a satisfactory value at these levels. This indicates that this type of decoupled plasma source etcher has a wide process window.

Conclusion

In summary, the W plug loss is found to relate to the wafer surface voltage. According to the experimental result, lower source power, lower gas ratio of Cl_2/BCl_3, higher pressure and higher bias power will result in high tungsten plug loss and thus high via resistance. This is consistent with reported electrochemical charge potential models.

References

[1] S. Bothra, H. Sur and V. Liang ¡§A New Failure Mechanism b Corrosion of Tungsten in a Tungsten Plug Process¡¨. Annual International Reliability Physics Symposium, Reno Nevada, 1998. pp. 150 ~156.

[2] L. T. Koh, K. L. Chok, H. M. Li, and Y. M. Chool. ¡Titanium Corrosion in 0.25 µm Metal Interconnect ¡. International Interconnect Technology Conference, IITC99. pp. 47-49.
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Table.1: The arrangement of a L9 experiment and the obtained Vpp and W loss

	Ws (W)	Cl2/ BCl3 (sccm)	Pressure (mT)	Wb (W)	Vpp (V)	W Plug loss Level
L1	600	60/60	6	100	227	5
L2	600	80/40	18	300	624	4
L3	600	90/30	12	200	433	3
L4	1200	60/60	18	200	408	3
L5	1200	80/40	12	100	181	4
L6	1200	90/30	6	300	350	1
L7	1800	60/60	12	300	355	2
L8	1800	80/40	6	200	165	1
L9	1800	90/30	18	100	159	2

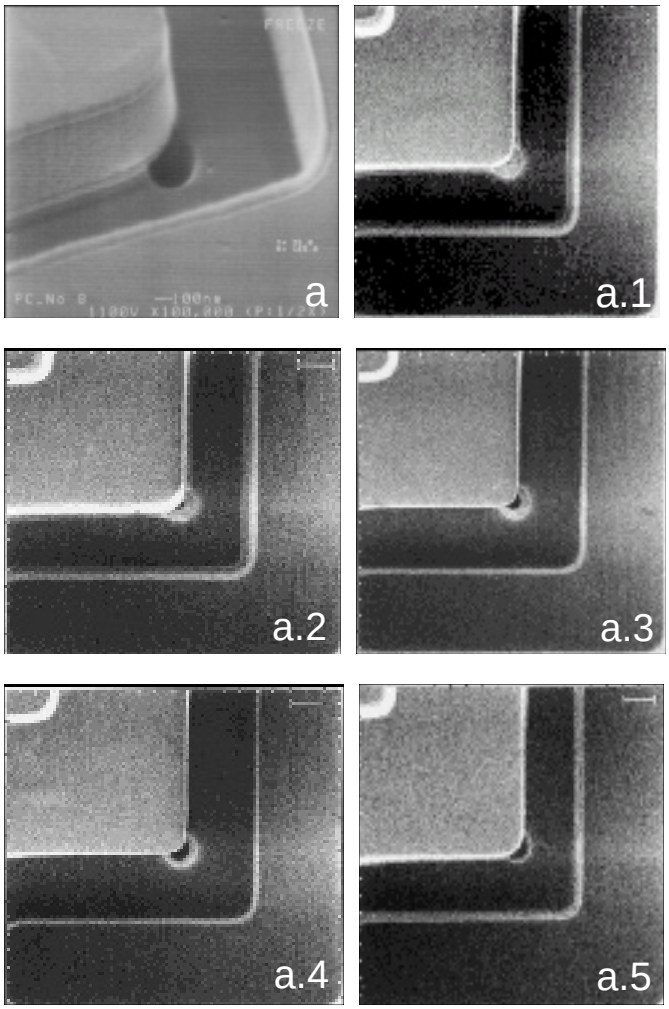

Fig.1: (a) An example of severe W plug loss after solvent stripping. (a.1)~(a.5) The extent of W plug loss divided into 5 levels from plug loss level 1 to 5.

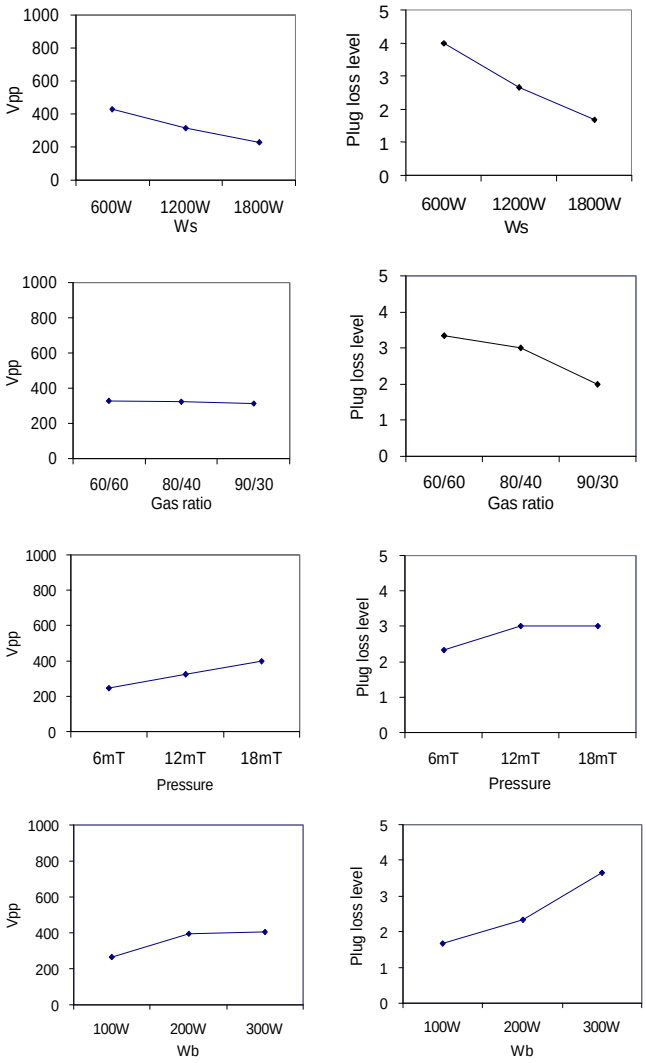

Fig.2: Individual etch parameter (Ws, gas ratio, pressure and Wb) effects on plasma potential and W plug loss.

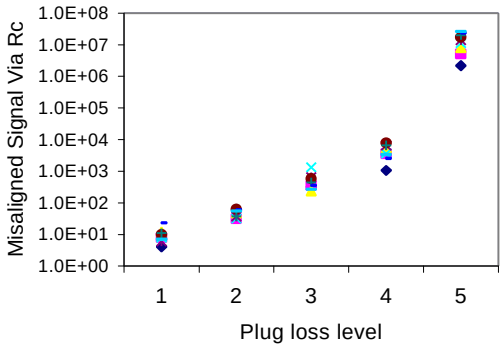

Fig.3: Electrical test result shows misaligned via resistance as a function of plug loss level.