A Novel Assessment of Process Control Monitor in Advanced Semiconductor Manufacturing: A Complete Set of Addressable Failure Site Test Structures

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Abstract ¡This work describes the implementation of a novel assessment of process control monitor in advanced semiconductor manufacturing. It manifests the design and simulation results of addressable failure site test structures. Four novel test structures with three level interconnects have been developed and validated with in-house simulation system. The novel test structures are used to identify the locations of killer defects used to wafer map defect sites. A test chip of 22x6.6 mm^2 containing four types test structures was implemented using 0.25 mm logic backend of line process. This simple and efficient test structure for killer defect identification demonstrated its superiority in yield enhancement.

I. INTRODUCTION

With the rapid expansion market of integrated circuit foundry service, typically, there are tens to hundred IC products per year coming out from a mass-production line, which apply more than two generations of technologies. The features of foundry manufacturing contribute to the complexity of process control monitor (PCM) and yield enhancement (YE). Moreover, the short life cycle and small wafer volumes of various products make it difficult for the foundry manufacturers to choose a typical and volume-leading product as the PCM vehicle. Therefore, it is essential to design a test chip for PCM as well as YE tools.

The design requirement of a test chip is to contain those structures for detecting random and systematic process problems, and short turn around time of problem solving[1]. Typically, SRAM is a common test vehicle for logic process development and yield analysis of mass-production line because SRAM has the features of high density and failure site addressable[2][3]. With the aid of software, the optical inspection defect data can map with failure bit map (FBM). By classifying the signature of FBM, the failure mode is characterized, the defective process steps could be identified, then precise site failure analysis could be performed to track down defect source. The systematic failure analysis method on SRAM test vehicle is used for all kinds of memory and field programmable gate array (FPGA). Thus, with the increasing chip size and the lowering defect density, it will be an optimal way by segmenting a test structure into memory-like structures so as to quickly ascertain the defect type and track back the defective process steps [4~9].

To provide a test structure which is short loop process compatible, provide maximum effective area and come with the minimum number of probe contact pads, we develop complete set of **a**ddressable **f**ailure **s**ite **t**est **s**tructures (AFS-TS).

II. TEST STRUCTURE DESIGN

For the convenience sake on model description, some graphic terminology has been adopted to model the geometry of layout objects inside a test structure. The nodes (**N**={$\mathbf{n}_1$, $\mathbf{n}_2$, $\mathbf{n}_3$ ¡ , $\mathbf{n}_N$}) stand for the measurement points with conductive layout objects (conductive unit [**CU**]) like comb or meandering lines. The line (**L**) describes the measurement path between two measuring pads, either short circuit check (SCC) or open circuit check (OCC). **L** = { $\mathbf{l}_{ij}$, i, **j** = **1**, **2**, **3** ¡ , **N** (a) if **i** 1 **j**, the $\mathbf{l}_{ij}$ means Short Circuit Check Unit (SCCU); (b) If **i** = **j**, the $\mathbf{l}_{ij}$ means Open Circuit Check Unit (OCCU); } The whole test structure is noted by **G** = **(N, L).** Hence, to achieve a precise localization of defect inside test chip means to access every node and identify faults inside the edges.

Fig. 1 shows the schematic layouts & their geometry graphs of typical test structures. The design concern of unit cell is correlated to the one of the critical process step and layers. The minimum design rule (MDR) is used for the design rule of unit cell. For isolated contact & stacked via chain, minimum spacing of contact & via are defined as five times of design rule. To ensure the lowest yield loss from interconnection of unit cell, the width & spacing of interconnection between unit-cells is 2~5 times MDR width & spacing. The resistance of unit-cell is extracted from the statistical measurement distribution of fault-free device so called golden device. Then, The unit cell of test chip is put into the common placement and routine. To validate the design of test structure, in-house simulator in Matlab 5.2 is programmed to extract the voltage & leakage current spatial distribution from test chip. With itinerating review on the simulation results and testing methods, an optimal testing method and structure are thus confirmed. The development flow for test structure design is shown in Fig. 2.

Based on this design methodology, four types of test structures were developed, named as 2D, XY, CON, and CON-Y, respectively, and their geometry graphs and chip layout are shown in Fig. 3, and Fig. 4. The unit-cells of 2-D test structure are arranged in 2-D permutation [7,9,10]. The unit cells of XY, CON, and CON-Y of test structures are placed into two orthogonal groups in X-direction, and Y-direction. In XY-type, the unit cells of X, and Y direction are electrically independent, but for CON and CON-Y, the unit cells of the X, and Y direction are electrically connected in X/Y and Y direction only, respectively.

The standard WAT 32-pins probe card is adopted for compatibility of WAT testing. Table 1 shows the comparison of total of unit cells inside the AFS-TS and the scale of test structures. The scale of test structure is much larger than typical logic chip, which is necessary to ensure high catching rate of random defects as well as systematic defects. The CON-type comes with the highest detection resolution in a limited chip area, which means the CON-type provides the most electrically fault detectable unit cells.

III. MODELING AND TESTING OF FAULT

The test structure is composed of unit cells modeled as resistors. Figure 5 shows the schematic graph of short-circuit model and measurement circuit configuration. R_{inf} represents leakage from measurement system. The defect-*M* caused short-circuit between *Node-I* and *Node-J* is modeled as Rs_{m-1}, and the resistance of *Node-I* and *Node-J* are labeled as $(R_{i-1} + R_{sm-2})$ and $(R_{j-1} + R_{sm-3})$, respectively. The resistance and location of defect are generated by random number generator.

The open circuit fault is defined that the resistance of unit cell is out of specification of golden devices. The measurement of open circuit is the standard WAT resistance measurement either to force I, then measure V, or to force V, then measure I. The short circuit fault is defined that the leakage current between nodes is lager than leakage current limitation dependent on the technology and process, for example in this work, $3.3*10^{-8}$ A at 3.3 V biased is used for 0.25 um backend of line (BEOL) process test structures. The open circuit measurement is performed in each node, and the short circuit measurement is done between all of nodes. The algorithm of single and multi electrical defect detection could be found in [9~10]. The short circuit defect can be located at the high leakage current site as shown in Fig. 6.

IV. EXPERIMENT AND DISCUSSION

A **t**riple-**l**ayer **m**etalization (TLM) systems of 0.25 um BEOL process is enacted to validate the AFS-TS. The set of AFS-TS contains the test structures of sheet resistance, via resistance, stacked via resistance, and the critical BEOL integration process, where contains 155 dies in a wafer. The wafer is fabricated on 200 mm p<100> silicon wafer deposited with a PE-oxide as buffer layer, Al-Cu(0.5%) metal and W-plug is used for via1 and via2, low-k Fluorine doped silicon glass(FSG) is for inter-metal dielectric-1(IMD-1) and IMD-2, and the IMD chemical/mechanical polish(CMP), and W-touchup CMP are used as planarization process. The deep UV lithography is done for each photo-layers, except pad layer by I-line lithography. For the cost concern, the multi-chip mask is used for 6 layers, where the metal-1, metal-2 and metal-3 for in one dark-layer mask, and Via-1, Via-2, and Pad in one clear-layer mask.

Process Optimization

As the test vehicle is introduced to manufacturing line with other products, the process condition such as lithography etching time, and CMP polishing time are not optimized, which the yield of period-1 shows the average yield loss is around 25 % compared with the fine-tuned process shown in period-3. As lithography process is optimized at perion-2, and CMP and etching process tuning is done at period-3, the yield is back to normal condition and the yield loss is contributed by random defects. The yield trend chart of test structures is shown in Fig. 7. The stacked borderless via test structure is used as optimization index of interconnection integration process. Both of yields of open circuit and short circuit are increased as process is fine tuned.

Failure Analysis of Root Process Killer

In view of the fact that the failure site of AFS-TS can be electrically detected by WAT, the testing result come with the detail of defect information such as site address and related process step. Therefore, either electrical or physical failure analysis at specific site can be performed and timely provide the root cause of process killer. Figure 9, and Figure 10 show the Metal3 continuity and bridging yield for two wafers, the normal and the abnormal processes, respectively. Figure 9 shows that the normal process (Wafer_ID=8) meets the process control limits both for continuity and bridging, but not in the abnormal process (Wafer_ID=2). Figure 9, 10 show the Metal3 sheet resistance in column, and row at the left hand-side and the right hand-side, respectively. The wafer map of sheet resistance in Fig. 9 shows that the center is slightly higher than the edge but still within specification. Figure 10 indicates that the failure is concentrated within the wafer center. Figure 11, and Fig.12 show the leakage current wafer map. Again, Figure 11 shows the center is slightly higher than the edge but still within specification. Figure 12 shows the short circuit failure at the right hand-side of wafer and low leakage at the wafer center, which is consistent with the wafer center preferring to open circuit failure.

V. CONCULSIONS

This above mentioned design methodology builds up a systematic design flow and a complete set of test structure of conductive layer and interconnection for process optimization. Defects information including site address, and related process step can be electrically characterized and located prior to physical failure analysis. With this approach, data can be quickly processed in a large volume, and the precise electrical defect density can be extracted as well. This system can thus provide a common manufacturing defect control tool in memory and logic semiconductor.

VI. REFERENCES

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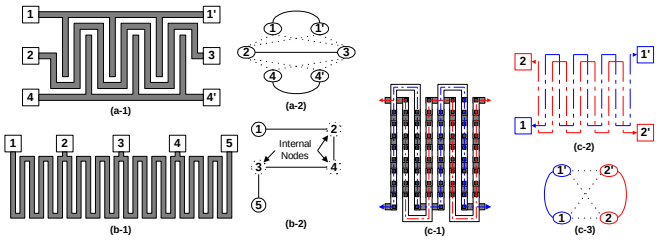

Fig. 1: Typical test structure and their geometry graphs. The solid line represents the conductive component and the dash line stands the possible leakage paths. (a-1), (b-1) Schematic layout of conductive layer. (a-2), (b-2) Geometry graph. (c-1) Schematic layout of Contact/Via chain. (c-2) Placement and routing. (c-3) Geometry graph.

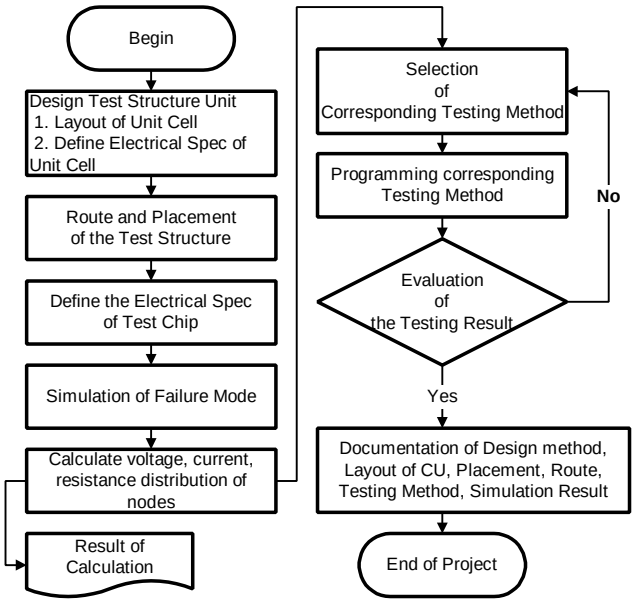

Fig. 2: The flow shows the development methodology of the novel test structure.

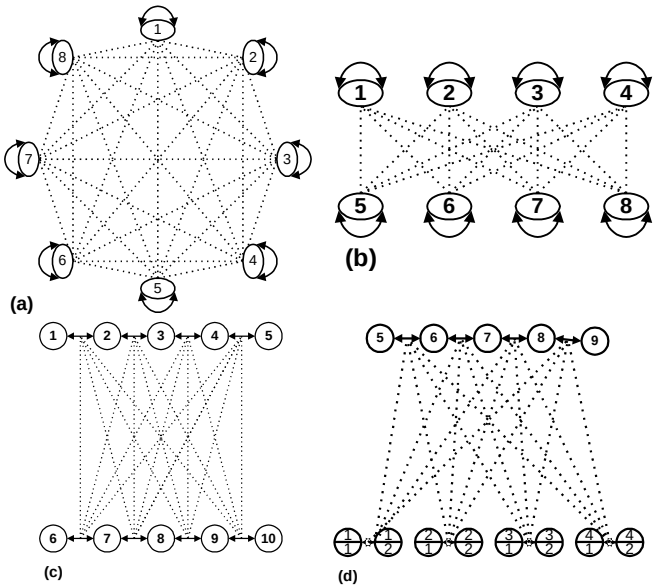

Fig. 3: Geometry graph of four types of test structure. (a~d) are 2D, XY, CON, and CON-Y, respectively.

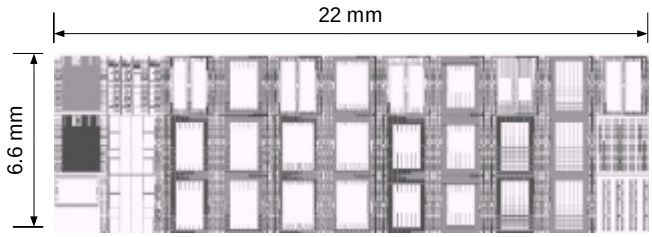

Fig. 4: Layout of four types of addressable failure site and PCM test structures.

Table 1: Comparison of total and scale of unit cells of four types of addressable failure site test structures.

Type AFS-TS / Type of Design Rule		2-D	XY	CON	CON-Y
M1	Dense(meter)	3.88 m	4.10 m	3.61 m	3.80 m
Metal3	Dense(meter)	3.10 m	3.20 m	2.94 M	3.12 m
Via1	Normal	469.2 K	491.0 K	417.6 K	469.2 K
Via1	Borderless Fringe	2.20 M	2.33 M	2.11 M	2.26 M
Via1	Borderless Extension	1.99 M	2.14 M	1.94 M	1.99 M
Via2	Normal	469.2 K	491.0 K	417.6 K	469.2 K
Via2	Borderless	1.90 M	2.00 M	1.82 M	1.95 M
Stacked Via	Borderless Fringe	751.9 K	833.5 K	730.5 K	788.2 K
Stacked Via	Borderless Extension	751.9 K	833.5 K	730.5 K	788.2 K
Total Cells (Column X Row)		15X8	8X8	15X15	15X8
Detection Resolutions		2	3	1	2

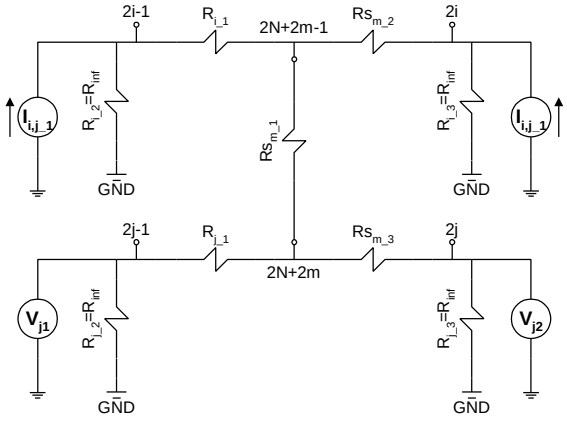

Fig. 5: Schematic graph of short-circuit model.

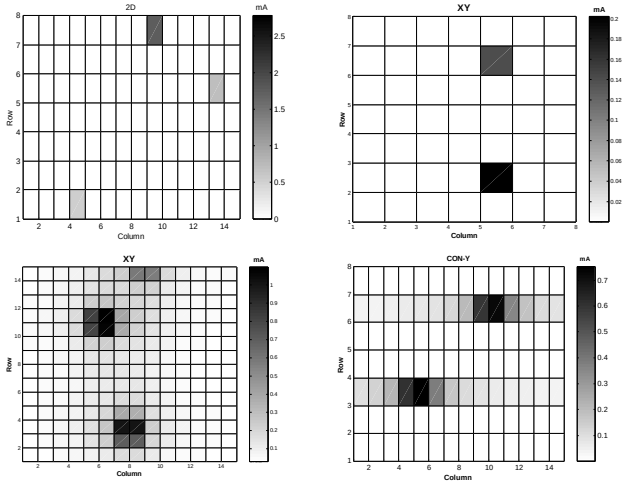

Fig. 6: Leakage chip map of four types of test structure. (a~d) are 2D, XY, CON, and CON-Y, respectively.

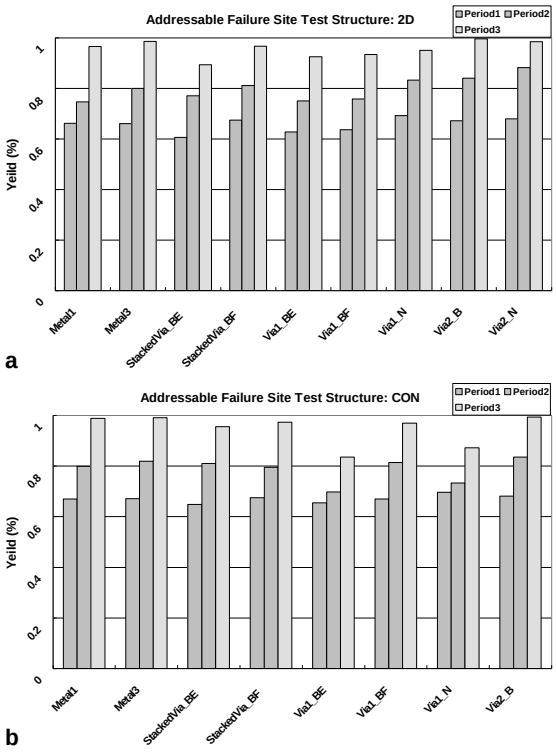

Fig. 7: The yield trends test structure categorized by test key module. (a) 2-D type. (b) CON type.

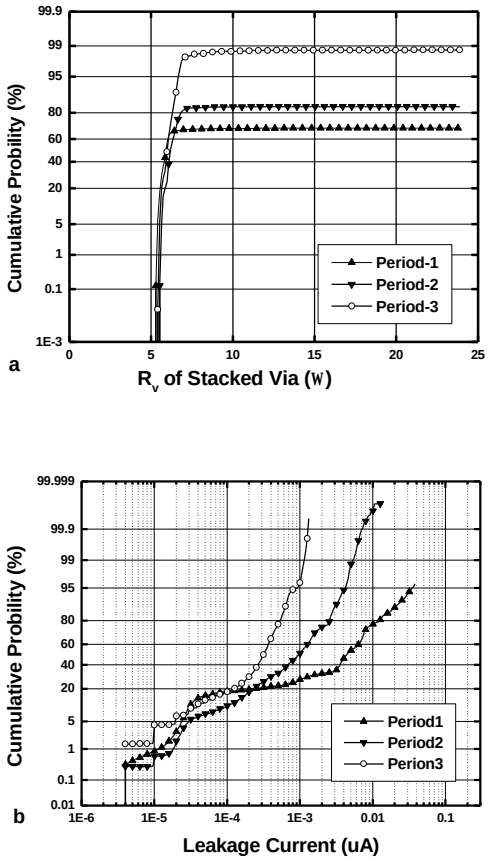

Fig. 8: The effect of process optimization. Stacked borderless via test structures is used as optimization index.

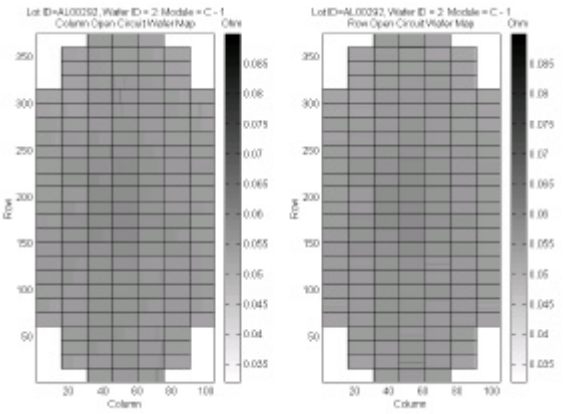

Fig. 9: L. Wafer map of Column direction M3 sheet resistance.
R. Wafer map of Row direction M3 sheet resistance.

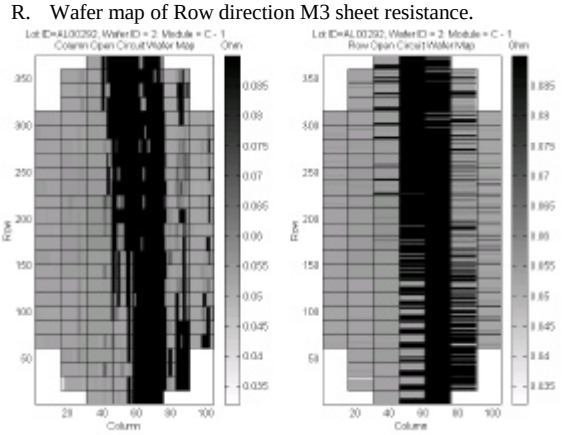

Fig. 10: L. Wafer map of Column direction M3 sheet resistance.
R. Wafer map of Row direction M3 sheet resistance.

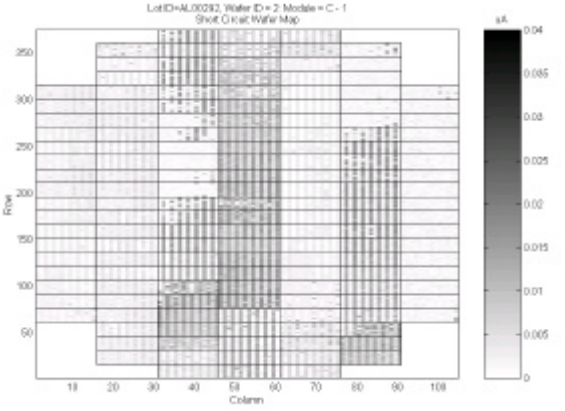

Fig. 11: Wafer map of leakage current. Normal process.

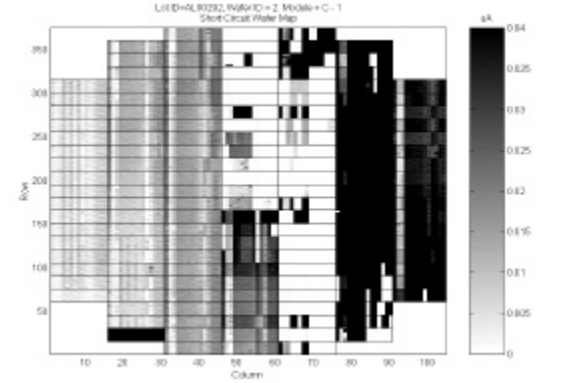

Fig. 12: Wafer map of leakage current. Abnormal process.