Manufacturing Defect Control and Yield Analysis by Using Addressable Failure Site Test Structures (AFS-TS)

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Abstract

This work describes the implementation of a novel test structure called addressable failure site test structure for manufacturing defect control in advanced semiconductor manufacturing. It manifests the design, simulation results, defect control and yield analysis of addressable failure site test structures. The novel test structures are used to identify the locations of killer defects which are then used to wafer map defect sites. A test chip of 4.0x6.6 mm^2 containing nine types of test structures was implemented using 0.25 μm logic backend of line process. This simple and efficient killer defect identification of process steps is employed as yield enhancement strategy.

Summary

With the progresses in process technology of ultra large-scale integrated circuit (ULSI), the criteria of process stability is getting strict and stringent. The scale of process control test vehicle or test structures, referring to the totals of transistors, contacts, vias, interconnect, etc., is required much more than that of typical chip design to ensure the high yield of IC products. However, as the scale increases, the increase of test structure chip area results in the difficulty in detecting and isolating failure site. It is thus essential to design the system which could detect the failure information including address, size, and susceptive failure process steps. It would be a promising way to segment a test structure into memory-like structures that can make it more efficient in quickly ascertaining the defect type, tracking back the defectively process steps, and reducing defect density [1~8].

In this work, we propose a novel design scheme of test structures, called addressable failure site test structures (AFS-TS), for manufacturing defect control (MDC) as well as IC process development. The design principle is to resolve the whole test structures into sub-chip matrix individually tested by electrical parametric tester, and provide a highly accurate estimation of the killer defect ratio by combining the optical inspection and electrical testing map. For the convenience sake on model description and presentation, some graphic terminology has been adopted to model the geometry of layout objects inside a test structure. The nodes ($N=\{n_1, n_2, n_3$ ¡ ., $n_N\}$) stand for the measurement points with conductive layout objects (conductive unit [CU]) like comb or meandering lines. The line (L) describes the measurement path between two measuring pads, either short circuit check (SCC) or open circuit check (OCC). L = { l_{ij}, i, j = 1, 2, 3 ¡ , N (a) if i 1 j, the l_{ij} means short circuit check unit (SCCU); (b) If i = j, the l_{ij} means open circuit check unit (OCCU); } The whole test structure is noted by G = (N, L). Hence, to achieve a precise localization of defect inside test chip means to access every node and identify faults inside the edges. Figure 1 shows the schematic layouts & their geometry graphs of typical test structures. Figure 2 presents the geometry graph of AFS-TS, where 32 nodes were separated as two X, Y groups, solid line is a conductive component, and dot-line means a possible leakage path. The AFS-TS with 32 (N=2*m)-nodes provides 225 ($(m-1)^2$) SCCUs in solid-line and 30 (2*(m-1)) OCCUs in dash-line. The placement and routine is shown in Fig. 3. The novel design only adopts two conductive layers without active devices, and could be applied to different processes and technologies, such as interconnect contact/via and conductive layer are shown in Fig. 4(a), and Fig. 4(b), respectively.

The first step is to design SCCU/OCCU and define the corresponding electrical testing specification. The sub-matrix of test chip is composed of unit cells either SCCU or OCCU, and is put into the common placement and routine. The AFS-TS is modeled as X, Y resistors network as shown in Fig. 5. Figure 6 manifest the testing method, where wafer automatic testing (WAT) measure and shift around the probe pads. To validate the design of test structure, in-house simulator in Matlab 5.2 is programmed to extract the voltage and leakage current spatial distribution from test chip as shown in Fig. 7, where the peaks are short circuit failure. With itinerating review on the simulation results and testing methods, an optimal testing method and structure are thus confirmed. Based on this design methodology, the test chip contains nine backend of line (BEOL) modules of AFS-TS and MDC structures as shown in Fig. 8.

A standard 0.25 um BEOL process is enacted to validate the AFS-TS. The statistical data was taken from 155 dies per wafer, where C-1 Module is two 1.45m Metal3 groups divided into 15 segments. Figure 9, and Figure 10 show the Metal3 continuity and bridging yield for two wafers, normal and abnormal processes, respectively. Figure 9 shows that the normal process (Wafer_ID=8) meets the process control limits both for continuity and bridging, not the abnormal process (Wafer_ID=2). Figure 11, 12 show the Metal3 sheet resistance in column, and row at the left hand-side and right hand-side, respectively. The wafer map of sheet resistance in Fig. 11 shows that the center is slightly higher than edge but still within specification. Figure 12 indicates that the failure is concentrated within the wafer center. Figure 13, 14 show the leakage current wafer map. Again, Figure 13 shows the center is slightly higher than edge but still within specification. Figure14 shows the short circuit failure at the right hand-side of wafer and low leakage at the wafer center, which is consistent with the wafer center preferring to open circuit failure. Owing to the merit of addressable failure site test structures, we could quickly address the failure site based on the testing result. Figure 15 shows the bridging defect of Metal3.

This above mentioned design methodology builds up a systematic design flow and a complete set of test structure of conductive layer and interconnection process for defect tracking method, which enable the correlation of inspection defect and electrical testing faults. Defects can be characterized and located prior to physical failure analysis. The WAT data can be compared with the defect data obtained from inspection machine for high accurate killer ratio defining and yield prediction, which provides the promising way to correct the errors of defect data obtained by inspection machine. Using this approach, large quantities of data can be quickly processed allowing precise electrical defect density to be set, also provide a common manufacturing defect control tool.

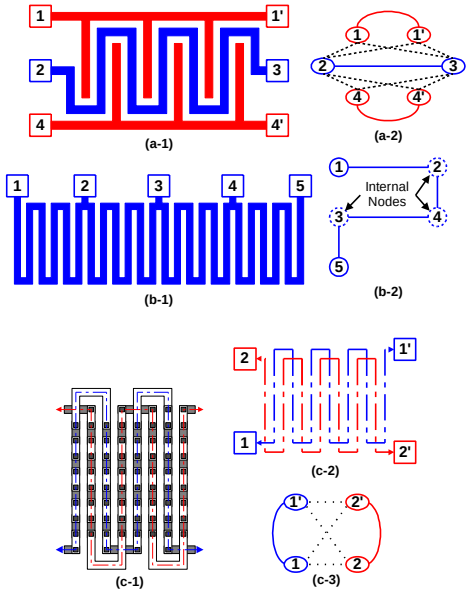

Fig. 1: Typical test structure and their geometry graphs. The solid line represents the conductive component and the dash line stands the possible leakage paths. (a-1), (b-1) Schematic layout of conductive layer. (a-2), (b-2) Geometry graph. (c-1) Schematic layout of Contact/Via chain. (c-2) Placement and routing. (c-3) Geometry graph.

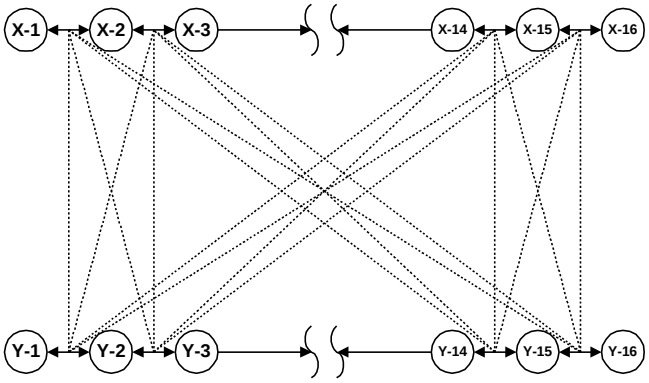

Fig. 2: Geometry graph of (32-nodes, 32 pads) (N=2*m, m=16) test structure. The test structure contains 225 ($(m-1)^2$) SCCUs in solid-line and 30 (2*(m-1)) OCCUs in dash-line.

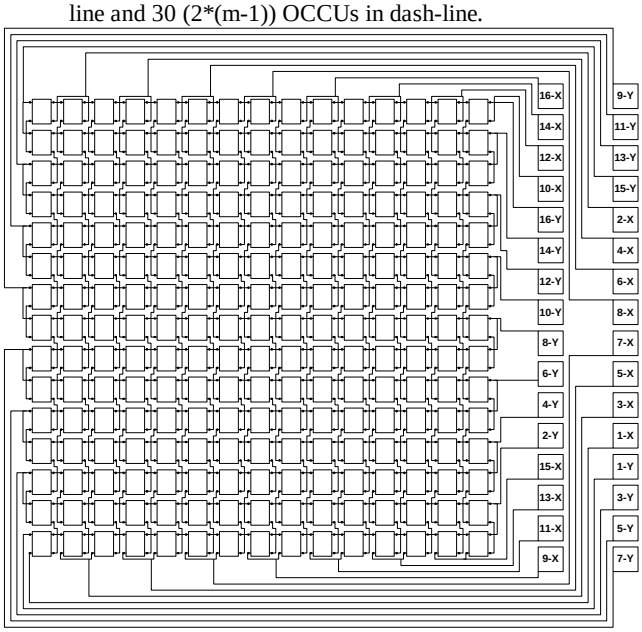

Fig. 3: Placement and routine of test structure. 32-probepads WAT test probe card is used.

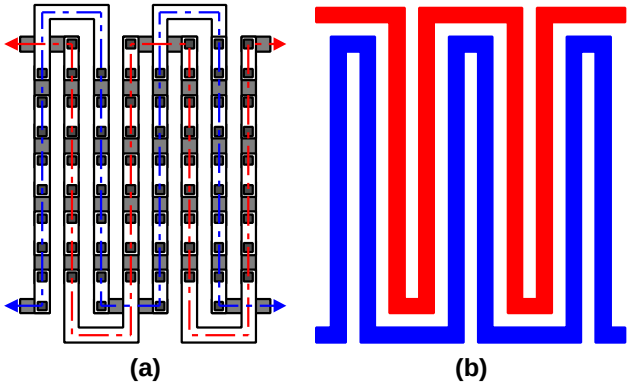

Fig. 4: Schematic layout of matrix element. (a) Schematic layout of Contact/Via chain. (b) Schematic layout of conductive layer.

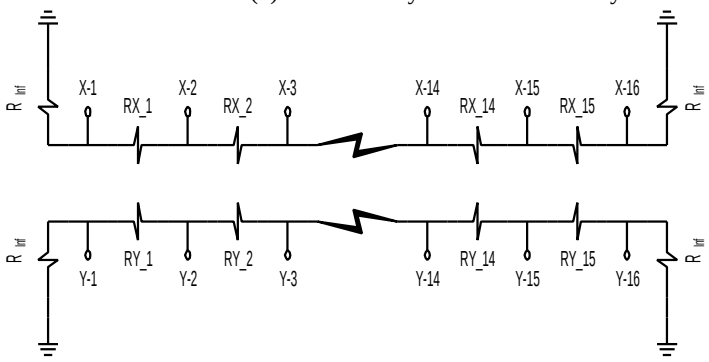

Fig. 5: The major test structure is modeled as 15*2 sub-resistors with R_{Inf} connected to GND, where R_{Inf} represents leakage from measurement system.

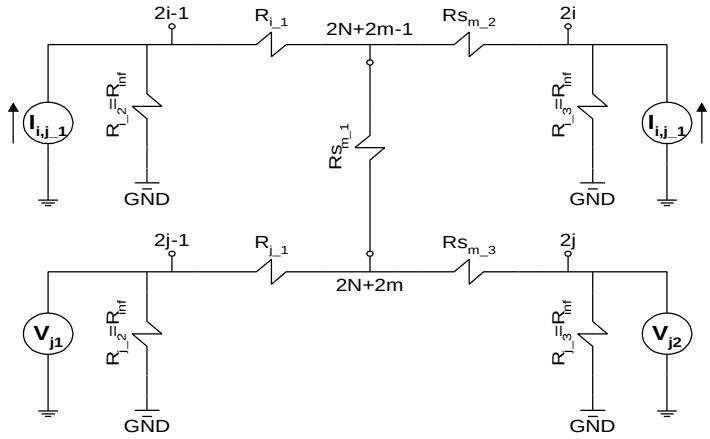

Fig. 6: Schematic graph of short-circuit model.

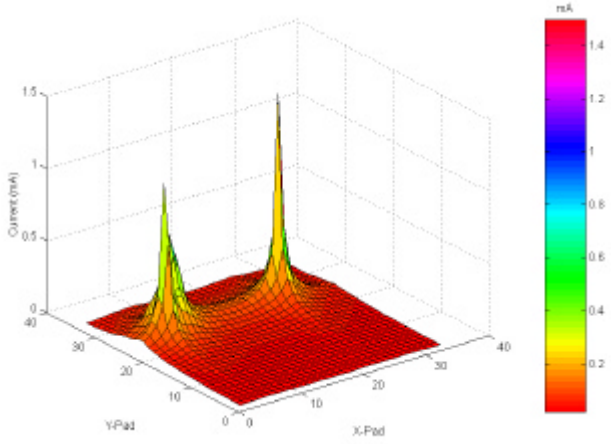

Fig. 7: 3-D surface graph of leakage current between nodes.

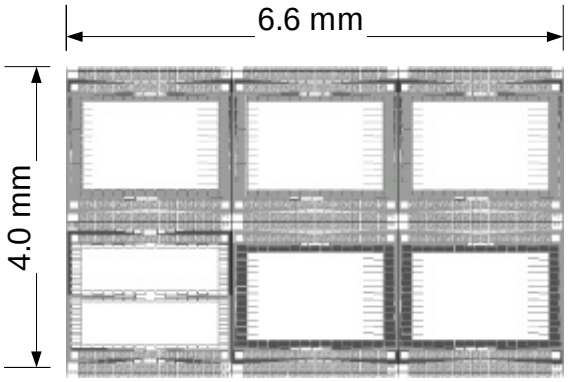

Fig. 8: Layout of addressable failure site test structures.

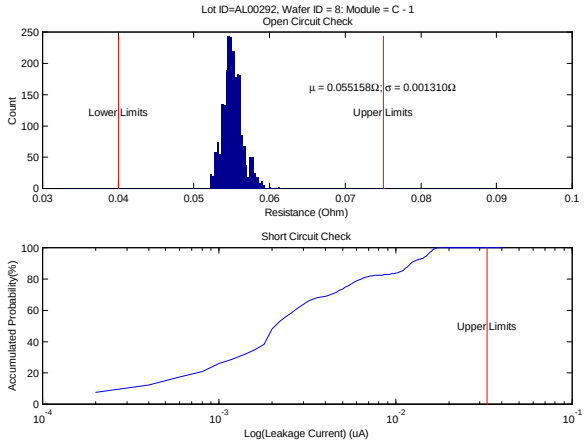

Fig. 9: U. Histogram of M3 sheet resistance. B. Accumulated probability of leakage.

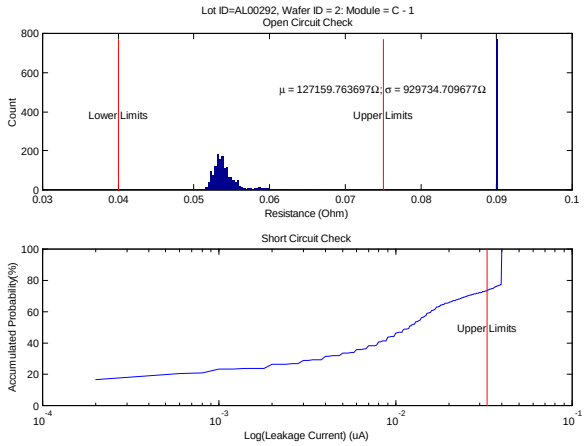

Fig. 10: U. Histogram of M3 sheet resistance. B. Accumulated probability of leakage.

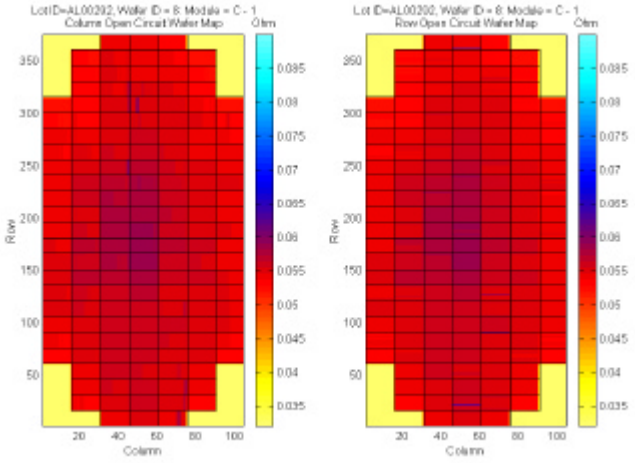

Fig. 11: L. Wafer map of Column direction M3 sheet resistance.
R. Wafer map of Row direction M3 sheet resistance.

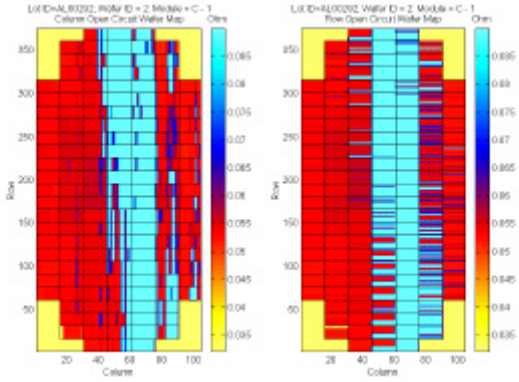

Fig. 12: L. Wafer map of Column direction M3 sheet resistance.
R. Wafer map of Row direction M3 sheet resistance.

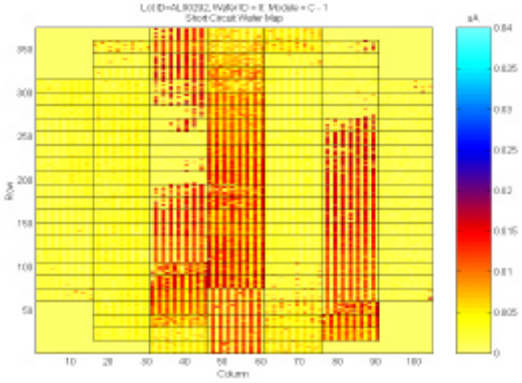

Fig. 13: Wafer map of leakage current.

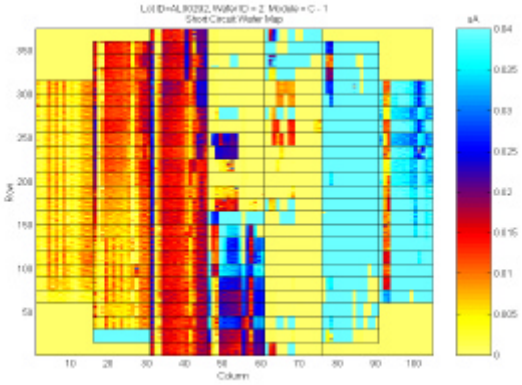

Fig. 14: Wafer map of leakage current.

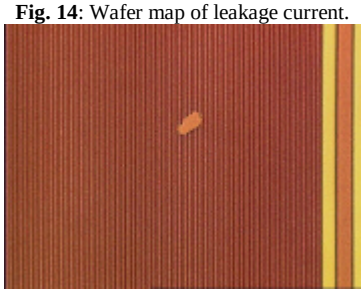

Fig. 15: Bridging defect of M3.

References

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