Optimization of Low-k Dielectric (Fluorinated SiO_2) Process and Evaluation of Yield Impact by Using BEOL Test Structures

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ABSTRACT

This work describes the optimization of low-k dielectric process and evaluation of yield impact by using back end of line (BEOL) test structures. Three splits of low-k dielectric process was compared with high-density-plasma un-doped-silicon-glass (HDP-USG) process are electrically characterized with the test structures of the BEOL unit process and integration process parameter extraction. The interconnect capacitance is used as the optimization criteria of low-k dielectric process and the yield impact is reviewed for the concern of manufacturing.

INTRODUCTION

With the rapid shrinkage of integrated circuit industry, the circuit delay due to interconnect is getting larger than the one of transistor, which it seriously degrade the performance of the device speed [1]. Compared with conventional inter-metal dielectric materials, the contribution of RC delay and cross-talk of interconnect has been greatly improved by the scheme of low-k dielectric process [2]. A sophisticated electrical characterization of low-k dielectric process had been proposed and the influence of cross talk was analyzed in the regime of high frequency[3]. However, for the concern of volume production and the compatibility of clean room of fabrication line, it is necessary to develop a methodology for analysis dielectric constant and the evaluation of yield impact with the quick turn around time.

In this work, a complete set of BEOL test structure for extract dielectric constant and evaluate the yield impact of low-k dielectric process is implement. The systematic analysis flow and deign of test structure is explored. The process tuning of low-k dielectric by fluorinated SiO_2 (FSG) is investigated and the yield impact is scrutinized by using the BEOL test structure.

METHODOLOGY

Usually, process optimization and new material development are qualified by the electrical specification of the scribe-line test-key and product yield. Though the scale and area of scribe-line test-key is too small to detect the process variation while tuning process and developing new material. Even caused low product yield, minor variation of electrical parameter extracted by the test vehicle will be hardly detected. Hereby, it is necessary to adopt the test vehicle, which of area and scale is capable of capturing the systematic failure by process or machine mal-function as well as the random defect caused by the falling particulate or flicker.

The design principle of BEOL test vehicle is to provide the most area for test structures and the complete set of test structures for the electrical parameter extraction, such as sheet resistance, single contact/via resistance, stacked via chains resistance, and etc. The BEOL test vehicle contains four types test-key of the yield impact evaluation and the electrical parameter extraction test structure such as, 4-point Kelvin, Van der Pauw, dielectric constant extraction and etc.

Table 1: Scale of BEOL test structure.

Type of Design Rule		TWOD	XY	CON	CXY
M1	Dense(meter)	3.88 m	4.10 m	3.61 m	3.80 m
Via1	Normal	469.2 K	491.0 K	417.6 K	469.2 K
Via1	Border-less Fr	2.20 M	2.33 M	2.11 M	2.26 M
Via1	Border-less Ext	1.99 M	2.14 M	1.94 M	1.99 M
Via2	Normal	469.2 K	491.0 K	417.6 K	469.2 K
Via2	Border-less	1.90 M	2.00 M	1.82 M	1.95 M
StackedVia	Border-less Fri	751.9 K	833.5 K	730.5 K	788.2 K
StackedVia	Borderles|sExt	751.9 K	833.5 K	730.5 K	788.2 K
Area Size		Medium	Large	Small	Medium

Table 1 shows the scale size of four type of test structures, which of the testing method using resistance network addressable algorithm could be found in [4]. The CON-type test structures with minimum area will be sensitivity for the process variation. The XY-type test structures with the maximum area will be the most capable to catch the defect yield impact. Traditionally, at the scribe-line test-key, the counts of the via chains is only 500 ~ several thousand and the length of serpentine conductive layers is 0.01 ~ 0.02 meter long. Compared with the sensitivity, the conventional test-key will be 1/500 less than of BEOL test structure adopted in this work. All of via test structures are categorized in two types, border-less and normal via. Normal via provides loose design rule for getting minimum contact resistance in via chain. Border-

less via will check un-landing via process window, where both are designed in the minimum design rule.

The test vehicle containing three layers for metal and two layers for via and one layer for pad are taped out in two masks, which one is dark and the other is clear. Each mask is combine with three layers. The die area is 1/3 of mask that is running at one shot per die.

The comb-meander and plate test structures is used for the extraction of the intra-layer and inter-layer metal capacitance, respectively. Interconnect capacitance of low-k FSG is used as the criteria of process release. Due to chemical vapor deposition is a mature process, these approach should require only a minimal change in integrated-circuit fabrication for different conditions. The judgement of various inter metal dielectric (IMD) process is concluded by comparing with the yield of stacked trend-vias, single trend-vias, metal sheet and different-area-size test structures with various design rules.

MEASUREMENT AND TESTING

For new process or material, the strictest electrical and physical specification will be proven by the BEOL test structures of yield impact and evaluations, which include different rules, sizes and pitches. In low-k dielectric process, the intra-metal capacitance is the major component of RC delay. The comb-meander test structure shown in Fig. 1(a) is used to extract the intra¡ metal value, where the line width is varied from 0.4 µm to 0.28 µm with metal pitch fixed at 0.64 µm. (1, 1¡¦) is floating, then (2, 2¡¦)is forced high, and (3, 3¡¦) is ground for data measurement. The result is equal to two parallel capacitors. One is make (1, 1¡¦) ground (2, 2¡¦) force high, the other is make (1, 1¡¦) ground (3, 3¡¦) for high.

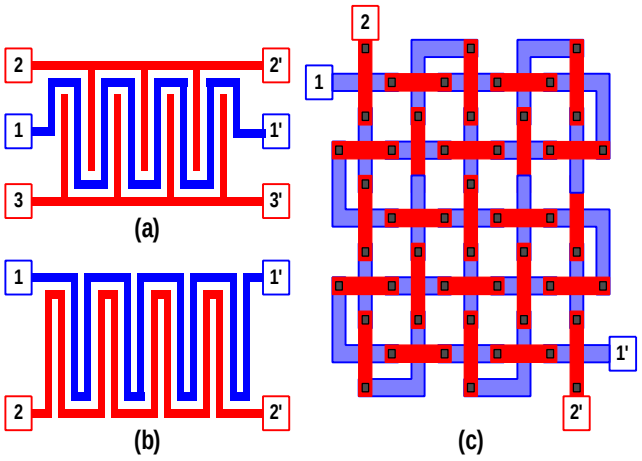

Fig. 1: BEOL test structure. (a) Capacitance test structure. (b) Metal leakage and continuity test structure. (c) Via- leakage and continuity test structure.

To ensure the low-k dielectric process is stable for manufacturing, the test structures of continuity and integrity of different-area-size metal structure and single or stacked trend-vias presented in Fig. 1(b, c). Fig. 1(b) is metal leakage and continuity test structure. To test metal leakage, (1, 1¡¦) is forced high and (2, 2¡¦) is ground. As metal continuity test, (1)/(2) are forced high and (1¡¦)/(2¡¦) are grounds or vice versa. Fig. 1(c) is the test structure of via leakage and continuity. It is divided into two types, single and stacked via chains. The measurement is the same as metal leakage and continuity test structure.

EXPERIMENT

The schematic cross section of BEOL scheme is revealed in Fig. 2. Wafer is fabricated on 200 mm p-type <100> silicon wafer deposited a PE-oxide with furnace-anneal as buffer layer. The scheme of metal film is the sandwich, Al-Cu (0.5%) combined with titanium and titanium nitride sputtered as a stacked metal layer. IMD is coated with low-k material prior to the planarization process, chemical mechanical polishing (CMP). Poison-mode long-throw titanium-nitride process combines with RIE clean being for via1 and via2 glue layer. Low temperature tungsten plug process is used for via1 and via2. For the global planarization process, the IMD-CMP, tungsten CMP (W-CMP), and oxide buffering CMP are proceeded.

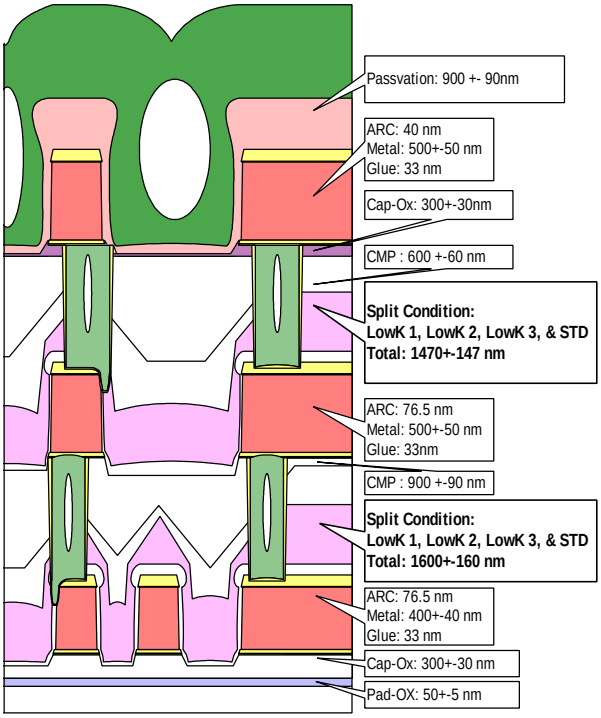

Fig. 2: Cross section schematic diagram of BEOL.

The IMD low-k split condition is categorized as follows: **lowk-1**, **lowk-2**, **lowk-3** processes and standard HDP-USG. The IMD is a sandwich structure containing three layers: the linear buffer oxide layer is used for metal protection prior to the deposition of the low-k film. Finally,

an oxide layer is capped on the top. For **lowk-1** and **lowk-2**, the difference is buffer oxide thickness. The **lowk-1** and **lowk-3** have exactly same stacked scheme except fluorine (F) doping concentration. The low-k film is deposit by HDP process, its gas combination is the same as normal HDP process except SiF_4 additive gas. A standard HDP procedure contains Ar, O_2, SiH_4, He and NF_3. Ar provides bombarding energy and heating source. O_2 and SiH_4 is reaction gas. He gas is adopted for cooling wafer backside. The wafer holder is electro static chuck (ESC). NF_3 is cleaning gas generated by remote plasma control. It also called as remote micro-wave-clean. All the measurement is conducted on Agilent Technology 4071 tester, in the SPECS environment and TSK UF-200 probe station. The capacitance measurement condition is 1Mhz with 2.5 Volt DC biased.

RESULTS

The capacitance of intra-metal indicates that **lowk-1** < **lowk-2** <¡ **lowk-3** < standard HDP-USG process as shown in Fig. 3. Intra-metal capacitance for **lowk-1** is less than **lowk-2,** by the means of its buffer oxide is thinner. **Lowk-1** dielectric thickness is only 58% of **lowk-2**. The intra-metal low-k dielectric filled ratio in the gap is 56% for **lowk-1**, 25% for **lowk-2**, and 56% for **lowk-3**. Since **lowk-3** fluorine doping concentration is only 30% of **lowk-1**, **lowk-1** capacitance should less than **lowk-3** even the scheme is identical. The additive effect is neutralization by gap filling ratio, that is the reason **lowk-2** and **lowk-3** is almost identical even they do not have same schematic and fluorine doping concentration. For HDP-USG, the capacitance is the highest of four groups. The trend charts indicate minimum space is sensitive to the filling capability and chemical addition quantity low-k material.

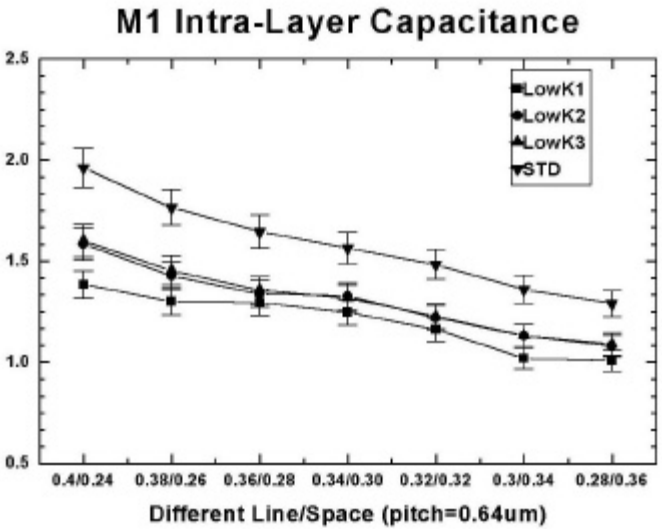

Fig. 3: Metal-1 Intra-layer capacitance.

The distribution uniformity on wafer identifies that the process control of four splits provides the least variation as shown in Fig. 4. **Lowk-1** shows the best uniformity because of higher fluorine doping concentration. The SEM micro-graphs demonstrate that the physical damage of top ARC and aluminum is not observed obviously different from four processes as shown in Fig. 5. Without liner protection layer, these samples appear seams after buffered-of-etch (BOE) treatment. These profiles point to **lowk-3** coating with a lower bombard/etching ratio film than **lowk-1** and **lowk-2**.

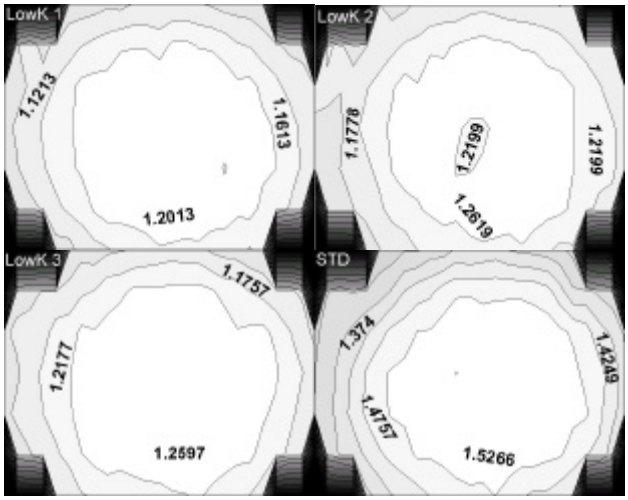

Fig. 4: Wafer map of Metal-1 intra-layer capacitance.

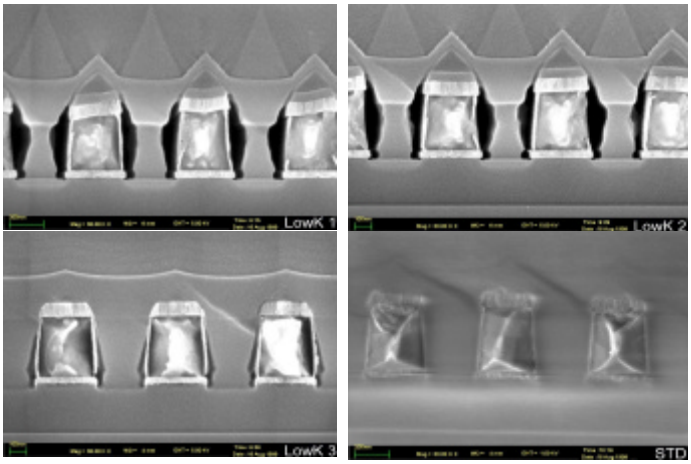

Fig. 5: Cross Section SEM micro-graphs of IMD-1.

For the inter-metal capacitance (plate to plate capacitance), the trends illustrate **Lowk-1** ¡ **Lowk-2** < **Lowk-3** < standard HDP-USG process as viewing in Fig. 6. It is different than previous intra-metal item, as the dominated-factor is dielectric film's fluorine doping concentration. In IMD scheme, the thickness of low-k material is about 42% in the IMD1 (M1/M2) and IMD2 (M2/M3) structure. The value of IMD1 and IMD2 is different for the reason that film structure is not identical. **Lowk-1** and **Lowk-2** are the same quantity in fluorine doping concentration, but **Lowk-3** is less. As HDP-USG, there is no any fluorinate in the film. The higher variation of inter-metal capacitance result from the thickness

variation of the IMD film. It is hard to make all parameter well under control like metal film and dielectric film thickness, fluorine doping concentration and CMP process window. The uniformity distribution on wafer shows a good capability of process control of four splits, specially, **Lowk-1** and **Lowk-2** come with the wide range of uniformity as shown in Fig. 7. **Lowk-1** and **Lowk-2** show the best profile because of high chemical addition is key factor. The contour is worse at HDP-USG without these additives.

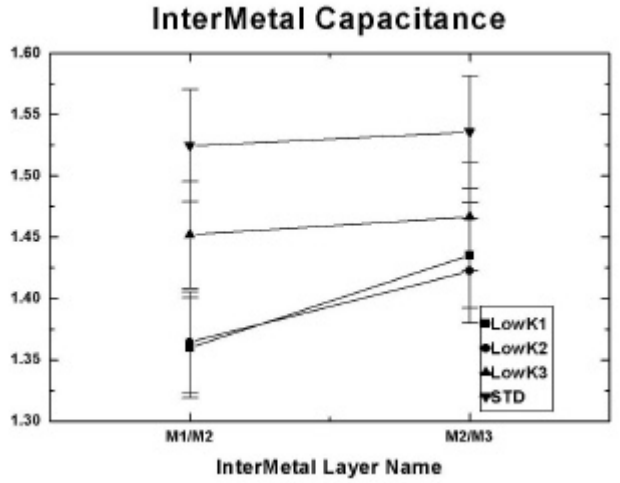

Fig. 6: Metal-1 inter-metal capacitance.

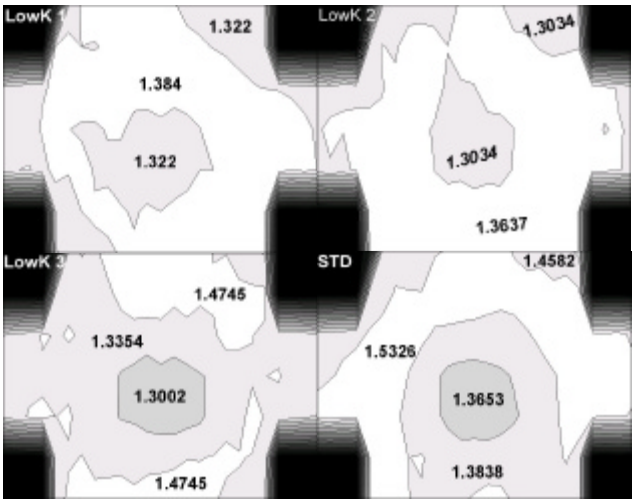

Fig. 7: Wafer map of Metal-1 inter-layer capacitance.

For the concern of manufacturing, the yield impact of process tuning has to be strictly reviewed. The test structure of via and metal is used to evaluate the yield of the continuity and integrity of single layer module. The stacked via is adopted for the release criteria of BEOL process integration. The whole test structure is constructed as a novel test chip, called as addressable failure site test structures (AFS-TS)[4]. The yield trend of various test structures shows that there is no obvious yield impact, except the metal-1 module fabricated by standard process as shown in Fig. 8. It is suspect that there is some damage at aluminum or oxidation on the aluminum side-wall. The damage is not observed significant in SEM micro-graphs. Maybe some chemical reaction, material transform or slight-damage in the aluminum. It reveals that **Lowk-1** has the best process integrity in BEOL. **Lowk-**2 and **Lowk-3** have proven the same influence in yield impact. The HDP-USG process makes largest yield lose because it without buffer oxide layer and the process is one step deposition.

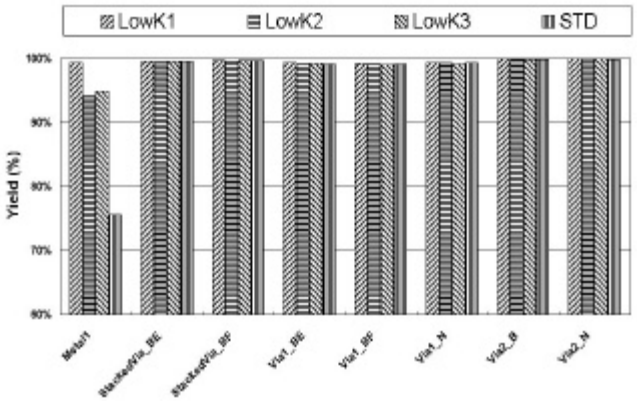

Fig. 8: The yield trend chart of BEOL test structures.

Calculating the test structure with different sizing points out that there is no huge defect influence in these processes. Sorting the test structure with different sizing set apart that small size will be more sensitivity in process optimization. **CON**-type has the smallest area in the four type of structure. **TWOD-** and **CXY-**type have the same size in area, but **CXY**-type is shorter in the metal sheet. **XY¡** type is longest of them and no suffering in yield loss as show in Fig. 9. **Lowk-1** reveals the process impact and integrity is least. **Lowk-2** and **Lowk-3** have some impact. HDP-USG is the highly influence. By analysis the cumulative probability chart of metal-1 sheet resistance as shown in Fig. 10, **Lowk-1** has the tightest distribution range of four conditions. **Lowk-2** and **Lowk-3** demonstrate these two conditions have the same capability. As the standard HDP-USG process, it suffers the higher sheet resistance with wide range, which is susceptive that the edge of metal more severely damaged or oxidized by the HDP-USG. The test key is more sensitivity since the unit-length is shorter and pitch is smaller[2].

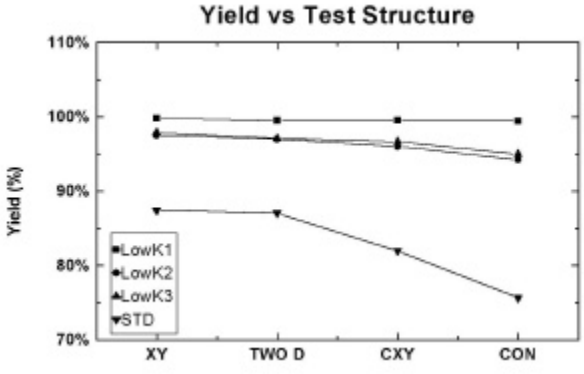

Fig. 9: The yield chart of metal 1test structures.

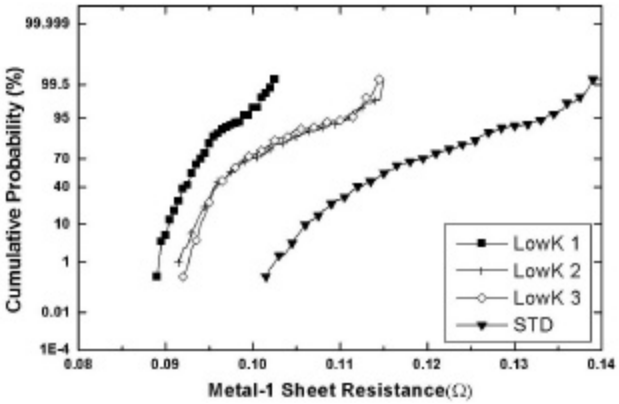

Fig. 10: Cumulative probability chart of Metal-1 sheet resistance.

CONCLUSION

The low-k dielectric process has been carefully characterized with the test structures of interconnect capacitance extraction and BEOL integration. With the feature of test structures, the yield analysis of low-k dielectric process can be done by BEOL short loop process, which provides the timely and costly solution for BEOL process optimization.

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