Eamon Caddigan

Joseph Kim

A Five-Stage Pipelined Processor with Branch Prediction

This project entails the construction of a simple pipelined processor. The chosen design will use a five-stage pipeline, and a branch target buffer will be included to prevent most stalls due to branch instructions.

The goal of this design is to produce a simple LC-2 processor that will execute operations quickly and properly. Heavy emphasis will be placed on the correct execution of every operand, as accuracy is much more important than speed.

A five-stage pipelined design and a branch target buffer will facilitate faster operation. Simple branch prediction will be implemented by the use of a two-bit counter. A BTB was chosen by the group as a means to give each member experience in the design of a different part of the processor, since cache design was introduced in MP2. An optimizer, to prevent stalls due to data dependencies by optimizing code at the assembly-level, will also be implemented as part of this project.

To allow for faster clock speed, this project will also involve the design of a new ALU, which will include a carry look-ahead adder. By doing this, the critical path will be governed by the fetch and decode stages of the pipeline, allowing for an estimated clock period of 20 ns.