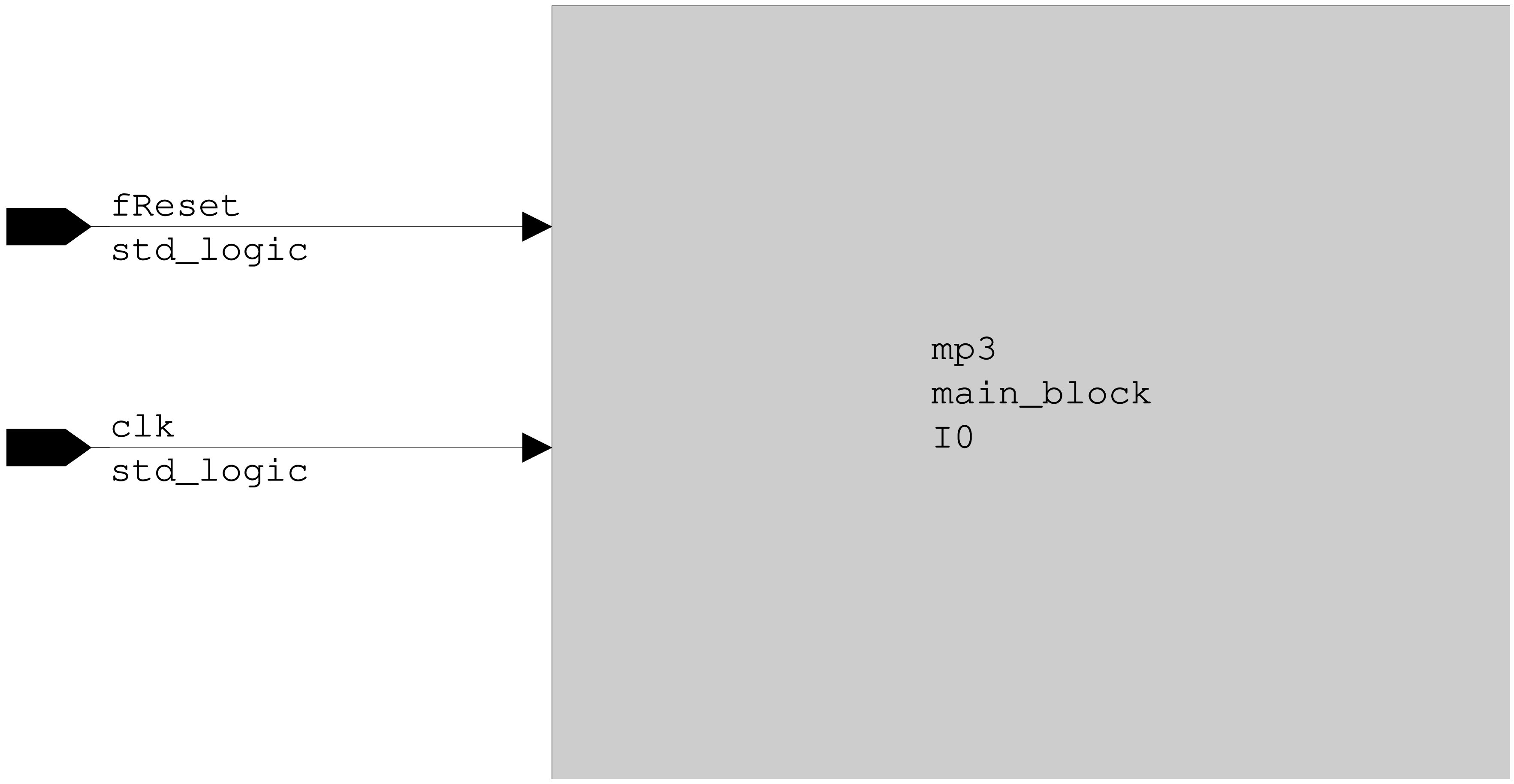
Package List

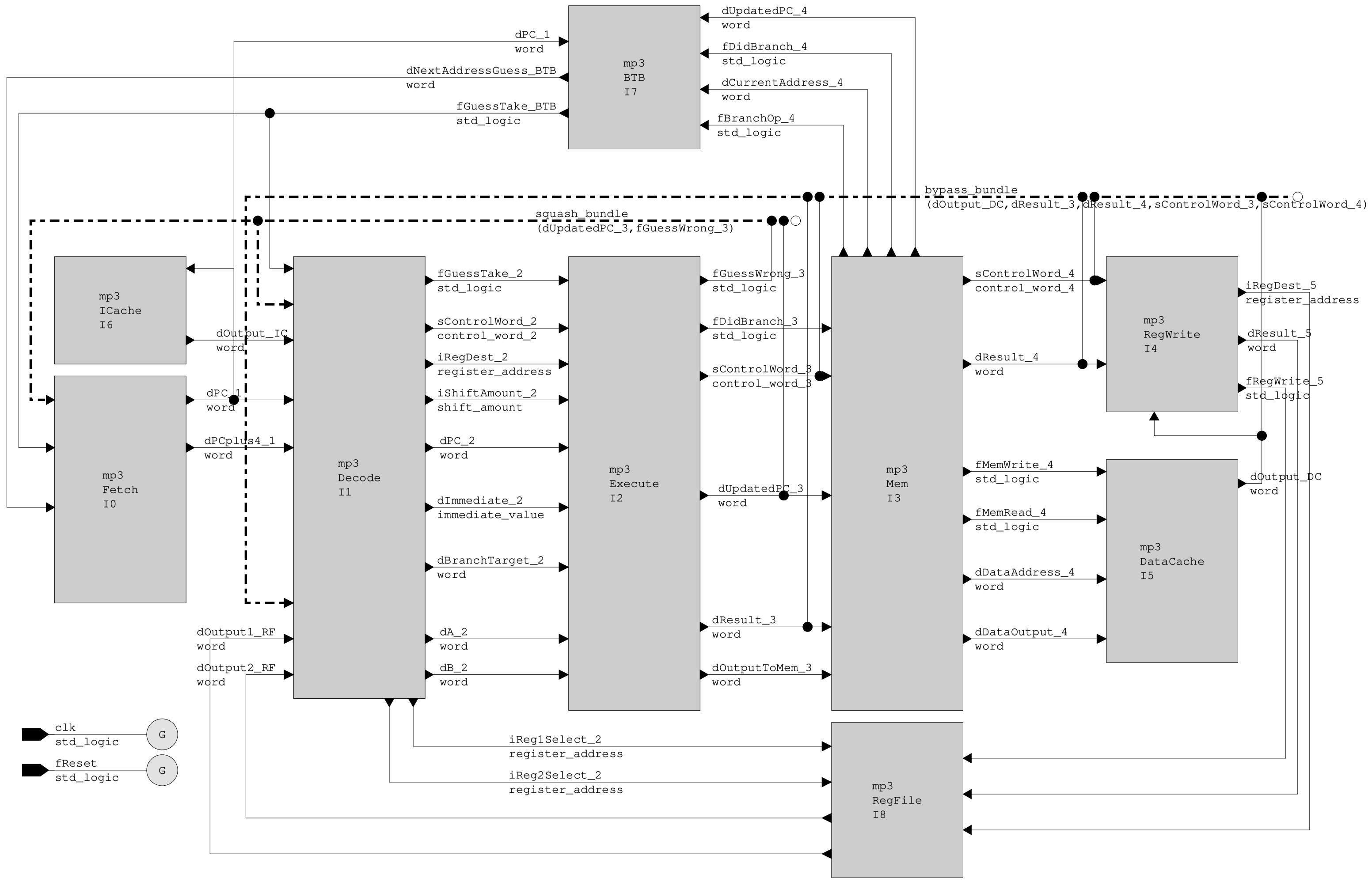
ieee	std_logic_1164
ieee	numeric_std
mp3	mp3_types
arithmetic	std_logic_arith

Declarations

clk : std_logic
fReset : std_logic



mp3/main_block/default



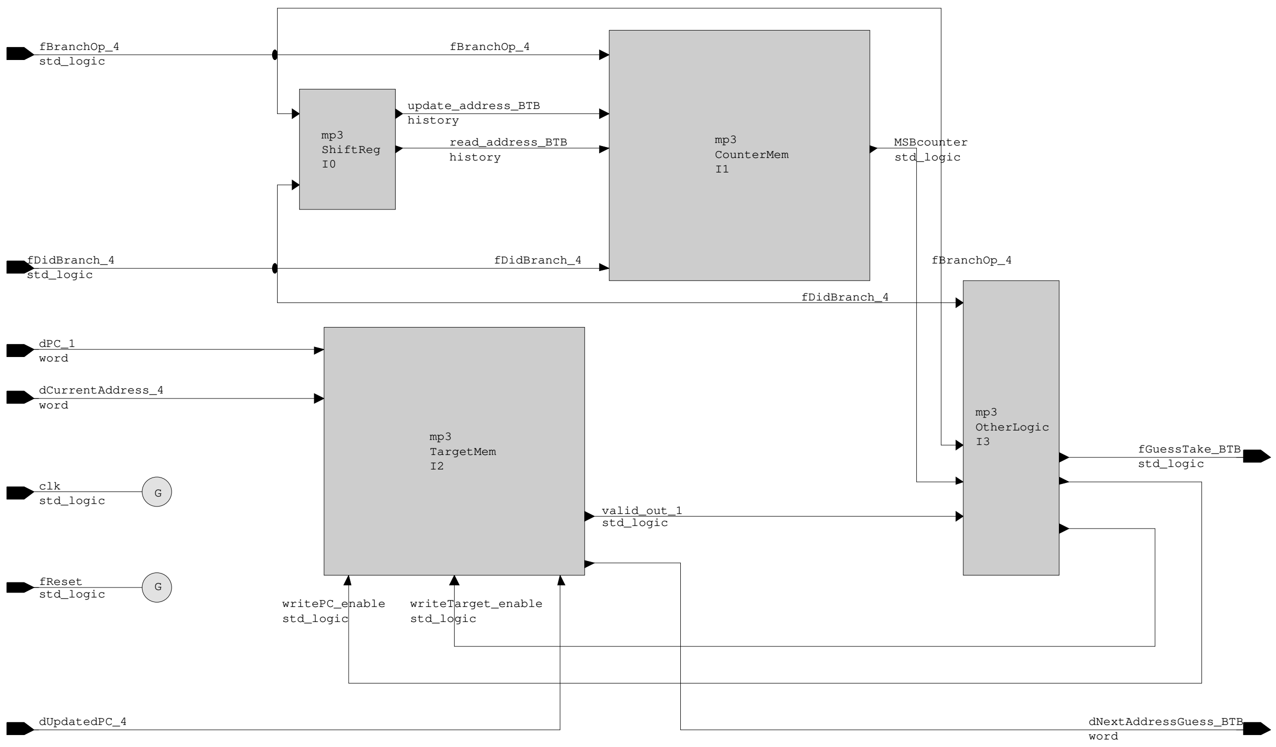
Declarations

clk : std_logic
dA_2 : word
dB_2 : word
dBranchTarget_2 : word
dCurrentAddress_4 : word
dDataAddress_4 : word
dDataOutput_4 : word
dImmediate_2 : immediate_value
dNextAddressGuess_BTB : word
dOutput1_RF : word
dOutput2_RF : word
dOutputToMem_3 : word
dOutput_DC : word
dOutput_IC : word
dPC_1 : word
dPC_2 : word
dPCplus4_1 : word
dResult_3 : word
dResult_4 : word
dResult_5 : word
dUpdatedPC_3 : word
dUpdatedPC_4 : word
fBranchOp_4 : std_logic
fDidBranch_3 : std_logic
fDidBranch_4 : std_logic
fGuessTake_2 : std_logic
fGuessTake_BTB : std_logic
fGuessWrong_3 : std_logic
fMemRead_4 : std_logic
fMemWrite_4 : std_logic
fRegWrite_5 : std_logic
fReset : std_logic
iReg1Select_2 : register_address
iReg2Select_2 : register_address
iRegDest_2 : register_address
iRegDest_5 : register_address
iShiftAmount_2 : shift_amount
sControlWord_2 : control_word_2
sControlWord_3 : control_word_3
sControlWord_4 : control_word_4

mp3/BTB/default

Declarations

MSBcounter : std_logic
clk : std_logic
dCurrentAddress_4 : word
dNextAddressGuess_BTB : word
dPC_1 : word
dUpdatedPC_4 : word
fBranchOp_4 : std_logic
fDidBranch_4 : std_logic
fGuessTake_BTB : std_logic
fReset : std_logic
read_address_BTB : history
update_address_BTB : history
valid_out_1 : std_logic
writePC_enable : std_logic
writeTarget_enable : std_logic



mp3/ShiftReg/flow

Architecture Declarations

SIGNAL update_address_buff1, update_address_buff2, update_address_buff3 : history;

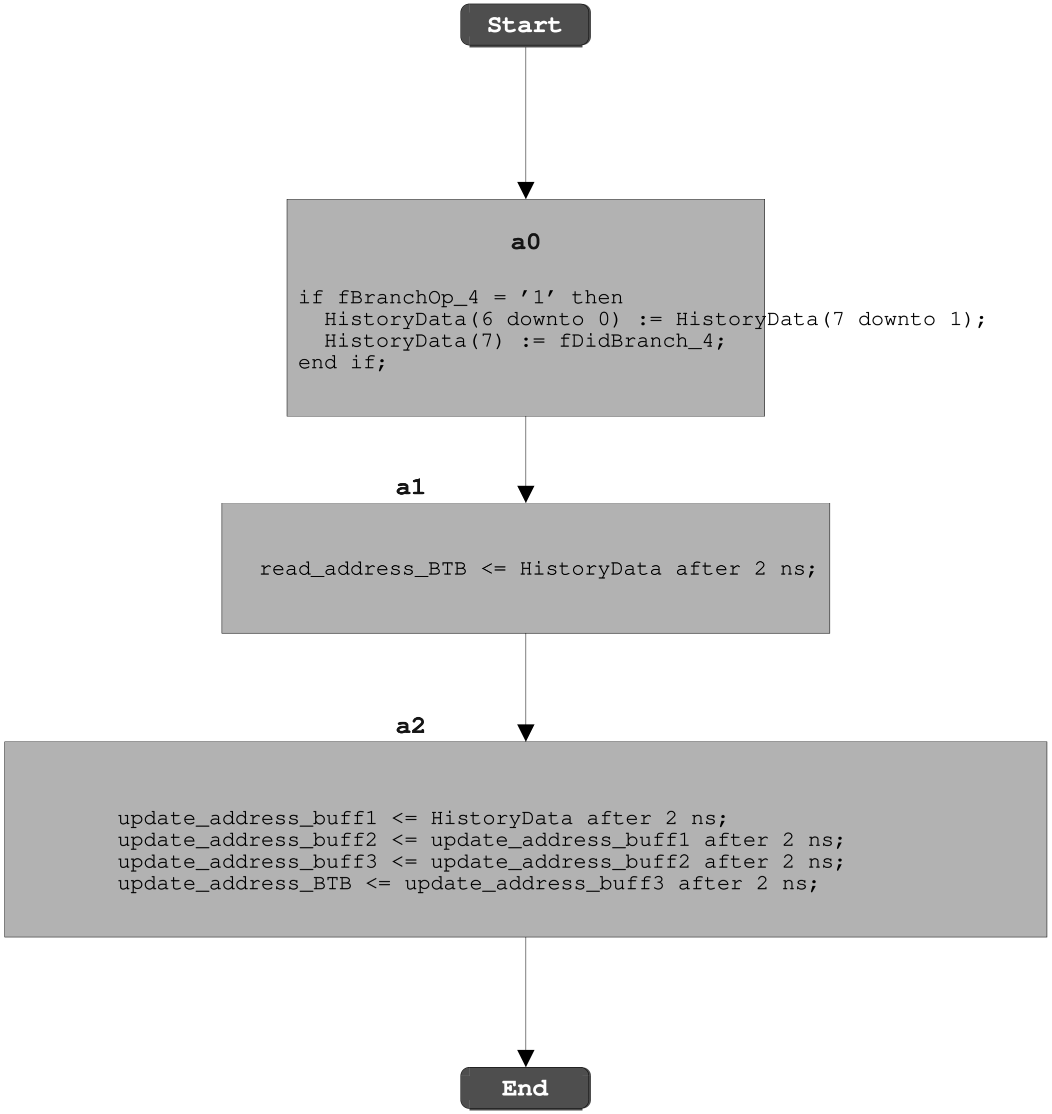
Concurrent Statements

Sensitivity List

< Automatic >

Process Declarations

Variable HistoryData : history := "00000000";



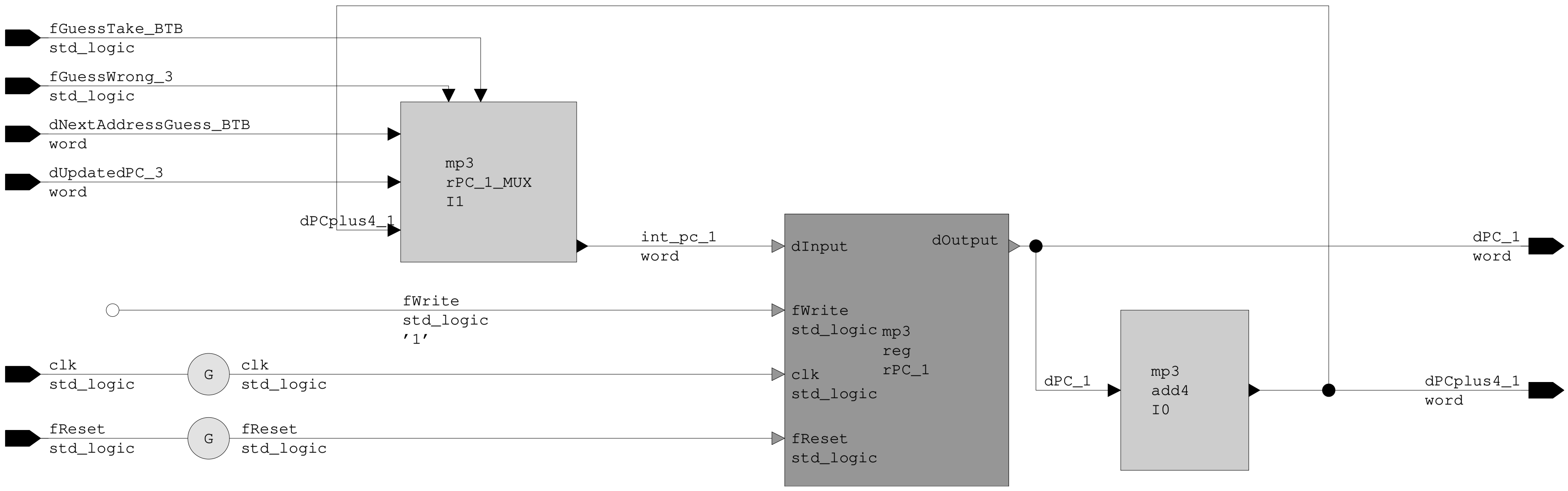
mp3/Fetch/default

Package List

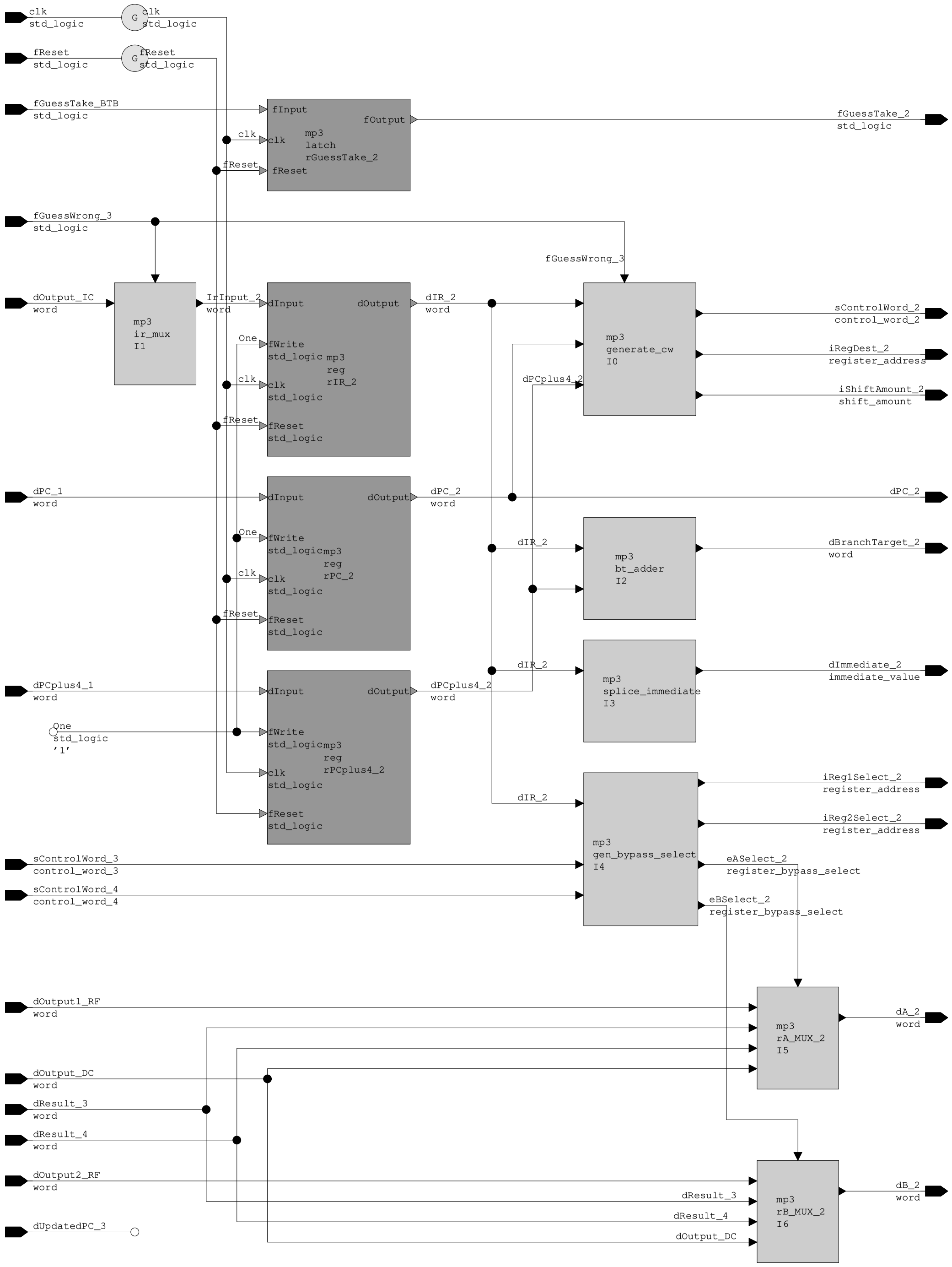
ieee	std_logic_1164
ieee	numeric_std
arithmetic	std_logic_arith

Declarations

clk : std_logic
dNextAddressGuess_BTB : word
dPC_1 : word
dPCplus4_1 : word
dUpdatedPC_3 : word
fGuessTake_BTB : std_logic
fGuessWrong_3 : std_logic
fReset : std_logic
fWrite : std_logic := '1'
int_pc_1 : word



mp3/Decode/default



Package List

ieee	std_logic_1164
ieee	numeric_std
arithmetic	std_logic_arith

Declarations

IrInput_2 : word
One : std_logic := '1'
clk : std_logic
dA_2 : word
dB_2 : word
dBranchTarget_2 : word
dIR_2 : word
dImmediate_2 : immediate_value
dOutput1_RF : word
dOutput2_RF : word
dOutput_DC : word
dOutput_IC : word
dPC_1 : word
dPC_2 : word
dPCplus4_1 : word
dPCplus4_2 : word
dResult_3 : word
dResult_4 : word
dUpdatedPC_3 : word
eASelect_2 : register_bypass_select
eBSelect_2 : register_bypass_select
fGuessTake_2 : std_logic
fGuessTake_BTB : std_logic
fGuessWrong_3 : std_logic
fReset : std_logic
iReg1Select_2 : register_address
iReg2Select_2 : register_address
iRegDest_2 : register_address
iShiftAmount_2 : shift_amount
sControlWord_2 : control_word_2
sControlWord_3 : control_word_3
sControlWord_4 : control_word_4

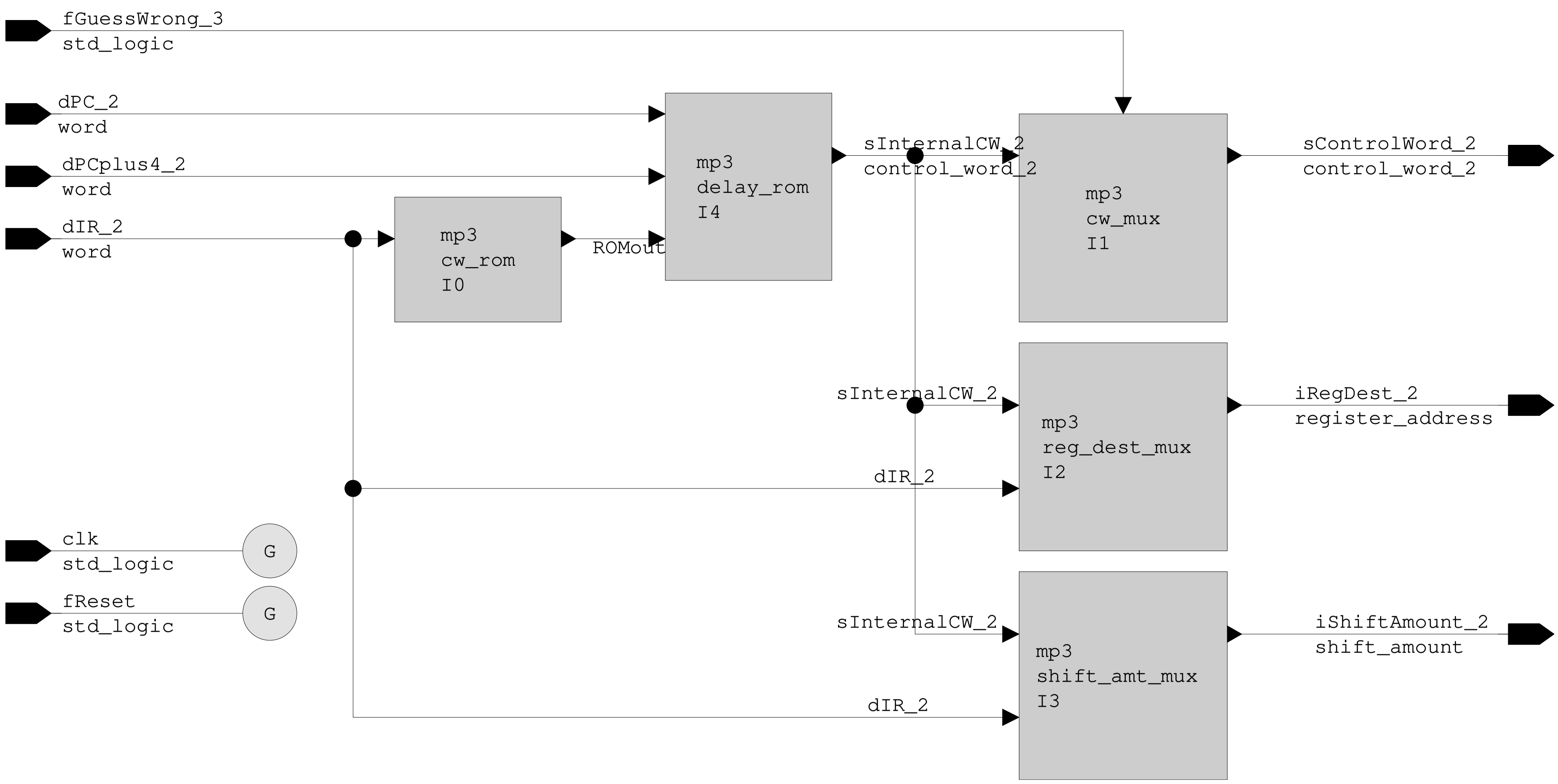
mp3/generate_cw/default

Package List

ieee	std_logic_1164
ieee	numeric_std
mp3	mp3_types
arithmetic	std_logic_arith

Declarations

ROMout : control_word_2
clk : std_logic
dIR_2 : word
dPC_2 : word
dPCplus4_2 : word
fGuessWrong_3 : std_logic
fReset : std_logic
iRegDest_2 : register_address
iShiftAmount_2 : shift_amount
sControlWord_2 : control_word_2
sInternalCW_2 : control_word_2



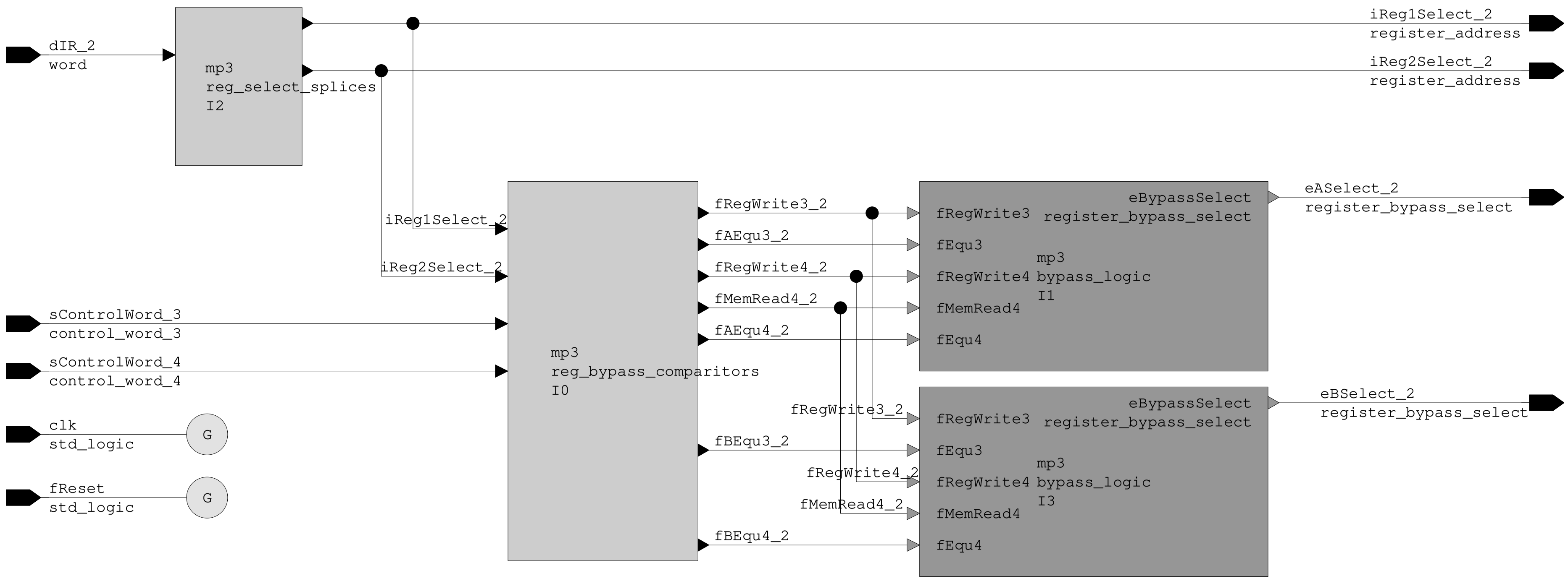
mp3/gen_bypass_select/default

Declarations

```
clk : std_logic
dIR_2 : word
eASelect_2 : register_bypass_select
eBSelect_2 : register_bypass_select
fAEqu3_2 : std_logic
fAEqu4_2 : std_logic
fBEqu3_2 : std_logic
fBEqu4_2 : std_logic
fMemRead4_2 : std_logic
fRegWrite3_2 : std_logic
fRegWrite4_2 : std_logic
fReset : std_logic
iReg1Select_2 : register_address
iReg2Select_2 : register_address
sControlWord_3 : control_word_3
sControlWord_4 : control_word_4
```

Package List

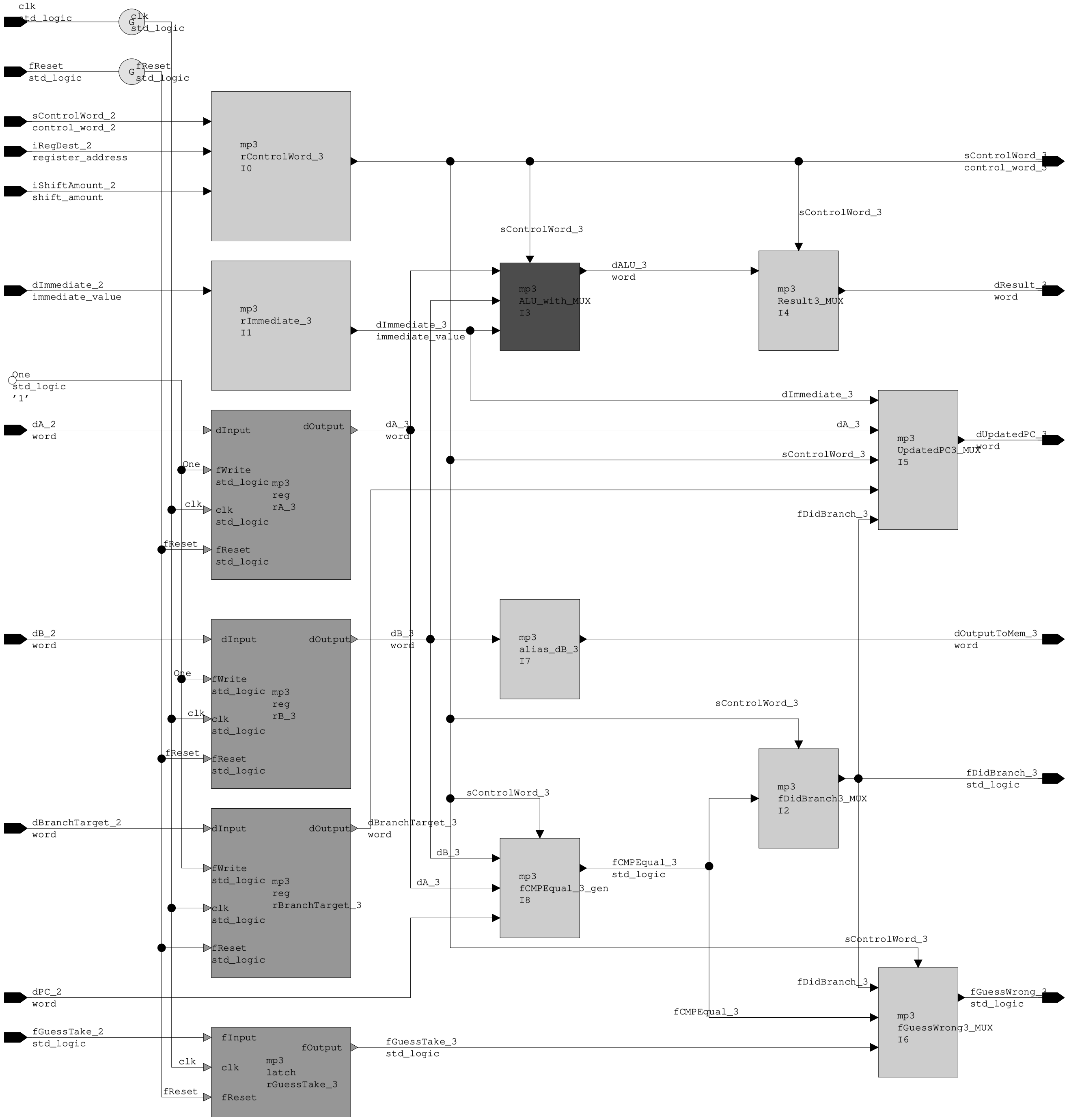
```
ieee std_logic_1164
ieee numeric_std
```



mp3/Execute/default

Declarations

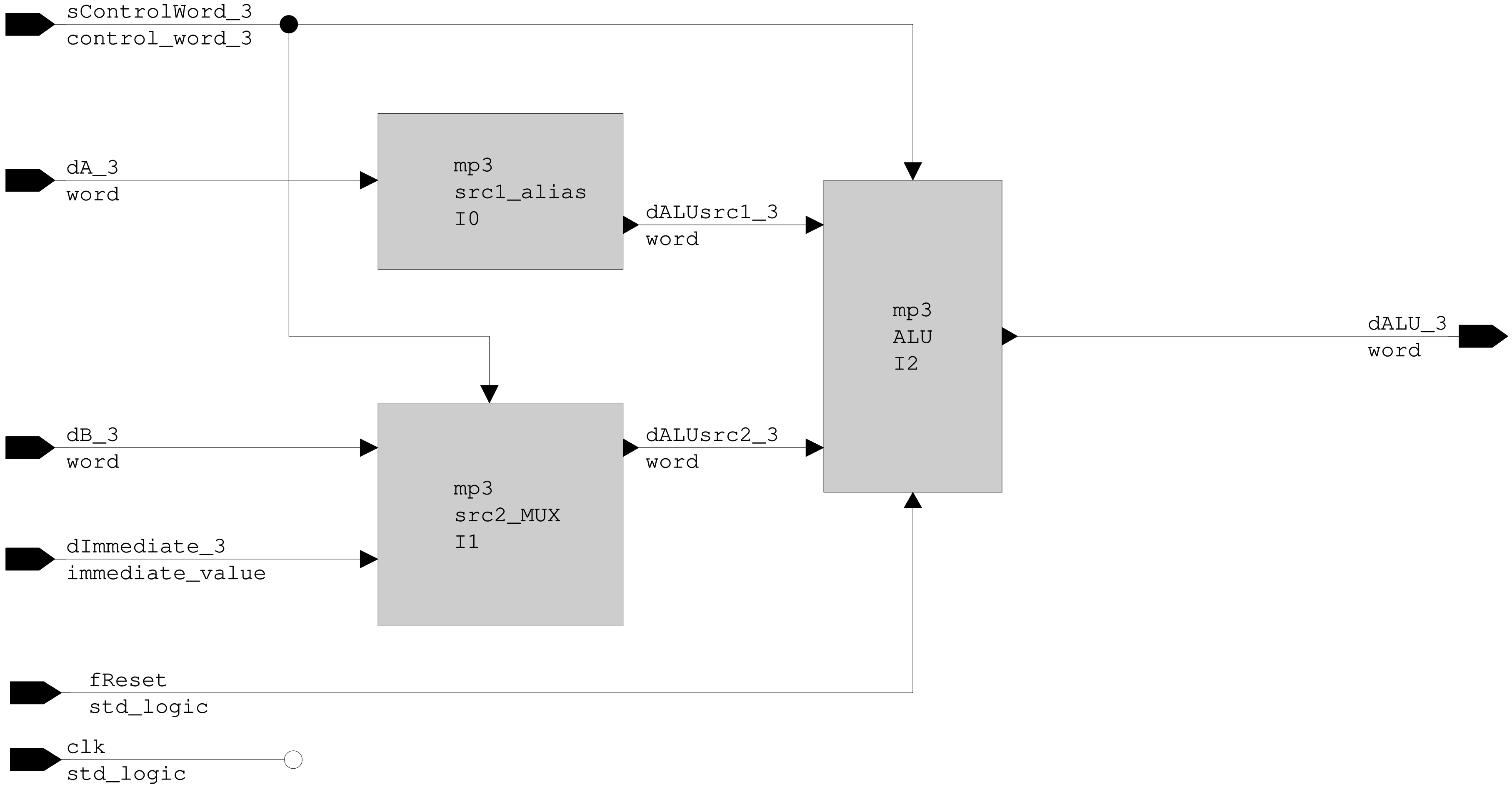
One : std_logic := '1'
clk : std_logic
dALU_3 : word
dA_2 : word
dA_3 : word
dB_2 : word
dB_3 : word
dBranchTarget_2 : word
dBranchTarget_3 : word
dImmediate_2 : immediate_value
dImmediate_3 : immediate_value
dOutputToMem_3 : word
dPC_2 : word
dResult_3 : word
dUpdatedPC_3 : word
fCMPEqual_3 : std_logic
fDidBranch_3 : std_logic
fGuessTake_2 : std_logic
fGuessTake_3 : std_logic
fGuessWrong_3 : std_logic
fReset : std_logic
iRegDest_2 : register_address
iShiftAmount_2 : shift_amount
sControlWord_2 : control_word_2
sControlWord_3 : control_word_3



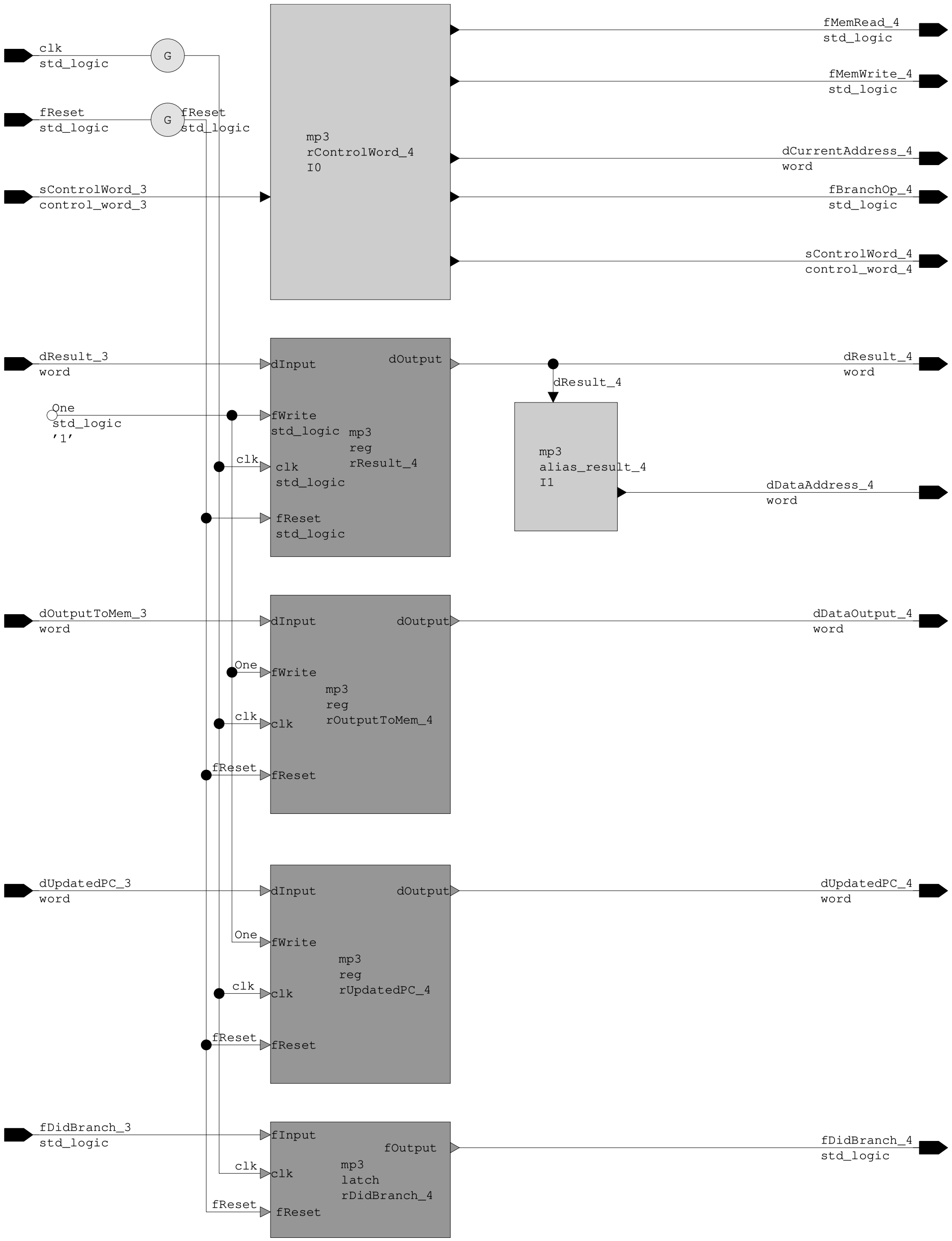
mp3/ALU_with_MUX/default

Declarations

```
clk : std_logic
dALU_3 : word
dALUsrc1_3 : word
dALUsrc2_3 : word
dA_3 : word
dB_3 : word
dImmediate_3 : immediate_value
fReset : std_logic
sControlWord_3 : control_word_3
```



mp3/Mem/struct



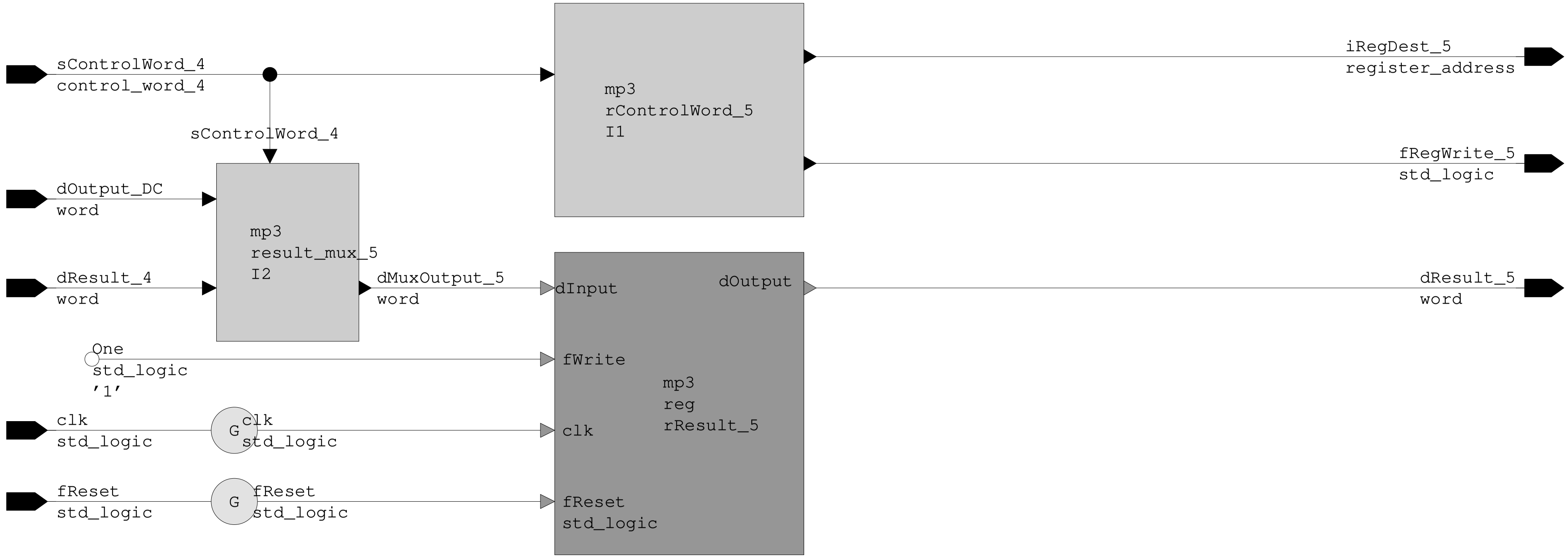
Declarations

One : std_logic := '1'
clk : std_logic
dCurrentAddress_4 : word
dDataAddress_4 : word
dDataOutput_4 : word
dOutputToMem_3 : word
dResult_3 : word
dResult_4 : word
dUpdatedPC_3 : word
dUpdatedPC_4 : word
fBranchOp_4 : std_logic
fDidBranch_3 : std_logic
fDidBranch_4 : std_logic
fMemRead_4 : std_logic
fMemWrite_4 : std_logic
fReset : std_logic
sControlWord_3 : control_word_3
sControlWord_4 : control_word_4

mp3/RegWrite/default

Declarations

```
One : std_logic := '1'
clk : std_logic
dMuxOutput_5 : word
dOutput_DC : word
dResult_4 : word
dResult_5 : word
fRegWrite_5 : std_logic
fReset : std_logic
iRegDest_5 : register_address
sControlWord_4 : control_word_4
```



1	dIR_2(31 downto 26)	dIR_2(5 downto 0)	ROMout.eRegDestSelect
2	op_alu	alufunc_add	EV_IR_15to11
3	op_alu	alufunc_sub	EV_IR_15to11
4	op_alu	alufunc_and	EV_IR_15to11
5	op_alu	alufunc_or	EV_IR_15to11
6	op_alu	alufunc_sll	EV_IR_15to11
7	op_alu	alufunc_srl	EV_IR_15to11
8	op_alu	alufunc_slt	EV_IR_15to11
9	op_addi		EV_IR_20to16
10	op_andi		EV_IR_20to16
11	op_ori		EV_IR_20to16
12	op_slti		EV_IR_20to16
13	op_lui		EV_IR_20to16
14	op_beq		*EV_IR_15to11*
15	op_bne		*EV_IR_15to11*
16	op_j		*EV_IR_15to11*
17	op_jal		EV_31

ROMout.fRegWriteOp	ROMout.fBranchOp	ROMout.fMemWriteOp
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'1'	'0'	'0'
'0'	'1'	'0'
'0'	'1'	'0'
'0'	'1'	'0'
'1'	'1'	'0'

ROMout.fMemReadOp	ROMout.eShiftAmountSelect	ROMout.eALUop
'0'	*EV_IR_10to6*	EV_Add
'0'	*EV_IR_10to6*	EV_Sub
'0'	*EV_IR_10to6*	EV_And
'0'	*EV_IR_10to6*	EV_Or
'0'	EV_IR_10to6	EV_ShiftLeft
'0'	EV_IR_10to6	EV_ShiftRight
'0'	*EV_IR_10to6*	EV_SetLessThan
'0'	*EV_IR_10to6*	EV_Add
'0'	*EV_IR_10to6*	EV_And
'0'	*EV_IR_10to6*	EV_Or
'0'	*EV_IR_10to6*	EV_SetLessThan
'0'	EV_16	EV_ShiftLeft
'0'	*EV_IR_10to6*	*EV_Add*
'0'	*EV_IR_10to6*	*EV_Add*
'0'	*EV_IR_10to6*	*EV_Add*
'0'	*EV_IR_10to6*	*EV_Add*