4-bit binary digital-to analog converter (DAC)

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ABSTRACT

For this bonus project I designed 4-bit binary digital-to-analog converter (DAC).
By using CMOS technology (1 micron, K_n'=25μA/V^2, K_p'=10μA/V^2, $V_{tn} = -V_{tp} = 0.8$ V, $\lambda = 0.01$) and assuming we have ±5 V supplies available, we produce a CMOS design of the converter.
The input is a parallel 4-bit word. The word changes every 100 μs (that is, a modest 10 kHz). The output is to be an analog signal with a minimum output of 0 V, and maximum at or near 1 V. Therefore, there are sixteen different output voltages, distributed evenly between 0V and 1 V. After that, I conducted a PSPICE simulation of my proposed design. The output of the simulation is the analog output of the DAC.

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1. Introduction

1.1 Background Information

Digital-to-analog conversion is a process in which signals having a few defined levels or states (digital) are converted into signals having a theoretically infinite number of states (analog). A common example is the processing of computer data into audio-frequency (AF) tones that can be transmitted over a twisted pair telephone line. The circuit that performs this function *is a* digital-to-analog converter (DAC).

Basically, digital-to-analog conversion is the opposite of analog-to-digital conversion. In most cases, if *an* analog-to-digital converter (ADC) *is* placed in a communications circuit after a DAC, the digital signal output is identical to the digital signal input. Also, in most instances when a DAC is placed after an ADC, the analog signal output is identical to the analog signal input.

Binary digital impulses, all by themselves, appear as long strings of ones(+5V) and zeros(0V), and have no apparent meaning to a human observer. But when a DAC is used to decode the binary digital signals, meaningful output appears. This might be a voice, a picture, a musical tune, or mechanical motion.

The intelligibility or fidelity of an analog signal can often be improved by converting the analog input to digital form using an ADC, then clarifying the digital signal, and finally converting the "cleaned-up" digital impulses back to analog form using an DAC.

1.2 The Presented Design

Figure 1 illustrates a weighted NMOS digital-to-analog converter which has a reference voltage source (+5V), a set of NMOS transistors instead of binary-weighted resistors, an inverting summing op-amp and a set of digital signal input ports instead of switches. From the diagram it can be noticed that each input port has it own binary bit of the digital input word which controls it. When the binary bit is 1 (switch is closed) the current flows through the Gate of each NMOS in series. Then, this makes NMOS saturated due to Drain voltage(V_D) and Gate voltage(V_G) is 5V. So, there is current between Drain and Source(I_D). When the current from all networks of NMOS are summed in the amplifier, the total current is proportional to the output voltage of the amplifier.

Since the currents sum together and go through R_f where the inverting input is 0V and $V_{out} = I_f R_f$. The input NMOS are proportional to the binary weights of the input bits. The lowest number of NMOS (R) corresponds to the lowest binary-weighted input ($2^0 = 1$). The other NMOS are multiples of R (i.e. 2R, 4R, and 8R) and the equivalent binary weight is 2^1, 2^2, and 2^3, respectively. The input current(I_D) is proportional to the binary weights and the output voltage is proportional to the sum of the binary weights. This is because the sum of all the input current(I_D) is through R_f(269.949Ω).

Since the lowest number(2^0) of NMOS corresponds to the lowest binary-weighted input(LSB) and the highest number(2^3) of NMOS corresponds to the highest binary-weighted input(MSB), V_{out} is actually inverted voltage. This is the reason that we need the inverting amplifier followed by the summing buffer amplifier. By putting same resistance (R1=R2=100Ω), we can easily implement the inverting amplifier circuit.

2. Design Procedure

Figure 2 is the summing amplifier with scaled resistors. This design was what we first came out. This is the simplest digital to analog conversion with scaled resistors. Since the currents sum together and go through Rf where the inverting input is 0V and Vout = IfRf. The input resistors are inversely proportional to the binary weights of the input bits. The input current is proportional to the binary weights and the output voltage is proportional to the sum of the binary weights. This is because the sum of all the input current is through Rf.
The disadvantage of the weighted resistor DAC is the numerous resistor values, which is really bad in IC design. For instance, if we take an 8-bit converter, the 8 resistors will range from R to 128R in binary weighted steps. Also, it requires too many different precision resistors and a large resistor value range. This type of DAC is very difficult to mass produce due to the range of resistors required.

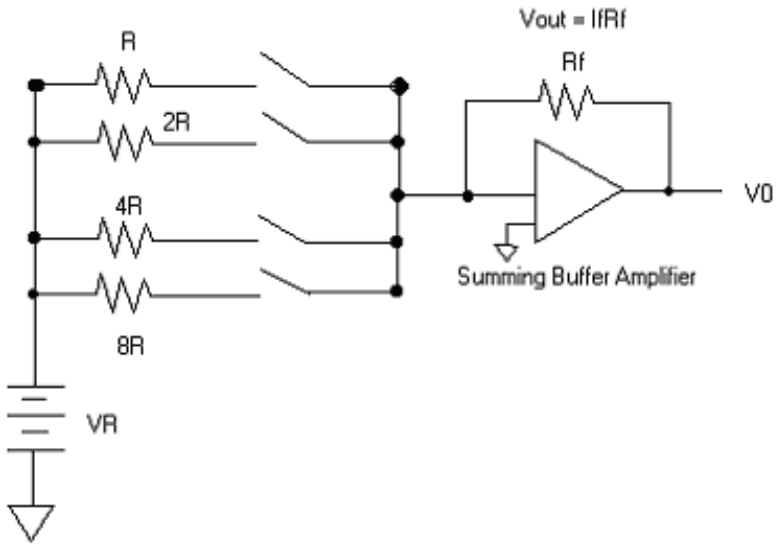


Fig 2. The summing amplifier with scaled resistors.

The next design we came up is R-2R Ladder DAC. This is a more clever circuit based on similar concepts but uses only two values of register. Comparing to above design, it requires much fewer resistors.
It is also easy to calculate the current through each resistor by voltage divider. The output scale can be stretched or compressed by varying the feedback resistor R

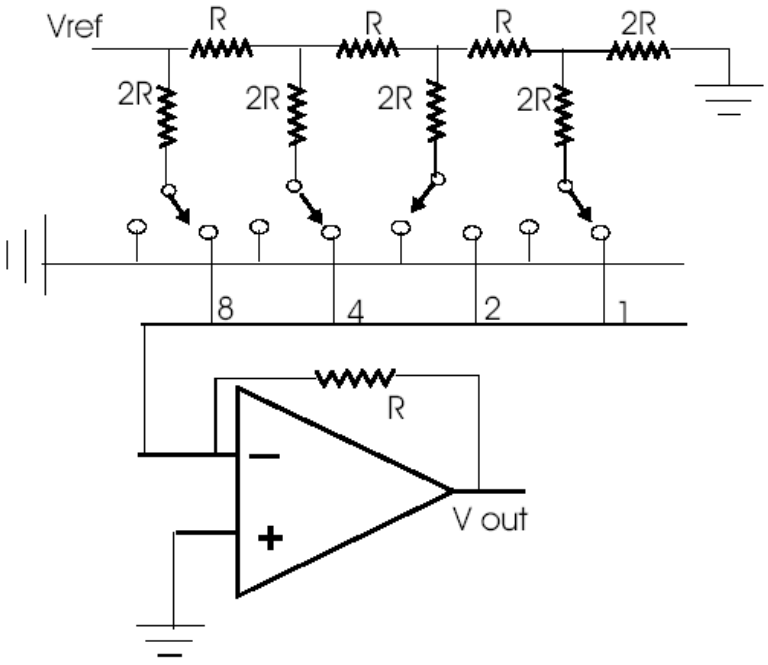


Fig 3. The R-2R ladder with summing amplifier.

3. Design Details

As I illustrated in introduction, Figure4 shows a weighted NMOS digital-to-analog converter which has a reference voltage source (+5V), a set of NMOS transistors instead of binary-weighted resistors, an inverting summing op-amp and a set of digital signal input ports instead of switches.
This design is pretty similar with the design in Figure2. But, weighted resistor DAC has somewhat disadvantages. One thing is the numerous resistor values. It requires too many different precision resistors. The other thing is total resistor value is really huge, which is also really bad in IC design. Therefore, we replaced every resistor with NMOS transistors.
NMOS transistor is 'on' when voltage between gate and source is greater than threshold voltage. Also, if voltage between gate and source is greater than voltage between drain and source, then NMOS transistors are saturated. We used this characteristic of NOMS instead of using just resistors.
From the Figure 4, when the binary bit is 1 (switch is closed 5V) the current flows through the gate of each NMOS in series. Then, this makes NMOS saturated due to drain voltage(V_D) and gate voltage(V_G) is 5V. So, there is current between Drain and Source(I_D).

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

From the formula above, we know K_n'=25μA/V^2, W/L = 1 (1 micron technology) V_{tn} = 0.8 V, λ =0.01, V_{GS} = 5V, and V_{DS} = 5 V.

So, by plugging these values into equation, we can have i_D value, which is

$$i_D = 2.31525 \text{ E} -4 \text{ (A)}$$

Let's suppose digital input is "0001"(DSTM0=1, DSTM1=0, DSTM2=0, DSTM3=0). Since M1 NMOS transistor is only saturated and other NOMS transistors are off, so the output voltage(V_{OUT}) should be 1/16(V).

$$\frac{i_D}{Rf} = \frac{1}{16} V$$

By plugging into i_D = 2.31525 E –4 (A) we can have the value of feedback resistor.

$$R_f = 269.949249\ \Omega$$

In summary, when the current from all networks of NMOS are summed in the amplifier, the total current is proportional to the output voltage of the amplifier.
Since the currents sum together and go through R_f where the inverting input is 0V and $V_{out} = I_f R_f$. The input NMOS are proportional to the binary weights of the input bits. The

input current(i_D) is proportional to the binary weights and the output voltage is proportional to the sum of the binary weights. This is because the sum of all the input current(I_D) is through R_f(269.949Ω).
Since the lowest number(2^0) of NMOS corresponds to the lowest binary-weighted input(LSB) and the highest number(2^3) of NMOS corresponds to the highest binary-weighted input(MSB), V_{out} is actually inverted voltage. This is the reason that we need the inverting amplifier followed by the summing buffer amplifier. By putting same resistance (R1=R2=100Ω), we can easily implement the inverting amplifier circuit.

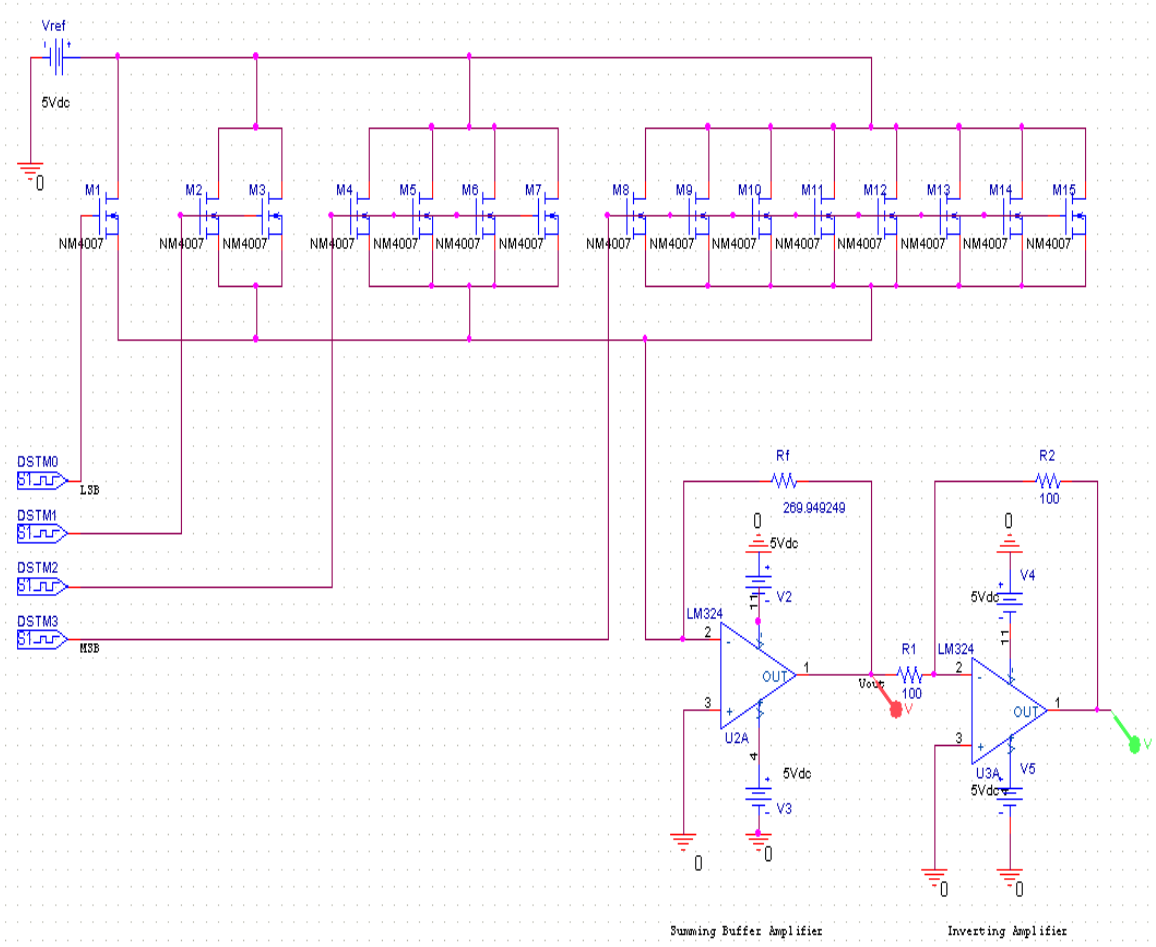


Fig. 4 DAC with NMOS and Inverting Amplifier

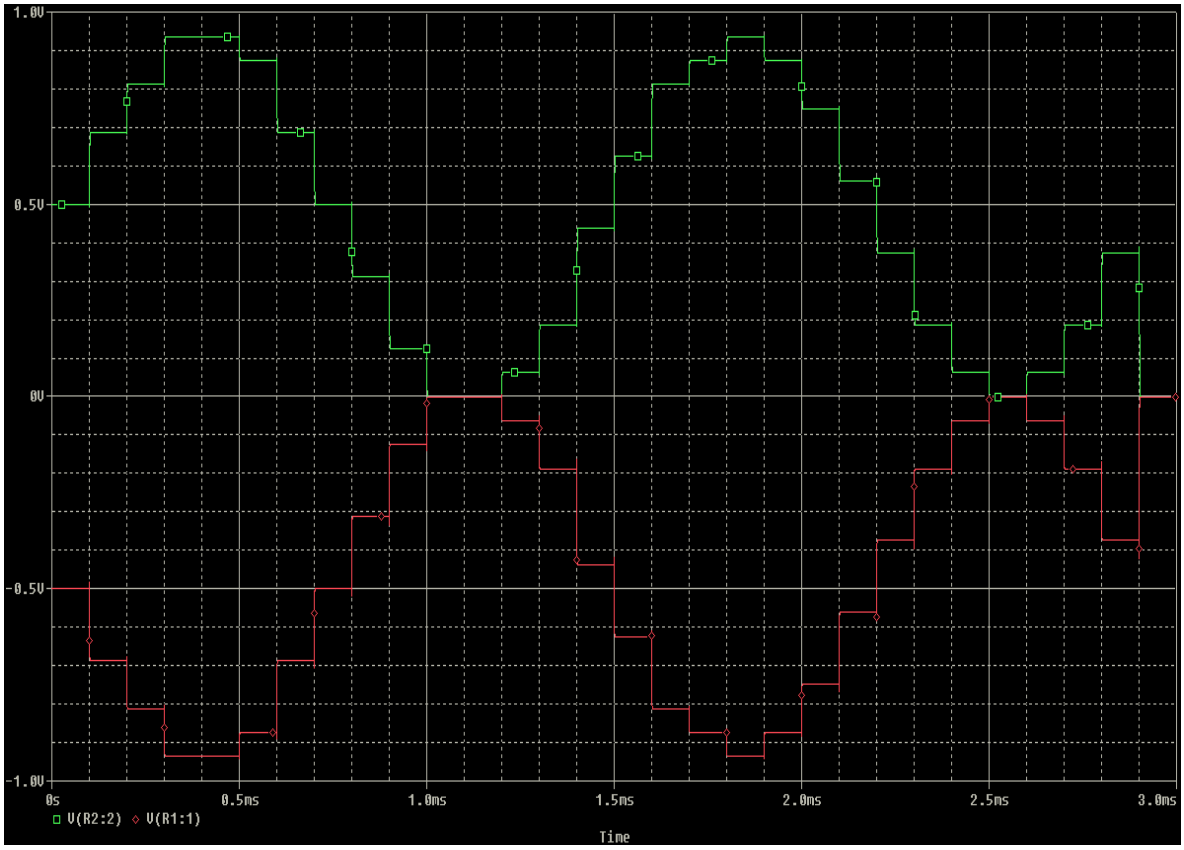


Fig. 5 Output simulation of DAC circuit

4. Relative Equation

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

$$i_D = \frac{1}{2} k_p' \frac{W}{L} (v_{SG} + V_t)^2 (1 + \lambda v_{SD})$$

$$V_{tn} = V_{t0} + \gamma \left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f} \right)$$

$$V_{tp} = V_{t0} - \gamma \left(\sqrt{2\phi_f + V_{BS}} - \sqrt{2\phi_f} \right)$$

$$\gamma = 0.5\sqrt{\mathrm{V}} \qquad 2\phi_f = 0.6\,\mathrm{V}$$

$$k_n' = \mu_n C_{ox}$$

5. Performance Analysis

Performance Characteristics of Digital-to-Analog Converters

Resolution:
The resolution of a DAC is the reciprocal of the number of discrete steps in the DAC. This is independent of the number of bits. Resolution can also be shown as the number of bits converted, which is 4bits.

Accuracy:
This is the comparison of the actual output of a DAC with the expected output. This is expressed as a percentage of a full scale, or maximum output voltage.
Linearity. A linear error is a deviation from the ideal straight-line output of a DAC.

Index	Data	Calculated Value (V)	Simulation Value (V)	Error Rate (%)	Index	Data	Calculated Value (V)	Simulation Value (V)	Error Rate (%)
1	8	0.5000	0.5242	0.95	16	10	0.6250	0.6553	0.95
2	11	0.6875	0.7209	0.95	17	13	0.8125	0.8520	0.95
3	13	0.8125	0.8520	0.95	18	14	0.8750	0.9175	0.95
4	15	0.9375	0.9831	0.95	19	15	0.9375	0.9831	0.95
5	15	0.9375	0.9831	0.95	20	14	0.8750	0.9175	0.95
6	14	0.8750	0.9175	0.95	21	12	0.7500	0.7864	0.95
7	11	0.6875	0.7209	0.95	22	9	0.5625	0.5898	0.95
8	8	0.5000	0.5242	0.95	23	6	0.3750	0.3931	0.95
9	5	0.3125	0.3276	0.95	24	3	0.1875	0.1965	0.95
10	2	0.1250	0.1309	0.95	25	1	0.0625	0.0654	0.96
11	0	0.0000	-0.0002	0.00	26	0	0.0000	-0.0002	0.00
12	0	0.0000	-0.0002	0.00	27	1	0.0625	0.0654	0.96
13	1	0.0625	0.0654	0.96	28	3	0.1875	0.1965	0.95
14	3	0.1875	0.1965	0.95	29	6	0.3750	0.3931	0.95
15	7	0.4118	0.4587	0.89					

Monotonicit:
A DAC is monotonic if it does not take any reverse steps then it is sequenced over its entire rage of input bits.

Setting Time:
This is the time it takes a DAC to settle within ±1/2 of a least significant bit of its final value when a change occurs in the input code.

Table 1. shows calculated value of given digital input value and I added PSPICE simulation value on APPENDIX

Index	Given Data	Binary representation of the given data				Time (ms)	Calculated Value (V)
		A3	A2	A1	A0		
1	8	1	0	0	0	0.0	0.5
2	11	1	0	1	1	0.1	0.6875
3	13	1	1	0	1	0.2	0.8125
4	15	1	1	1	1	0.3	0.9375
5	15	1	1	1	1	0.4	0.9375
6	14	1	1	1	0	0.5	0.875
7	11	1	0	1	1	0.6	0.6875
8	8	1	0	0	0	0.7	0.5
9	5	0	1	0	1	0.8	0.3125
10	2	0	0	1	0	0.9	0.125
11	0	0	0	0	0	1.0	0
12	0	0	0	0	0	1.1	0
13	1	0	0	0	1	1.2	0.0625
14	3	0	0	1	1	1.3	0.1875
15	7	0	1	1	1	1.4	0.4118
16	10	1	0	1	0	1.5	0.625
17	13	1	1	0	1	1.6	0.8125
18	14	1	1	1	0	1.7	0.875
19	15	1	1	1	1	1.8	0.9375
20	14	1	1	1	0	1.9	0.875
21	12	1	1	0	0	2.0	0.75
22	9	1	0	0	1	2.1	0.5625
23	6	0	1	1	0	2.2	0.375
24	3	0	0	1	1	2.3	0.1875
25	1	0	0	0	1	2.4	0.0625
26	0	0	0	0	0	2.5	0
27	1	0	0	0	1	2.6	0.0625
28	3	0	0	1	1	2.7	0.1875
29	6	0	1	1	0	2.8	0.375

Table 1. Calculated value of given input.

6. Design Limitation

Although this project was a fairly open assignment, the presented design was limited in several ways. First, the disadvantage of the weighted resistor DAC is the numerous resistor values. For instance, if we take an 8-bit converter, the 8 resistors will range from R to 128R in binary weighted steps. This type of DAC is very difficult to mass produce due to the range of resistors required where the tolerance is less than 0.5% to accurately convert the input. Second, because the project needs to be completed in approximately one months, it was not possible to explore some interesting advanced designs. And, we just simulated the output result with op-amps given in the library. However, I added our own amplifier design on APPENDIX even though we did not test with this amplifier.

REFERENCES

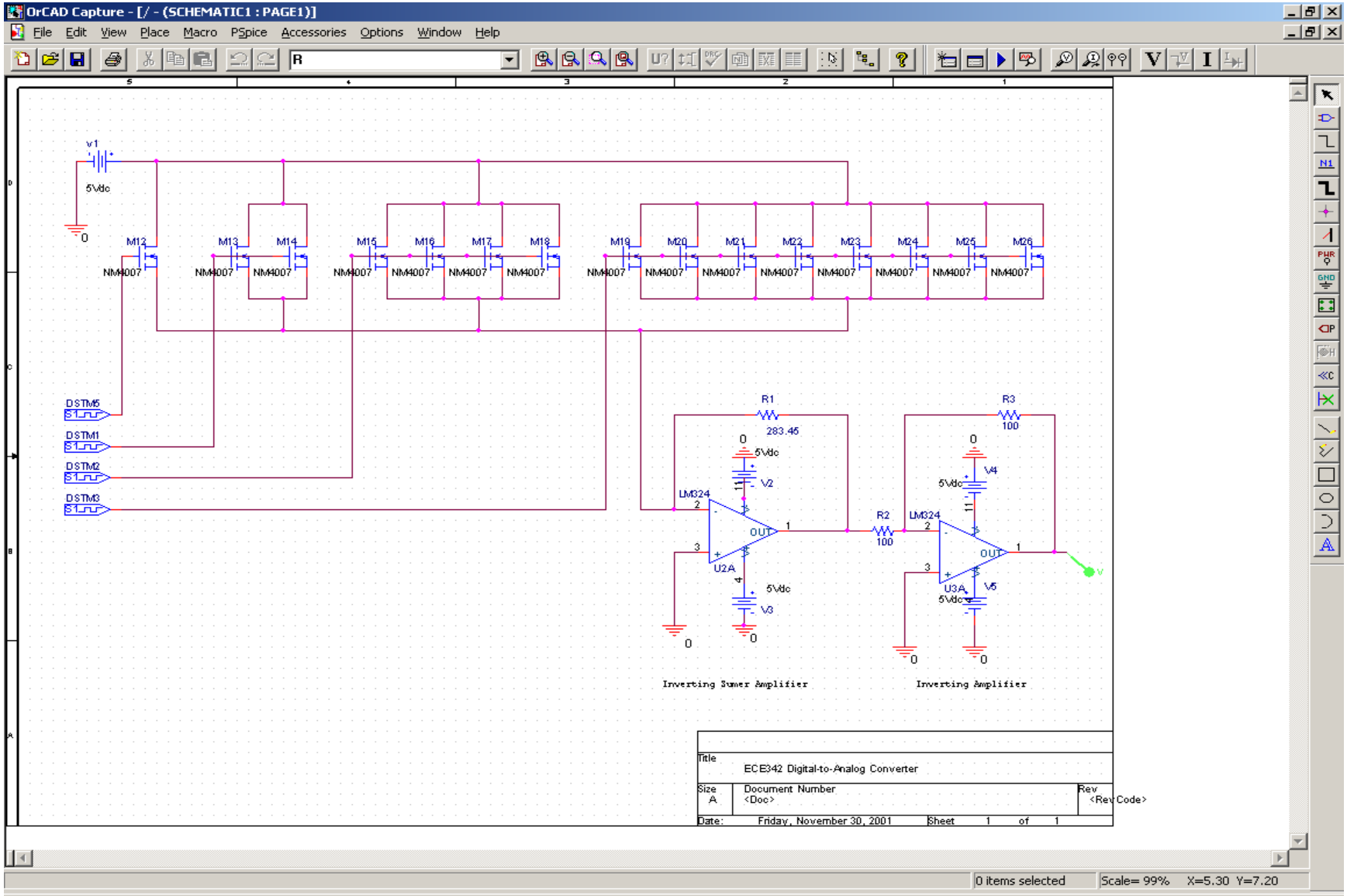
[1] D. C. Munson, Jr., "*ECE 310 Course Notes*," class notes for ECE 310, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Fall 1999.

[2] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. New York: Oxford University Press, 1998.

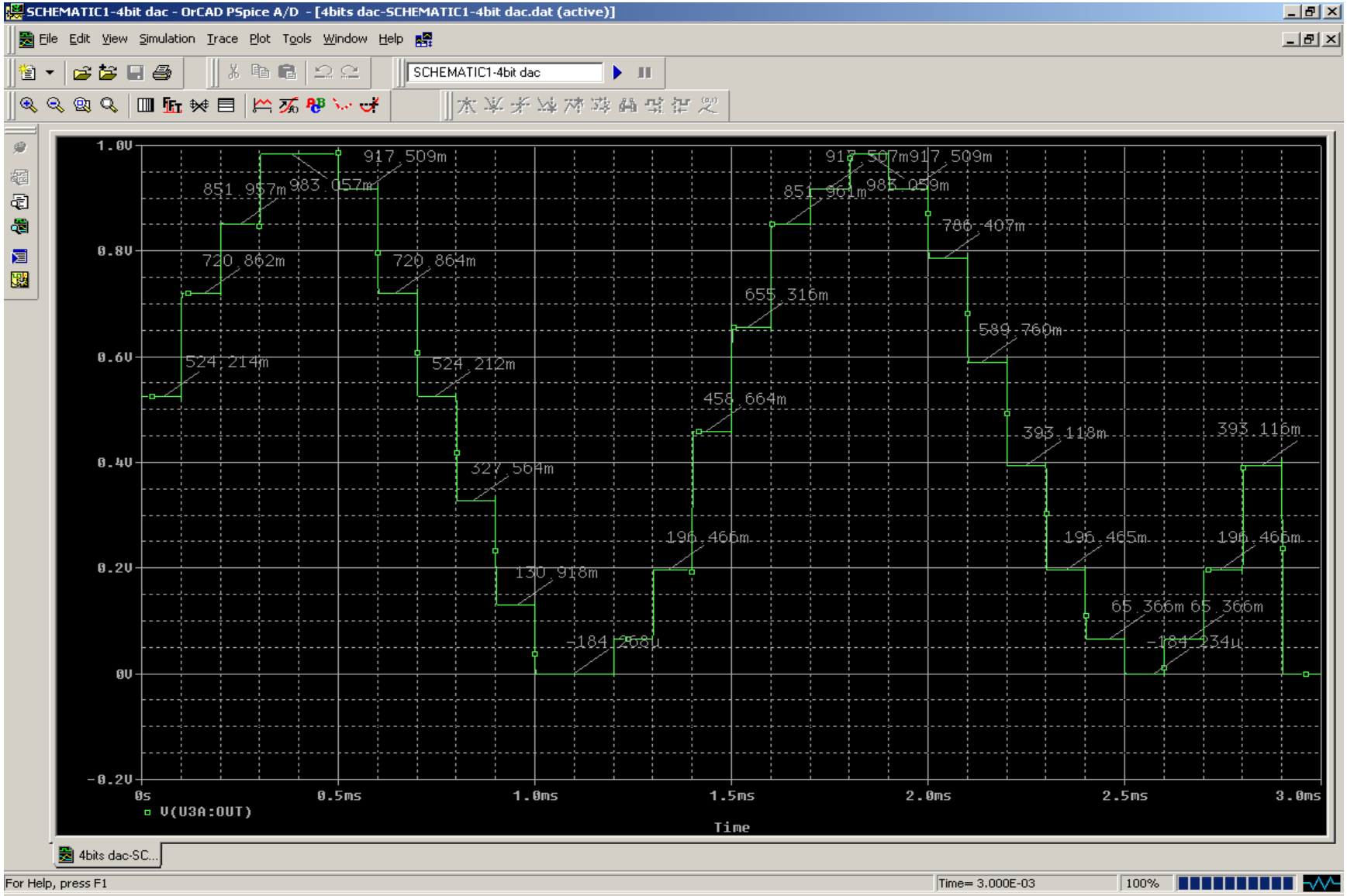
[3] B.P. Lathi, *Signal Processing and Linear Systems*. California: Berkeley Cambridge Press, 1998.

[4] D. C. Munson, Jr., "*ECE 210 Course Notes*," class notes for ECE 210, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Spring 1999.

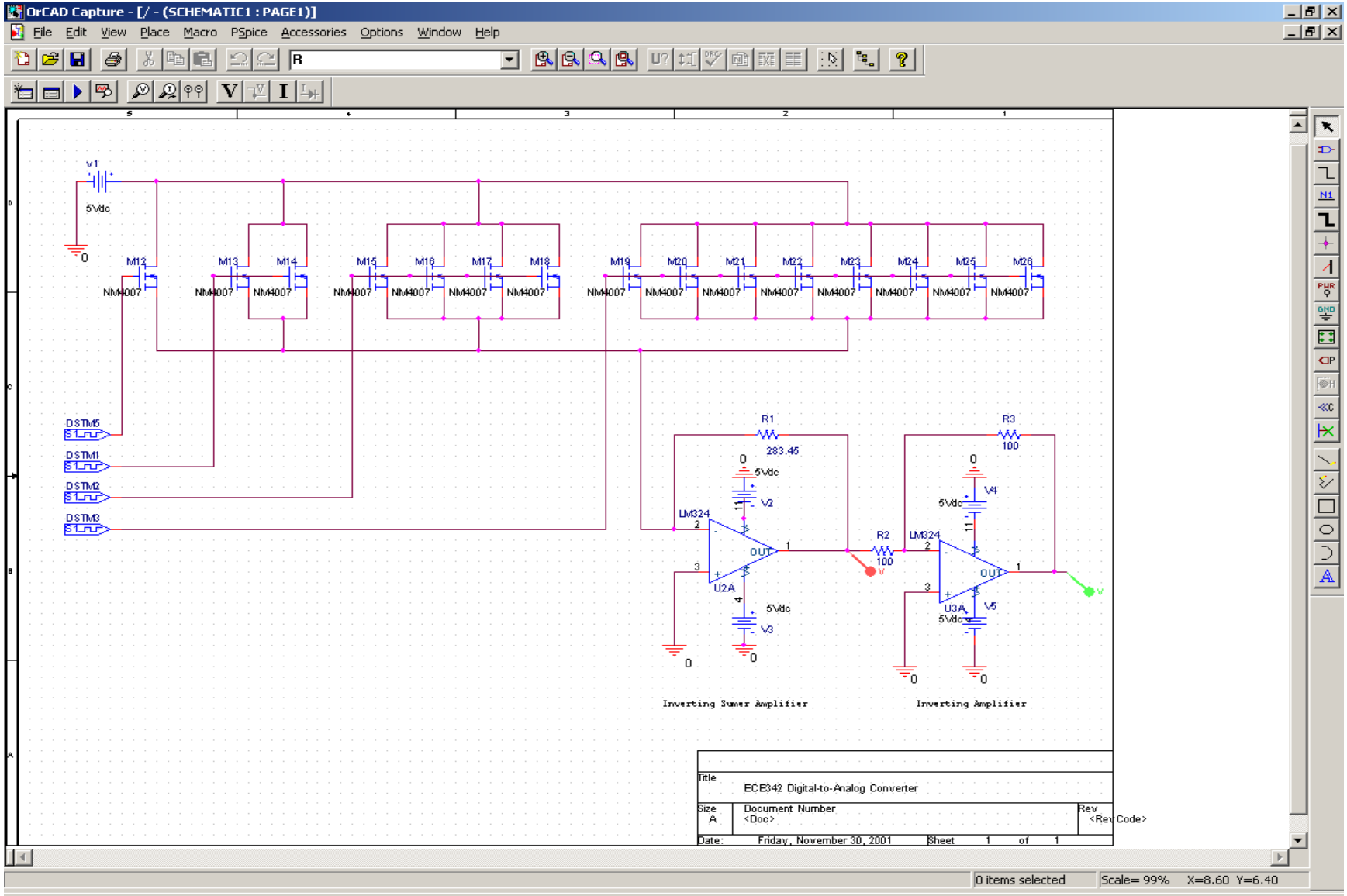
APPENDIX



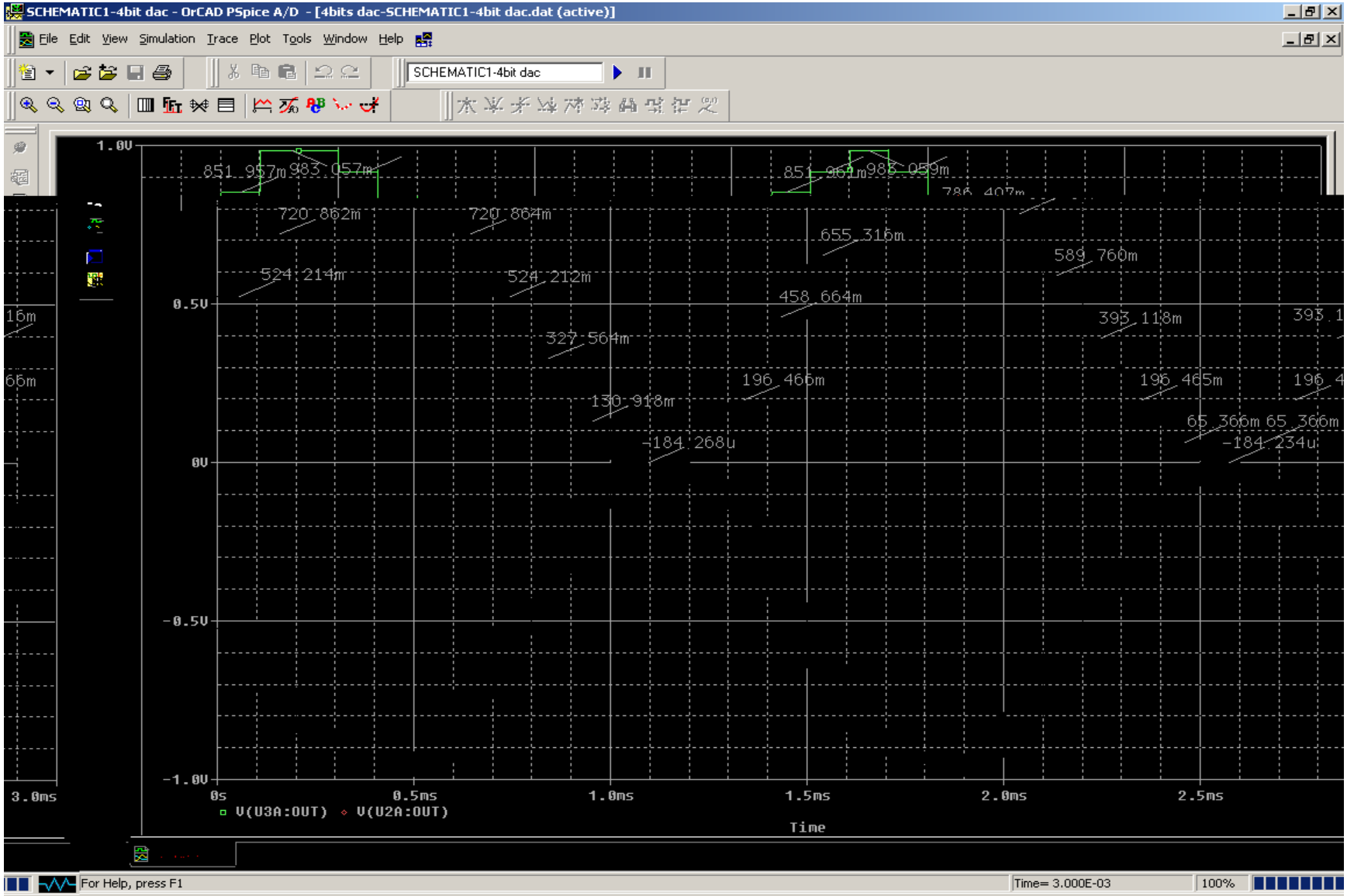
4bit Binary digital-to-analog converter



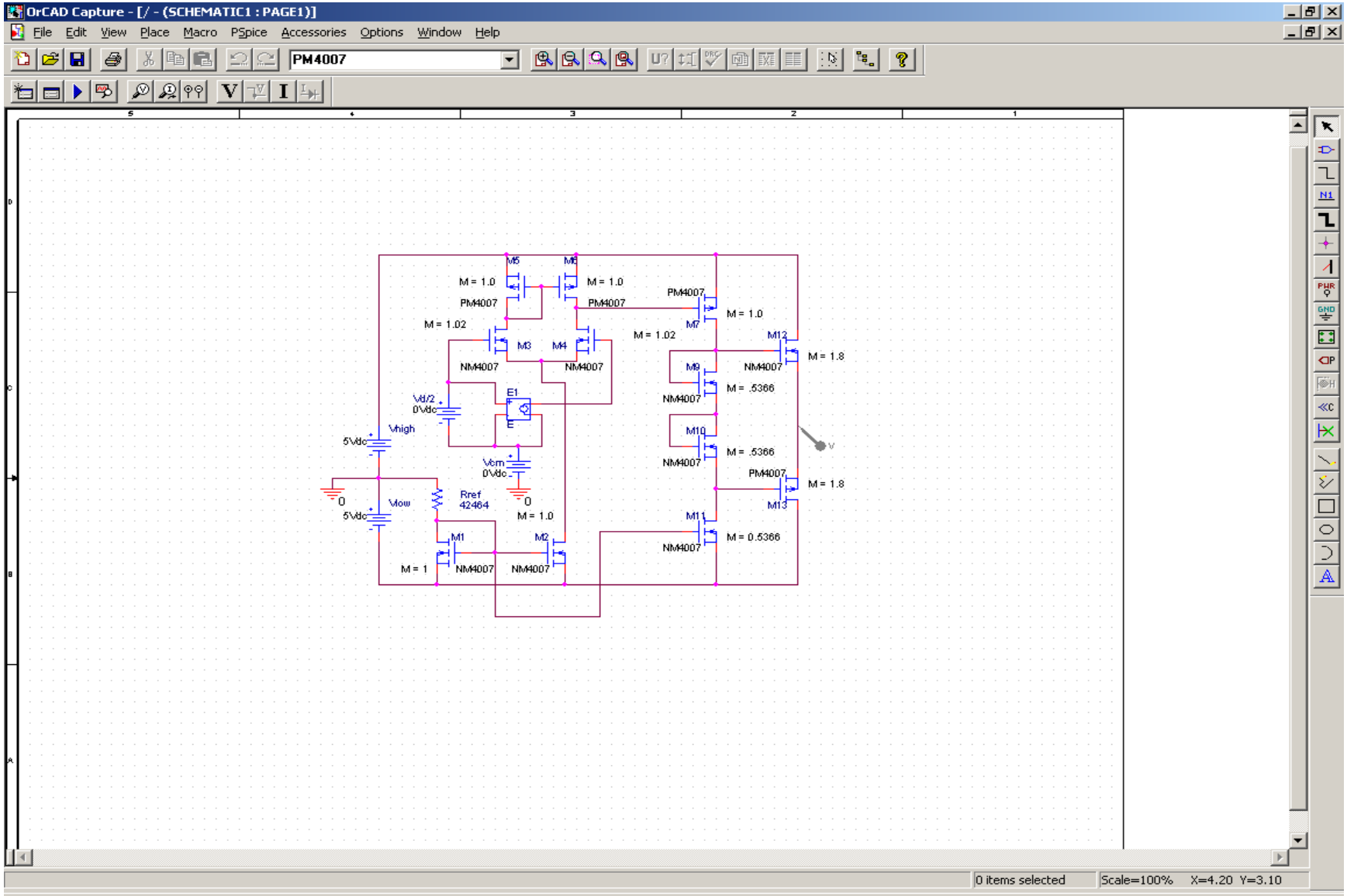
Simulation result of 4bit DAC. Output range is between 0V and 1V.



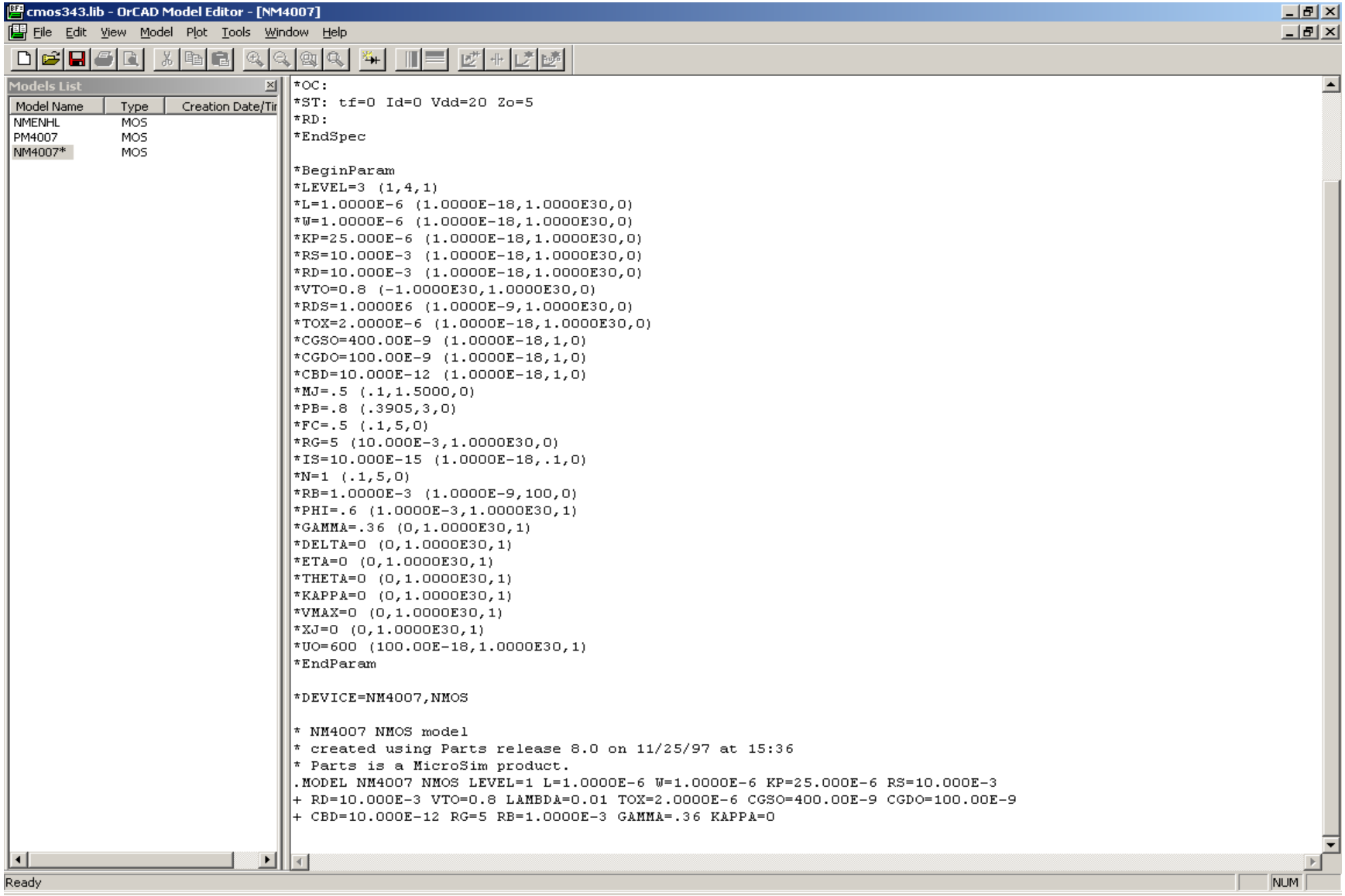
4bit Binary digital-to-analog converter



Simulation result of 4bit DAC. Red line is output before the inverting amplifier.



Operational Amplifier



NMOS Characteristics for 4bit DAC