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Theory, Design and Simulation of a Distribution STATCOM for Mitigation of Voltage Sag and Elimination of Harmonic

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ABSTRACT

This paper describes the theory, design and simulation of a 12-pulse Distribution STATCOM on an 11kV distribution system. The distribution STATCOM (D-STATCOM) is one of the custom power (CP) family which also includes dynamic voltage restorer (DVR), solid state fault current limiter (SSFCL), active filters and solid state transfer switch (SSTS). Custom power offers customer with no power interruptions, tight voltage regulation, low harmonic voltage and acceptance of fluctuating and non-linear loads without effect on the terminal voltage. The D-STATCOM, which consists of a thyristor-based voltage source inverter, uses advanced power electronics to provide voltage stabilization, flicker suppression, power factor correction, harmonic control and a host of other power quality solutions for both utility and industrial applications. In this paper however, the concern will be mitigating voltage sags on the 11kV distribution system and reduction of harmonics generated by the device. The D-STATCOM simulations are done by using the PSCAD/EMTDC version 3.0.7 electromagnetic transient program.

1. INTRODUCTION

Voltage sag is the most important power quality problems faced by many industries and utilities. It contributes more than 80% of power quality (PQ) problems that exist in power systems [1]. By defintion, a voltage sag is an rms reduction in the AC voltage at the power frequency, for duration from a half-cycle to a few seconds [2]. Voltage sags are not tolerated by sensitive equipment used in modern industrial plants such as process controllers, programmable logic controllers (PLC), adjustable speed drive (ASD) and robotics [1]. It has been reported that, high intensity discharge lamps used for industrial illumination get extinguished at voltage sags of 20% and industrial equipments like PLC and ASD are adversely affected by voltage sags of about 10% [3].

Various methods have been applied to reduce or mitigate voltage sags. The conventional methods are by using capacitor banks, introduction of new parallel feeders and by installing uninterruptible power supplies (UPS). However, the PQ problems are not solved completely due to uncontrollable reactive power compensation and high costs of new feeders and UPS. The D-STATCOM has emerged as a promising device to provide not only for voltage sags mitigation but a host of other power quality solutions such as voltage stabilization, flicker suppression, power factor correction and harmonic control [4]. The D-STATCOM has the added capability to sustain reactive current at low voltage, reduce land use and can be developed as a voltage and frequency support by replacing capacitors with batteries as energy storage [5].

In this paper, the configuration and design of the D-STATCOM will be explained in brevity. The designed D-STATCOM will then be connected in shunt to study 11 kV distribution system. Passive filters will be employed to reduce the harmonics present in the output of the D-STATCOM which exceed the limits by IEEE standards. This paper focuses on mitigating voltage sags and reduction of harmonics generated. Simulation results on the performance of the D-STATCOM for voltage sag mitigation and harmonic reduction will be shown and explained.

2. BASIC CONFIGURATION AND OPERATION OF D-STATCOM

The D-STATCOM is a three-phase shunt connected power electronics based device. It is connected near the load at the distribution systems. The major components of a D-STATCOM are shown in Fig. 1. It consists of a dc capacitor, three-phase inverter (GTO, thyristor) module, ac filter, coupling transformer and a control strategy [5]. The basic electronic block of the D-STATCOM is the voltage-sourced inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency.

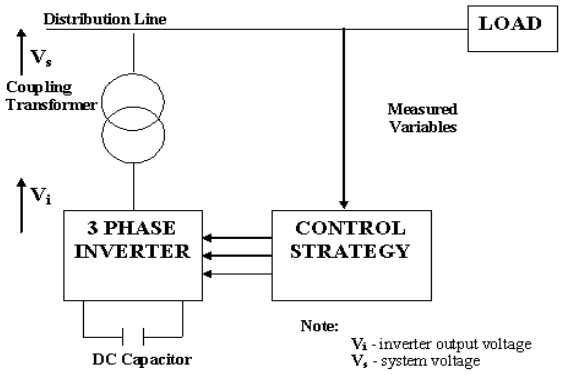
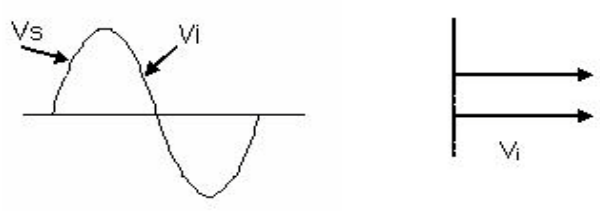
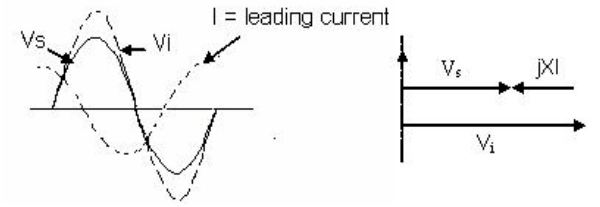


Fig. 1: Basic Building Blocks of the D-STATCOM

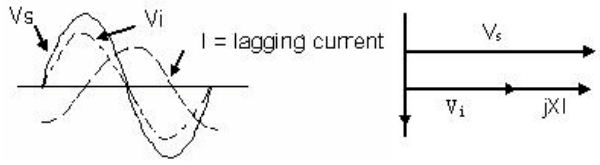
The controller of the D-STATCOM is used to operate the inverter in such a way that the phase angle between the inverter voltage and the line voltage is dynamically adjusted so that the D-STATCOM generates or absorbs the desired VAR at the point of connection. The phase of the output voltage of the thyristor-based inverter, V_i, is controlled in the same way as the distribution system voltage, V_s. Figure 2 shows the three basic operation modes of the D-STATCOM output current, I, which varies depending upon V_i. If V_i is equal to V_s, the reactive power is zero and the D-STATCOM does not generate or absorb reactive power. When V_i is greater than V_s, the D-STATCOM 'sees' an inductive reactance connected at its terminal. Hence, the system 'sees' the D-STATCOM as a capacitive reactance. The current, I, flows through the transformer reactance from the D-STATCOM to the ac system, and the device generates capacitive reactive power. If V_s is greater than V_i, the system 'sees' an inductive reactance connected at its terminal and the D-STATCOM 'sees' the system as a capacitive reactance. Then the current flows from the ac system to the D-STATCOM, resulting in the device absorbing inductive reactive power [4].



a) No-load mode ($V_s = V_i$).



b) Capacitive mode ($V_i > V_s$).



c) Inductive mode ($V_i < V_s$).

Fig. 2: Operation modes of D-STATCOM.

Figure 3 shows a typical 12-pulse inverter arrangement utilizing two transformers with their primaries connected in series [6]. The first inverter is connected to the system through a Y-Y arrangement, whereas a Y-Δ connection is used for the second inverter. Each inverter operates as a 6-pulse inverter, with the Y-Δ inverter being delayed by 30^0 with respect to the Y-Y inverter. The current flowing into each inverter is the same, scaled by the transformer ratio, as the current being drawn from the system by the D-STATCOM. For the Y-Δ inverter, the current is also delayed by 30^0 with respect to the current of the Y-Y inverter [6].

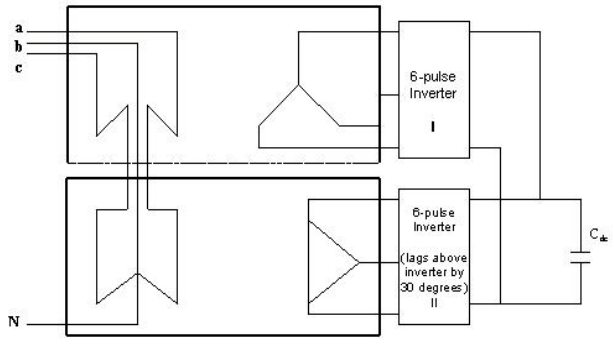


Fig. 3: The 12-pulse D-STATCOM arrangement.

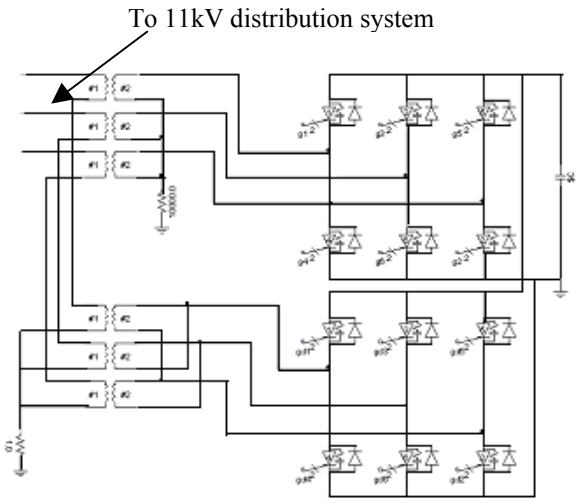


Fig. 4: The proposed D-STATCOM configuration.

3. DESIGN OF THE 12-PULSE D-STATCOM AND CONTROL SYSTEM

Figure 4 shows the proposed 12-pulse D-STATCOM configuration with the GTO's used as power devices. The GTOs are connected anti parallel with diodes for commutation purposes and charging of the DC capacitor [7].

The DC side of D-STATCOM is connected in parallel to keep the voltage on the DC side as low as possible and to improve utilization of the DC side capacitor. The first transformer is in wye-to-wye connection and the second transformer is in wye-to-delta connection. This is to give a 30^0 phase shift between the pulses and to reduce harmonics generated from the D-STATCOM. Both transformers are 11:2 kV step down transformers. The D-STATCOM is connected in shunt to the system. The 11kV distribution system is assumed loaded with 500kVA load at 0.9 pf lagging.

Controls of D-STATCOM are mainly manipulating the injection or absorption of reactive power by the DC capacitor. So, the proper size of capacitor is very important. The capacitor voltage, V_{DC}, controls the direction and magnitude of the D-STATCOM current.

The coupling transformer in Fig. 3 is used to produce a 12-pulse voltage. The phase voltages of inverter II lag the phase voltages of inverter I by 30^0 which compensates for the 30^0 phase lag of the delta connected inverter II. This can be achieved by time advancing the gate pulses of inverter II with respect to those of inverter I.

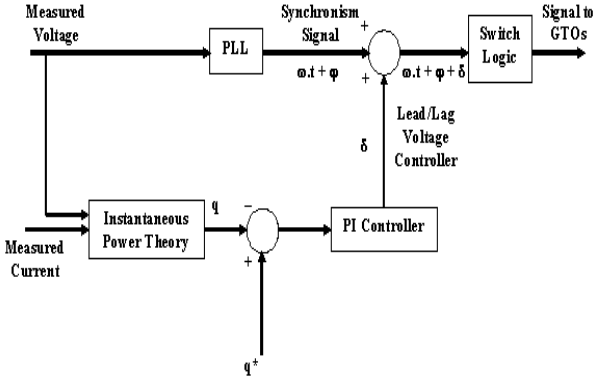


Fig. 5: The D-STATCOM control blocks.

Figure 5 shows control diagram of D-STATCOM constructed by PI controller. The PI controller provides the required phase angle for the inverters' switching pattern. Reactive power feedback using a PI controller makes it possible to improve transient response of the reactive power. The calculated reactive power, q, and reference reactive power, q*, are applied to the PI controller. The output of the PI controller is reference signal representing the phase angle δ.

The phase information, ωt, is generated from a signal generated by a phase locked loop (PLL) circuit. The phase comparator compares δ angle with ωt and determines the time which the corresponding switching devices are turned on and off. Each time the δ angle is changed, the dc capacitor voltage changes. The reactive power from the system is compared to the reference per-unit voltage which contributes to the change in phase shift [8]. The control system is based on the sinusoidal pulse width modulated switching method.

4. SIMULATION RESULTS AND DISCUSSION

In the simulation study, the voltage sags introduced to the system was done by the three-phase fault component from the PSCAD/EMTDC software's library.

Figure 6 shows the components used to generate voltage sag. By changing the fault impedance we will get different level of voltage sags. This is illustrated in Fig. 7.

The system was simulated for three seconds with the three-phase balanced fault occurring at time

1.5sec for a duration of 0.6 sec. Figure 8 shows the per-unit voltage, current and voltage profiles of the system. From Fig. 8, we can see that due to the three-phase fault, voltage sag has occurred.

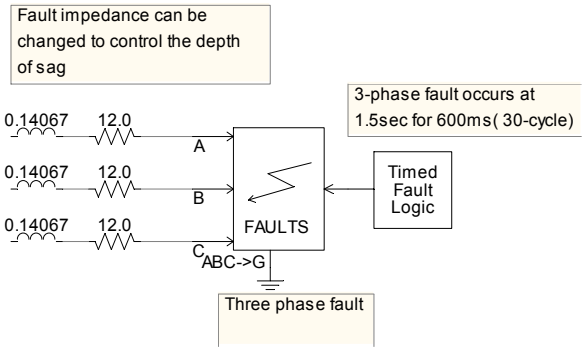


Fig. 6: Three-phase fault component to Introduce voltage sag.

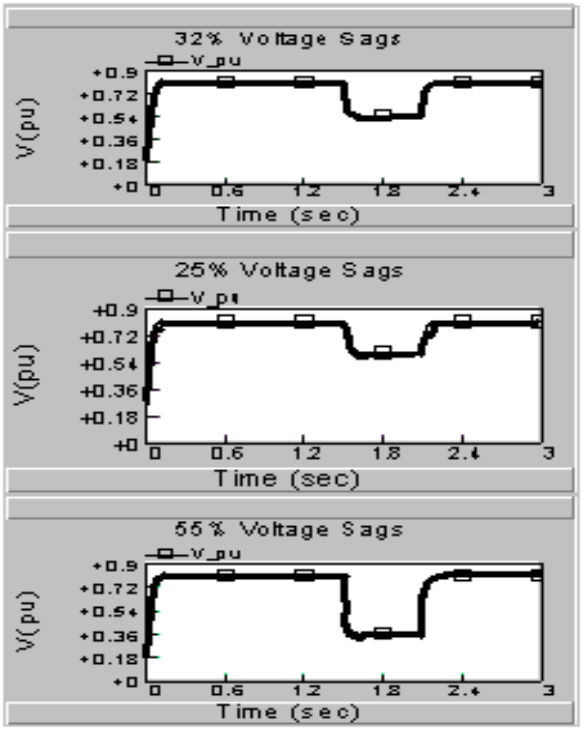


Fig. 7: Different voltage sags percentage due to different fault impedance.

The percentage of sag for the system is calculated using the following equation,

$$Sag(\%) = \frac{V_{pre-sag}(p.u) - V_{sag}(p.u)}{V_{pre-sag}(p.u)} \times 100$$
$$= \frac{0.81 - 0.55}{0.81} \times 100 \qquad (1)$$
$$= 32.1\%$$

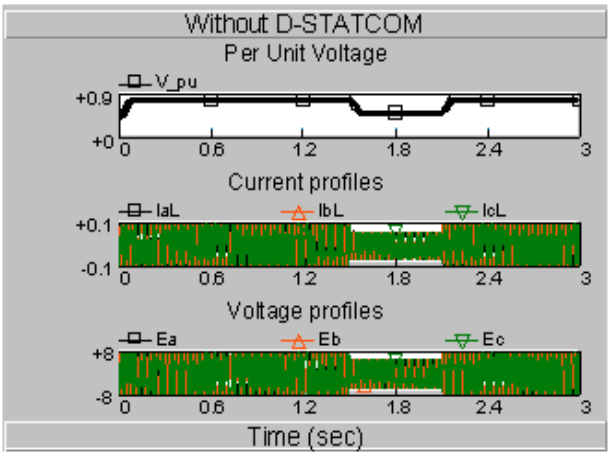


Fig. 8: Voltage (p.u), current (kA) and voltage (kV) of the System during voltage sag condition.

It is evident from the graphs shown in Fig. 8 that the line current, $I_{L\text{-}L}$ (rms), dropped from 89A to 62A and the line voltage, $V_{L\text{-}L}$, dropped from 7.344kV to 4.97kV. The DC capacitor value is calculated by trial and error. It was found out later through simulation works that the capacitance of $C_{DC} \approx 220\mu F$ is responding well to sustain the system's voltage during the fault.

The VAR rating of the D-STATCOM when C_{DC}=220μF is calculated as

$$\text{VAR} = 314.2 \times C_{DC} \times V_{L-L}^2 . \qquad (2)$$

$V_{L\text{-}L}$ is the nominal line-to-line voltage of the system at the point of connection of the filter. For this case, $V_{L\text{-}L}$ = 6.93kV. The VAR rating of the D-STATCOM is 3.3 MVAR.

4.1 Mitigation of Voltage Sags by D-STATCOM

The D-STATCOM is now connected in shunt with the 11kV system and the simulation is set to run again for 3sec. The switching frequency of the PWM control is set at 1.65kHz. Figures 9 and 10 show the results obtained from the simulation. From Fig. 9, it can be seen that the system's per unit voltage was maintained at 1.0 p.u. The spikes at the beginning and end of sag are due to capacitor charging and discharging. Figure 10 also shows the duration of voltage sag from 1.5s to 2.1s and during this period the D-STATCOM responds well to give the system better ride through capability. The sag was mitigated within 90 ms and limited to less than 20% of sag before the system recovered to 1.0 p.u.

Figure 10 shows that the D-STATCOM through the control feedback, the angle order is always kept at 30^0 between the 12 pulses. This is to prevent the increase of harmonics in the system. It can be seen that the DC current of the DC capacitor is fluctuating from negative to positive. This is due to the capacitor charging and discharging. The primary voltage of the 11:2 kV transformer, i.e. the system voltage, is maintained at about 11kV during the duration of sag. This proves that the D-STATCOM works very well in compensating the voltage sag caused by the balanced three-phase fault.

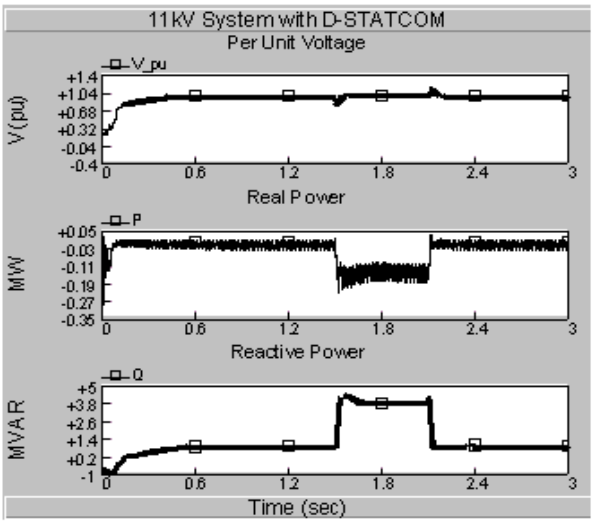


Fig. 9: 11kV system with D-STATCOM : V (p.u), real and reactive power.

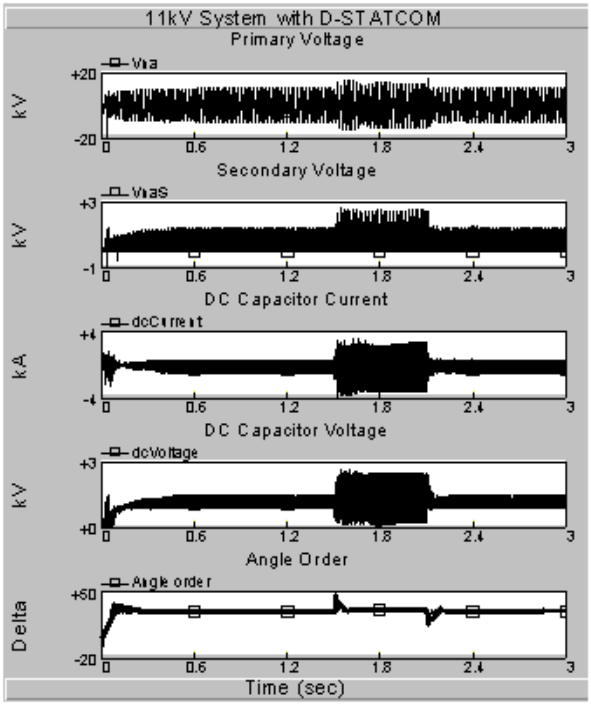


Fig. 10: System responses with the D-STATCOM.

4.2 Reduction of Harmonics Generated by D-STATCOM

IEEE Std. 519-1992 "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems" suggests limits for the total harmonic distortion (THD) of voltage at the point of common connection for low voltage and medium voltage systems. It suggests that for systems 69kV and below the limit of THD is 5.0% [9].

When the D-STATCOM is connected to the 11kV distribution system without the passive filters, the THD of the system was 14% and 24% before and during the sag respectively. When the sag is cleared the THD returns to 14% which is more than the limit. Figure 11 shows the THD of the system without passive filters.

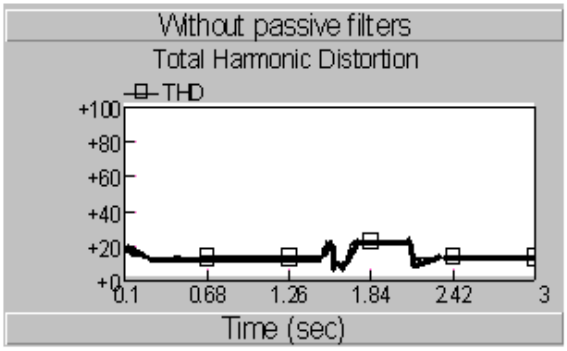


Fig. 11: THD of the system without filters.

In order to reduce harmonics generated by the D-STATCOM to below 5%, passive LC filters are employed. These filters can be connected to the primary side of the 11:2 kV transformer.

Initially, the dominant harmonics generated by the D-STATCOM are determined. Characteristic harmonics are related to the pulse number of the D-STATCOM. Since we are using the 12-pulse D-STATCOM the general characteristic harmonics equation is $12n \pm 1$, where n is an integer having values of 1, 2, 3 etc [9].

The dominant harmonics generated by the D-STATCOM are the 11^{th}, 13^{th}, 23^{rd} and 25^{th}. To find the values of L and C, the following equation is used,

$$\omega_0 = \frac{1}{\sqrt{LC}}, \qquad (4)$$

where ω_0 = resonant frequency.

The values calculated for L and C for 11th, 13th, 23rd and 25th harmonics are as follows:

$C_{11} = 2.2\mu F$ $L_{11} = 38.1mH$,
$C_{13} = 2.2\mu F$ $L_{13} = 27.3mH$,
$C_{23} = 2.2\mu F$ $L_{23} = 8.71mH$,
$C_{27} = 2.2\mu F$ $L_{27} = 7.37mH$.

These filters were connected in shunt to the D-STATCOM and the THD of the system was reduced to about 3%. This value is lower than the 5% THD limit [9]. Figure 12 shows the THD when passive filters were connected to the system.

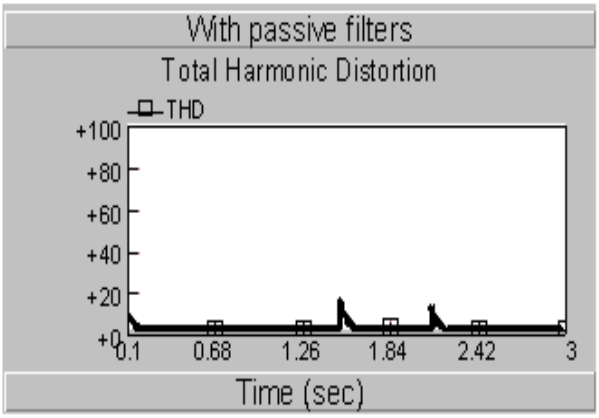


Fig. 12: THD of the system with filters.

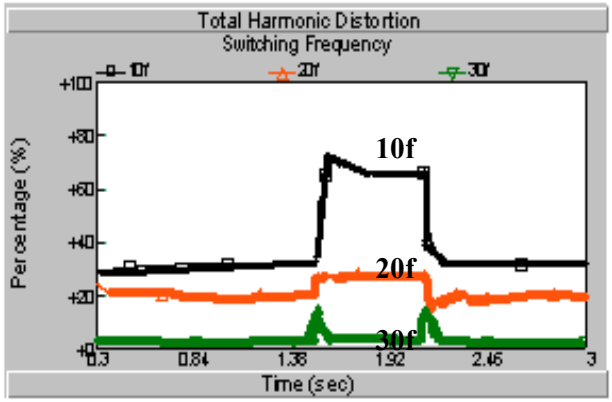


Fig. 13: THD of the system with different switching frequencies.

Figure 13 shows the reduction in THD of the system when the carrier frequency is increased. Here, *f* denotes the operating frequency of the system, which is 50 Hz. Care has to be taken when using higher switching frequency, for example 40*f*, 50*f* etc. The increase in switching frequencies mean greater stresses on the switching devices and therefore derating of the devices and also there is possibility of generation of high frequency harmonics component previously not present [13].

5. CONCLUSIONS

A simulation model of the 12-pulse D-STATCOM has been designed using the PSCAD/EMTDC program. An important aspect considered in the design is the control system. The control strategy for the D-STATCOM was the AC side voltage or reactive power control. PI controller is used to control the flow of reactive power to and from the DC capacitor. Phase Lock Loop components were used in the control to generate the switching signal, i.e. triangular waves, and reference signals, i.e. sinusoidal wave. PWM switching control was used to switch on and off the GTO's. The GTO's were connected inversely and parallel to diodes for commutation purposes and to charge the capacitor. Due to this type of control, the harmonics generated by D-STATCOM are lessened. GTOs are used in this simulation because it is easy to control the switch on and off of their gates and suitable for the designed D-STATCOM system.

From the simulation results, the designed D-STATCOM responded well in mitigating voltage sag caused by three-phase balanced fault. The DC capacitor value is dependent on the percentage of voltage sag. The difference of step drop load current during sag is the amount of reactive current needed to be compensated. For the 12-pulse D-STATCOM, the number of harmonics generated are in the order of $12n \pm 1$, n is an integer from 1, 2, 3, ...etc. The dominant harmonics are the 11th, 13th, 23rd and 25th harmonics. These harmonics are significantly reduced by connecting the passive filters to the system.

Lastly, the D-STATCOM is a promising device and will be a prominent feature in power systems in mitigating power quality related problems in the near future.

A new computational technique based on FMM-MoM for the solution of electromagnetic scattering problem has been proposed in this paper. As we know, MoM forms dense matrix that requires large amount of storage memory and CPU time. On the other hand, FMM generates a sparse matrix, that can save storage memory and CPU time. However, in the accuracy level of MoM is better than FMM. In our proposed method we optimized in between two methods to get the maximum advantages.

Our proposed method is tested for analyzing scattering from a simple conducting cylindrical body and the results are compared with those obtained by MoM and FMM. Results show the appropriateness of our method. For a body with large dimension and complex structure, extra care must be taken for the discretization, choice of expansion function, etc. The proposed method may be applied to other arbitrary shaped 2D as well as 3D electromagnetic problems.

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