Request

Productivity Gains through Re-Use and Quality Improvements of *HW* Models

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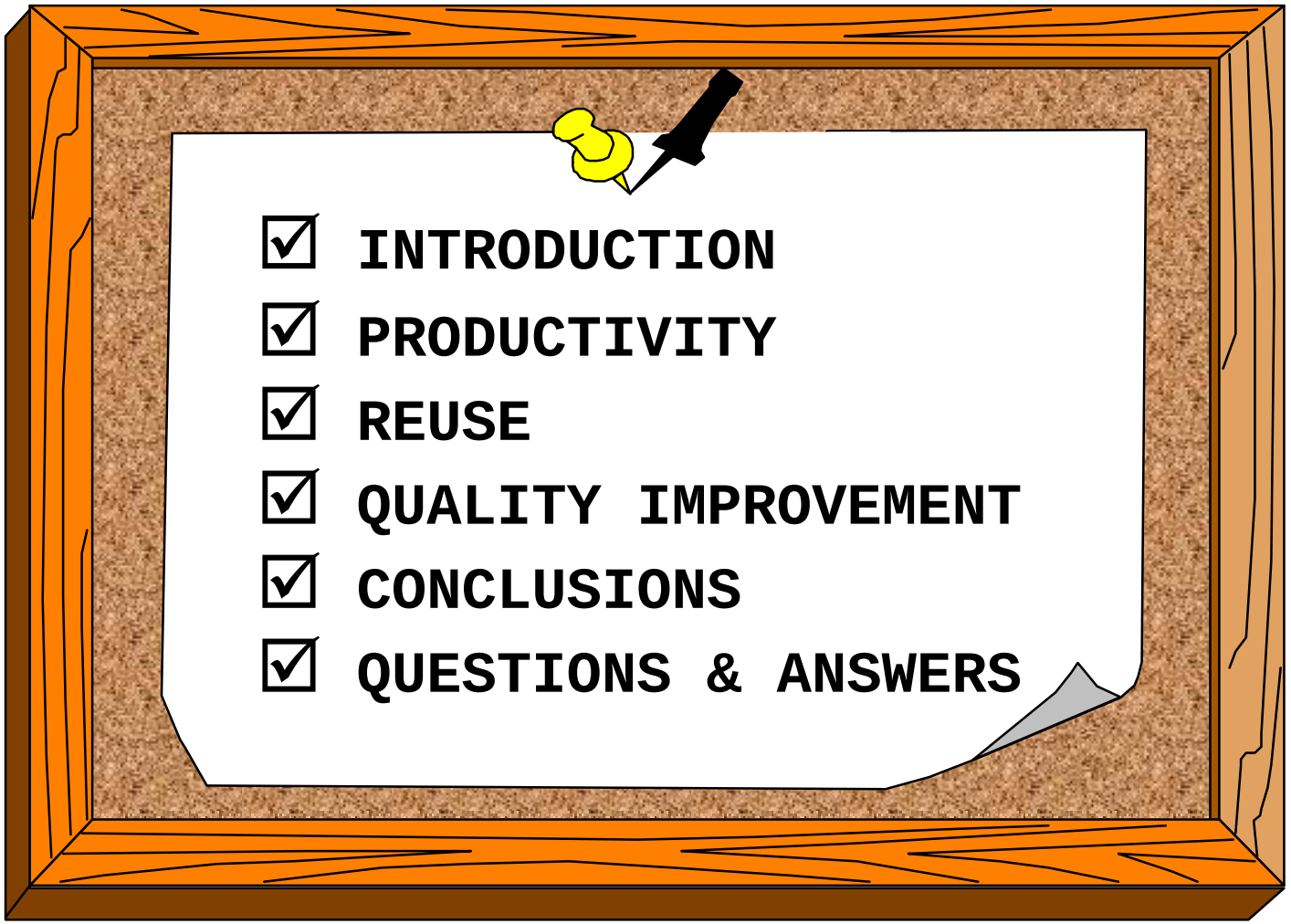
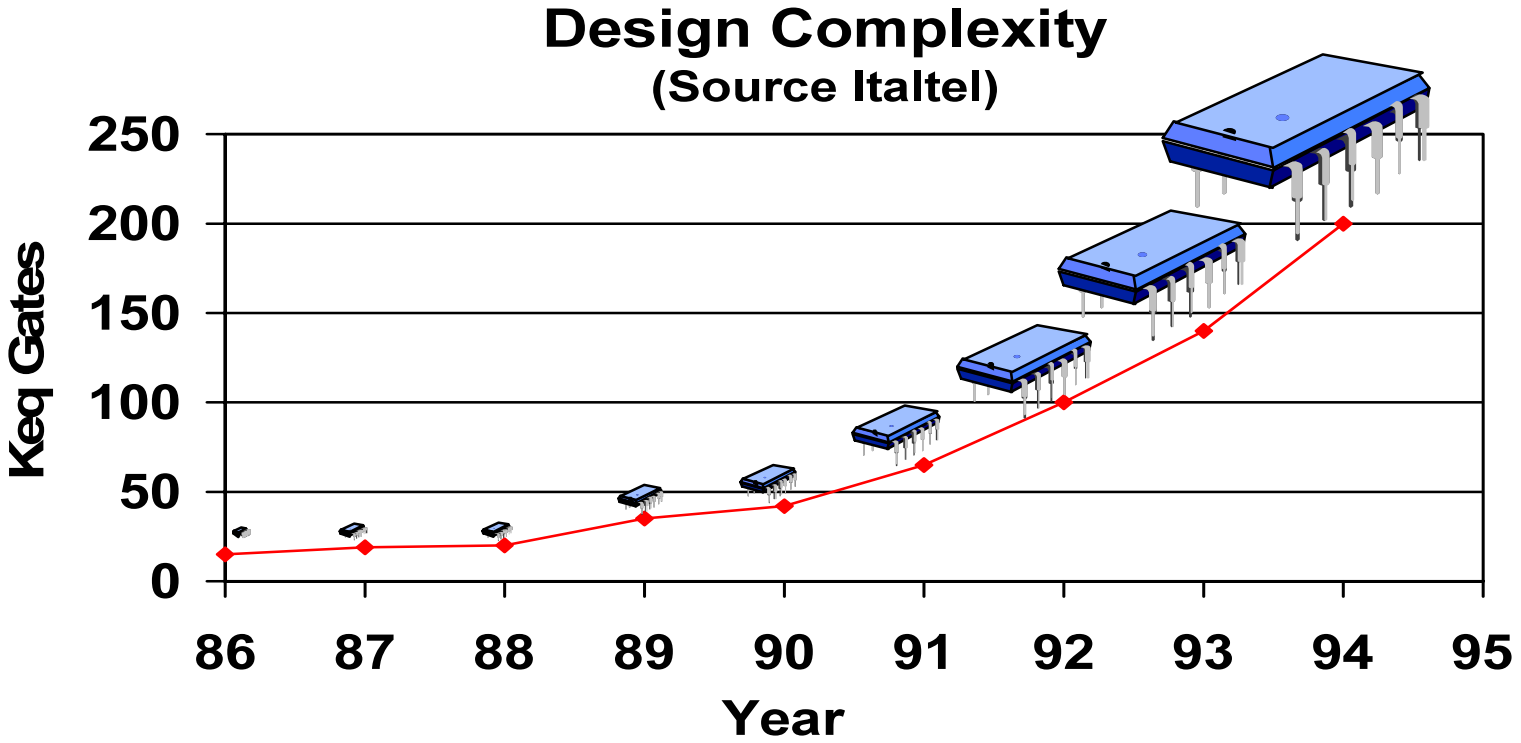
PRESENTATION OUTLINE



- ☑ INTRODUCTION
- ☑ PRODUCTIVITY
- ☑ REUSE
- ☑ QUALITY IMPROVEMENT
- ☑ CONCLUSIONS
- ☑ QUESTIONS & ANSWERS

INTRODUCTION: Trends



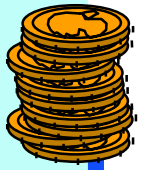
Gate count doubles each 2 years

Systems on a Chip

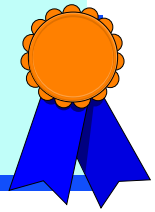
INTRODUCTION: Request Scenario

Needs

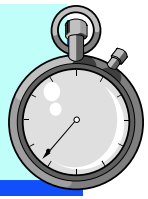
Minimize Cost



Increase Reliability



Reduce Time To Market

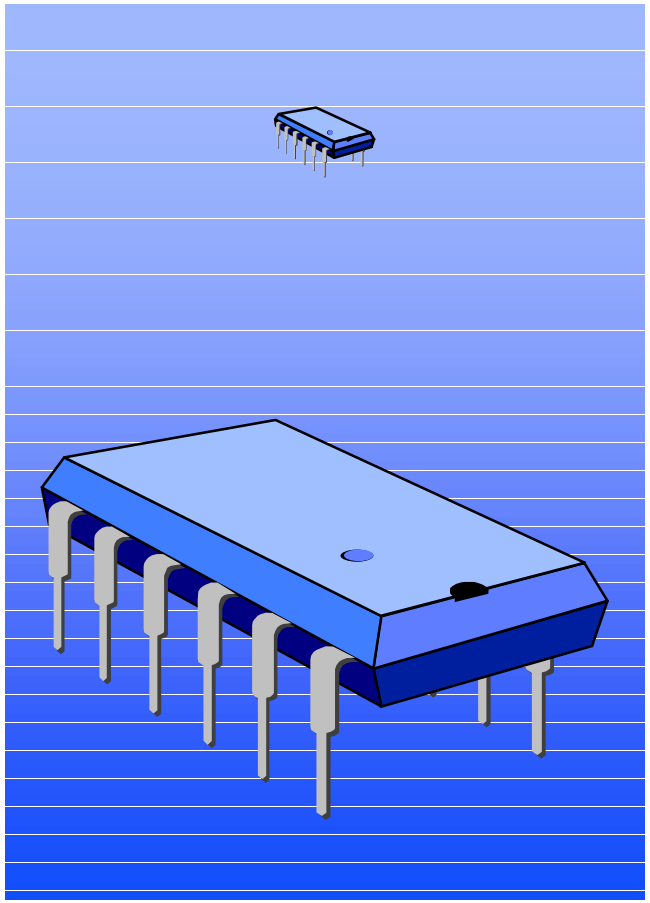


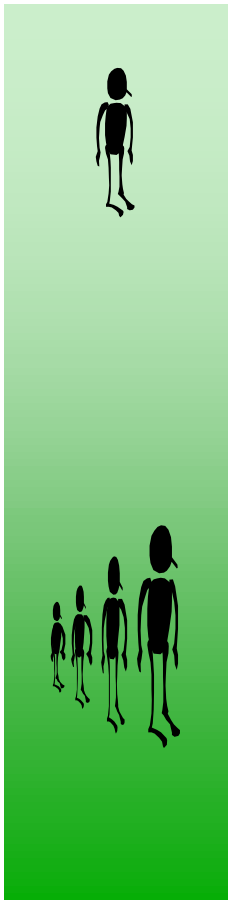
Request Solutions

Enhance Reusability of HDL Models

Enhance Design Quality

PRODUCTIVITY. Introduction

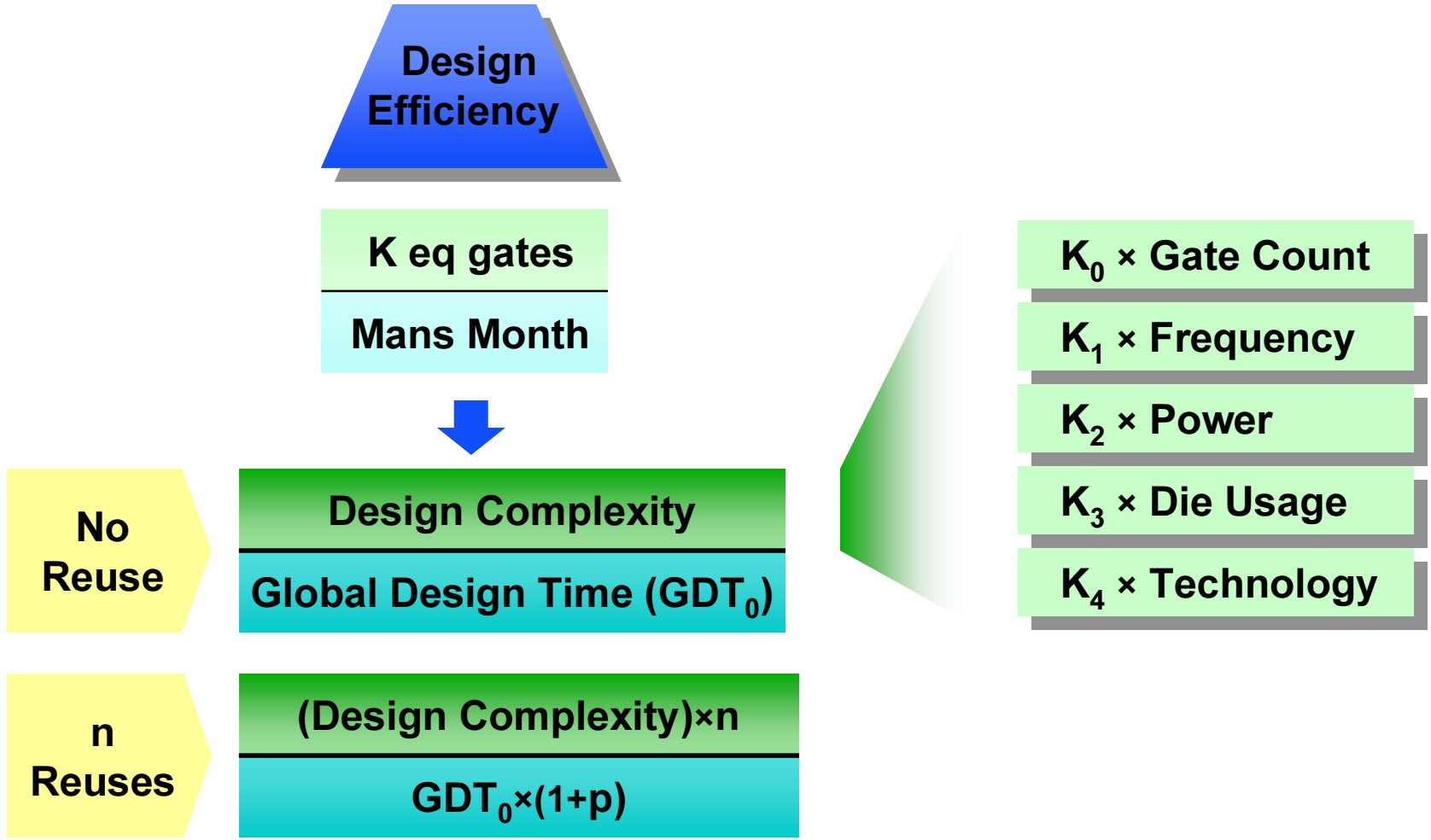




Complexity Increases more than design teams

Increase Design Efficiency

PRODUCTIVITY. Design Efficiency



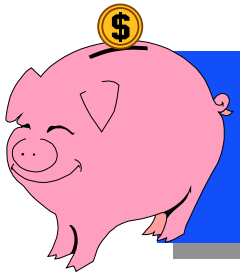
REUSE. Concept

Apply the Same Model In different Applications

Benefits for Designers

- Stable design specs
- Accurate estimations
- Hints on implementation
- Design Exploration

REUSE. Model 1



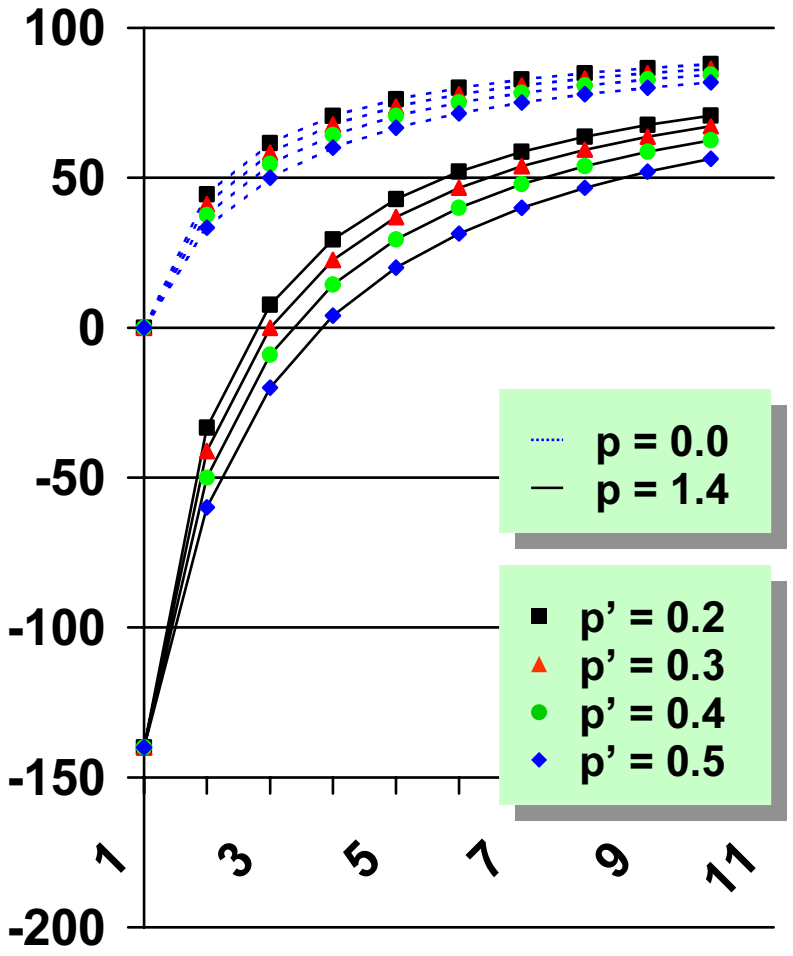
Savings in Design Time

$$1 - \frac{GDT_0 \times (1+p)}{GDT_0 \times (1 + (n-1)\times(1-p'))}$$

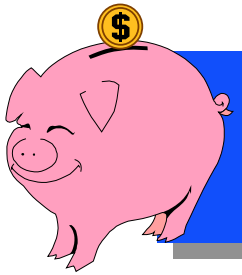
n = Number of reuses

p = Overhead in design time

p' = Correction for experience



REUSE. Model 2



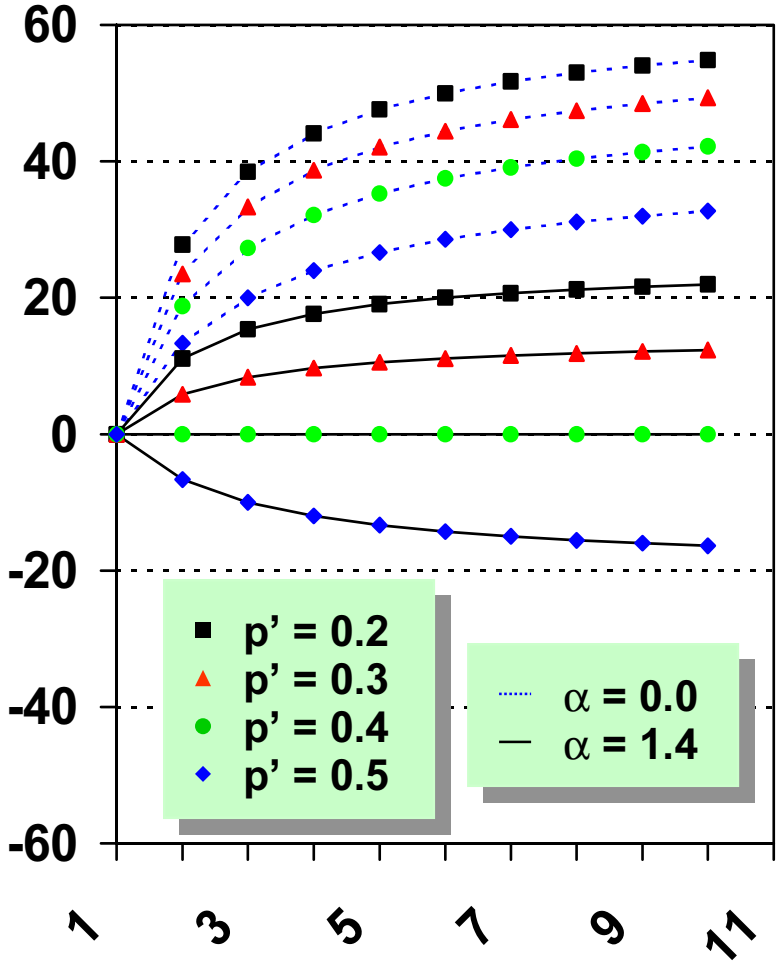
Savings in design time
Overhead proportional to number of reuses

$$1 - \frac{GDT_0 \times (1 + \alpha \times (n-1))}{GDT_0 \times (1 + (n-1) \times (1-p'))}$$

n = Number of reuses

α = Overhead in design time

p' = Correction for experience



REUSE. Macrocell types

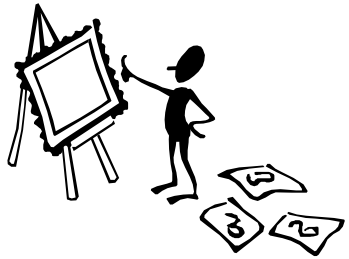
Level 1	Level 2	Level 3
Hard Macros ✓ High complexity ✓ Physical view ✓ Reuse ▫ No parameters ▫ No specialization ✓ Example: µP	**Soft Macros** ✓ Medium complexity ✓ Functional view ✓ Reuse ▫ Parametrization ▫ High value-added ✓ Example: Filters	**Technological Cells** ✓ Low Complexity ✓ Physical/Functional ✓ Reuse ▫ Libraries ▫ Generators ✓ Example: RAM

Best candidates for Reusable Techniques

REUSE. Environmets

	VHDL	Verilog
1	Parametrization (Generics)	Parametrization (Parameter)
2	Conditional Implementation	Conditional Implementation
3	Automatic Generation (Generate)	Preprocessor *Scripts*
4	External Generator Routines	External Generator Routines
5	*Copy & Paste*	*Copy & Paste*

QUALITY IMPROVEMENT

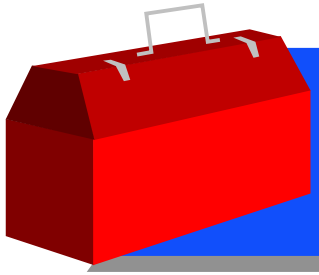


Quality is defined in terms of Relevant Attributes for a particular use

for VHDL Models

- **Reliability**
- **Suitability of models for the whole design flow**
- **Readability**
- **Efficiency in design an production cycles**

QUALITY IMPROVEMENT. Approach



Set of Analysis Tools

Measure the quality of VHDL models

- Source code complexity
- Simulation efficiency
- Presynthesis estimation
- Testability

Check compliance of VHDL models

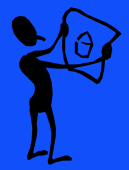
- User subsets
  - ✓ Logic synthesis subset
  - ✓ Application specific
- Coding Rules

QUALITY IMPROVEMENT. Impacts

Quality improvement impacts three different aspects

Efficient Implementation of Parameters

Area
Timing
Power



Compliance with Marquet Requirements

Testing

Reduction in Design Time

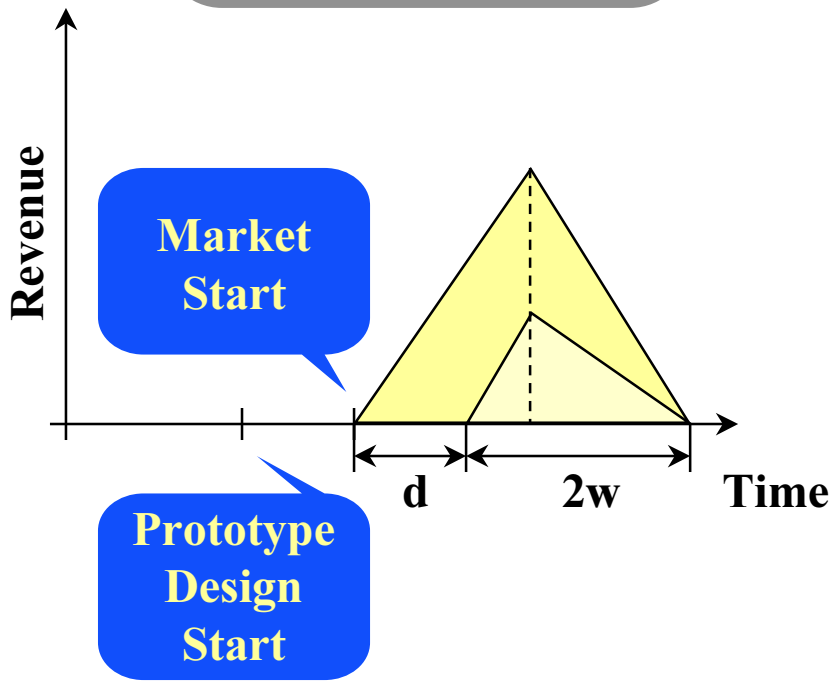
Simulation
Synthesis

QUALITY IMPROVEMENT. Life Cycle

Telecom Products Life Cycle

1. Analysis of Market
2. **Product Specification**
3. **Prototyping**
4. Production and Delivery
5. Support and Manteinance

Market loss (%)
$100d \times (3w-d)/(2w^2)$



CONCLUSIONS